Gray Shades in RMS Responding Displays With Wavelets Based on the Slant Transform

T. N. Ruckmongathan, Deepa S. Nadig, and P. R. Ranjitha

***Abstract*—A technique for displaying gray shades in root-mean-square responding displays is proposed. It is based on wavelets derived from a slant matrix of order 3. We have shown that the hardware complexity of display drivers and controller can be reduced to the same extent as that of the technique using the simple integer Haar wavelets. The number of time intervals to complete a cycle is 25% less than that of Haar wavelets, and we have also shown that it is not necessary to compute the orthogonal transform repeatedly.**

***Index Terms*—Gray shades, liquid-crystal displays (LCDs), matrix addressing, multiline addressing, wavelets.**

I. Introduction

MATRIX displays consist of N address lines (electrodes) and M data lines. Pixels are located at the intersection of these electrodes that are orthogonal to each other. Early addressing schemes were based on line-by-line addressing [1]. Nehring and Kmetz [2] explored the possibility of using orthogonal functions (like Walsh functions) and concluded that the selection ratio [ratio of root-mean-square (rms) voltages across the ON pixels to that across the OFF pixels] cannot exceed the limit $((\sqrt{N}+1)/(\sqrt{N}-1))^{1/2}$, where N is the number of lines scanned in a matrix display. However, there are several other advantages when a set of orthogonal functions (other than a set of rectangular pulses) is used for scanning the display. The second-generation techniques are based on selecting several address lines simultaneously by using orthogonal functions like Rademacher and Walsh functions [3]. Low supply voltage, good brightness uniformity among the pixels that are driven to the same state, etc., are some of the advantages of these techniques. In a matrix display, the address lines are scanned with waveforms derived from orthogonal functions, and the information is multiplexed through the data electrodes by applying waveforms that are proportional to the orthogonal transform of the data. Pixels in the rms responding displays act as detectors to demultiplex the data [4]. Most of the second-generation techniques were targeted for displaying bilevel information with pixels driven to either ON or OFF state. Limited number of gray shades can be displayed using techniques like pulse width modulation and frame rate control in conjunction with line-by-line or multiline addressing techniques. Techniques like amplitude modulation [5] and pulse height modulation [6] may be called the third-generation techniques because they are designed to display a large number of gray shades. Successive approximation techniques and the wavelet techniques [7], [8] are based on energy multiplexing. Capability to display a large number of gray shades with low hardware complexity of driver circuits is inherent in them because the number of time intervals is proportional to the logarithm of the number of gray shades. Selection ratio of these techniques is also a maximum. We have demonstrated a good reduction in hardware complexity of drivers and the controller of the passive matrix liquid crystal displays (LCDs) by using the modified integer Haar wavelets [8]. One of our aims is to show that neither the computation nor the hardware complexity increases when wavelets that are more complex than the integer Haar wavelets are used to scan the display. We have obtained a set of slant wavelets from the slant Hadamard matrix, which was proposed by Agaian *et al.* [9]. We have also shown that the number of time intervals can be reduced by 25% when slant wavelets are used instead of modified Haar wavelets to display 32 gray shades. The number of time intervals to complete a cycle depends on the number of gray shades as well as the choice of wavelets. Table I shows the number of time intervals to complete a cycle when integer Haar wavelets are used to display gray shades. Reducing the number

TABLE I
NUMBER OF TIME INTERVALS VERSUS NUMBER OF GRAY SHADES FOR HAAR WAVELETS

Number of gray shades	Number of time intervals in a cycle (Haar wavelets)
8	4N
16	8N
32	8N
64	8N

Manuscript received April 26, 2006; revised January 15, 2007. The review of this paper was arranged by Editor H.-S. Tae.

T. N. Ruckmongathan is with the Raman Research Institute, Bangalore 560080, India (e-mail: ruck@rri.res.in).

D. S. Nadig was with Visvesvaraya Technological University, Belgaum 590014, India. She is now with Wipro Technologies, Bangalore 560035, India (e-mail: nadig_ds@rediffmail.com).

P. R. Ranjitha was with Visvesvaraya Technological University, Belgaum 590014, India. She is now with Infosys Technologies, Bangalore 560100, India (e-mail: prranjitha@rediffmail.com).

Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/TED.2007.892023

of time intervals to complete a cycle is advantageous (assuming a constant refresh rate) for the following reasons.

1) Select time increases as the number of time intervals in a cycle decreases. Good brightness uniformity of pixels can be achieved when the select time is large because distortion in the addressing waveforms will be less, as the resistance–capacitance (RC) time constant will tend to be smaller than the select time.
2) Pixels in a matrix display can be modeled as variable capacitors, and power is dissipated in the ON resistance of the drivers when the pixels (capacitors) are charged and discharged to maintain the voltage across the pixels as dictated by the addressing technique [10]. Hence, power consumption in LCDs is similar to frequency-dependent power consumption in CMOS circuits because the power is dissipated whenever there is a transition in the addressing waveforms. Hence, techniques with less number of time intervals are preferred to reduce power consumption.

We have shown that the number of time intervals to complete a cycle can be reduced by 25% by using slant wavelets instead of Haar wavelets to display 32 gray shades. Slant wavelets for displaying 32 gray shades and construction of orthogonal matrices based on slant wavelets are outlined in Section II.

II. Slant Wavelets and Construction of Orthogonal Matrix

An orthogonal slant matrix proposed by Agaian [9] is shown here:

$$S_3 = \begin{bmatrix} \frac{1}{\sqrt{6}} & \frac{1}{0} & \frac{1}{\frac{-\sqrt{6}}{2}} \\ \frac{\sqrt{2}}{2} & -\sqrt{2} & \frac{\sqrt{2}}{2} \end{bmatrix}. \tag{1}$$

We have derived five wavelets from the orthogonal matrix S_3, and they satisfy the following conditions.

1) The energy of a wavelet is proportional to the weight of a bit of the gray shade.
2) Each wavelet is uniquely associated with 1 bit of the gray shade.
3) Wavelets are dc free to ensure long life of the display (application of dc voltages for a long duration will reduce the life of the display).

The five wavelets that satisfy these conditions are as follows:

$$w_{B4} = \{+4, +4, +4, -4, -4, -4\} \tag{2}$$

$$w_{B3} = \{+2\sqrt{6}, 0, -2\sqrt{6}\} \tag{3}$$

$$w_{B2} = \{+2\sqrt{3}, 0, -2\sqrt{3}\} \tag{4}$$

$$w_{B1} = \{+\sqrt{2}, -2\sqrt{2}, +\sqrt{2}\} \tag{5}$$

$$w_{B0} = \{+1, -2, +1\}. \tag{6}$$

These wavelets are more complex as compared to the wavelets in [7] and [8]. However, the use of these wavelets does not increase the hardware complexity of the drive electronics, as shown in this paper. The energies of these wavelets are 96, 48, 24, 12, and 6, respectively, and they are proportional $(\times 6)$ to the weight of bits in gray shade data. Subscripts $B4$ to $B0$ in (2)–(6) correspond to the binary weight of the gray shade data, as shown in the following expression:

$$g_{i,j} = \sum_{k=0}^{4} 2^k \cdot d_k \quad d_k = \begin{cases} +1, & \forall \text{ logic } 0 \\ -1, & \forall \text{ logic } 1 \end{cases}. \tag{7}$$

The values of the gray shades $g_{i,j}$ range from -31 to $+31$, and the neighboring gray shades differ by 2. Orthogonal matrices can be constructed with the wavelets in (2)–(6), and one such matrix is shown as follows:

$$O_{4\times 6} = \begin{bmatrix} +4 & -4 & +4 & -4 & +4 & -4 \\ +2\sqrt{6} & 0 & 0 & 0 & -2\sqrt{6} & 0 \\ 0 & +2\sqrt{3} & 0 & 0 & 0 & -2\sqrt{3} \\ +\sqrt{2} & +1 & -2\sqrt{2} & -2 & +\sqrt{2} & +1 \end{bmatrix}. \tag{8}$$

The number of nonzero elements is restricted to three in each select vector (columns of the orthogonal matrix) to reduce the hardware complexity of the data driver circuits. A data driver that is capable of selecting one out of eight voltages is adequate when the number of nonzero elements in the select vector is three. The number of rows in the orthogonal matrix is chosen to be four to reduce the hardware complexity of the controller, as explained in [8]. Several orthogonal matrices can be constructed using the wavelets in (2)–(6). An orthogonal matrix with three rows is

$$O_{3\times 6} = \begin{bmatrix} +4 & +4 & +4 & -4 & -4 & -4 \\ +2\sqrt{6} & 0 & -2\sqrt{6} & +2\sqrt{3} & 0 & -2\sqrt{3} \\ +\sqrt{2} & -2\sqrt{2} & +\sqrt{2} & +1 & -2 & +1 \end{bmatrix}. \tag{9}$$

The columns of the orthogonal matrix are referred to as the select vectors. Each element of the select vector corresponds to a bit of the gray shade data d_i. Data bits corresponding to the elements of the matrices in (8) and (9) are as follows:

$$D_{4\times 6} = \begin{bmatrix} d_4 & d_4 & d_4 & d_4 & d_4 & d_4 \\ d_3 & x & x & x & d_3 & x \\ x & d_2 & x & x & x & d_2 \\ d_1 & d_0 & d_1 & d_0 & d_1 & d_0 \end{bmatrix} \tag{10}$$

$$D_{3\times 6} = \begin{bmatrix} d_4 & d_4 & d_4 & d_4 & d_4 & d_4 \\ d_3 & x & d_3 & d_2 & x & d_2 \\ d_1 & d_1 & d_1 & d_0 & d_0 & d_0 \end{bmatrix}. \tag{11}$$

The x in data bit matrices corresponds to the zero in the orthogonal matrices.

III. Technique

Consider a matrix display with N and M electrodes that are orthogonal to each other and picture elements (pixels) located at the intersection of these address lines. Let the gray shade of a pixel located at the intersection of row i and column j be $g_{i,j}$, as given in (7). The address lines in the matrix display

are grouped into $(N/4)$ sets such that each set consists of four address lines. The steps involved in scanning the matrix display are as follows.

1) A set of address lines, i.e., four address lines are selected with voltages corresponding to one of the select vectors, i.e., a column in the orthogonal matrix in (8).
2) The data vector of each column in the matrix display is obtained by selecting the data bits of pixels in the selected rows and the elements of select vector, as shown by the data bit matrix in (10).
3) Data voltages (dot product of the select vector with the data vectors) are computed. For example, the data voltage when the select vector is the first column of the orthogonal matrix in (8) is as follows:

$$V_{\text{data}} = \begin{bmatrix} +4 \\ +2\sqrt{6} \\ 0 \\ +\sqrt{2} \end{bmatrix} \cdot \begin{bmatrix} d_4 \\ d_3 \\ 0 \\ d_1 \end{bmatrix} \cdot V_c. \tag{12}$$

   Here, d_4 ,d_3, and d_1 correspond to pixels in the first, second, and fourth address lines in the selected set. Subscripts (4 to 0) correspond to the bits, i.e., the most significant bit to the least significant bit.
4) Four address lines in a set are selected simultaneously for a time duration T (referred to as the select time) with voltages corresponding to one of the select vectors. For example, the address lines are selected by applying the voltages $+4\ V_r$, $+2\sqrt{6}\ V_r$, 0, and $+\sqrt{2}\ V_r$ to the first to fourth address lines in a set when the first column of the orthogonal matrix is the select vector.
5) Both select and data voltages are applied simultaneously to the corresponding electrodes for a duration T, which is referred to as the select interval T.
6) Select vector and the corresponding data vector are rotated (either up or down) vertically by one position. Three additional select vectors are obtained by rotating each select vector in (8) three times. Hence, the total number of select vectors is 24 (6×4).
7) The new select vector that is obtained by rotating a select vector in (8) is used to select either the same address lines or another set of address lines for a duration T, as described in steps 3 and 4.
8) A cycle is complete when the entire sets of address lines in the matrix display are selected with all the 24 select vectors, i.e., the 6 basic vectors and the 18 vectors derived by rotating them.

The display is refreshed continuously by repeating this cycle at a rate that is fast enough to avoid flicker and ensure rms response. The scanning sequence described here ensures that all the address lines in the matrix display are selected with the five wavelets once in each cycle. The waveforms across the pixels will be dc free because the wavelets are dc free. Typical waveforms of the addressing technique are shown in Fig. 1. The number of time intervals to complete a cycle is about $6N$. The analysis of this technique is presented in Section IV.

IV. Analysis

The rms voltage across a pixel when the matrix display is scanned with waveforms corresponding to the orthogonal matrix in (8) is as follows:

$$V_{\text{pixel}}(\text{rms}) = \sqrt{\frac{6\sum_{k=0}^{4} 2^k \left(V_r^2 - 2 \cdot d_{k,i,j} V_r \cdot V_c + N \cdot V_c^2\right)}{6N}} \tag{13}$$

$$V_{\text{ON}}(\text{rms}) = \sqrt{\frac{31\left(V_r^2 + 2V_r \cdot V_c + N \cdot V_c^2\right)}{N}} \tag{14}$$

$$V_{\text{OFF}}(\text{rms}) = \sqrt{\frac{31\left(V_r^2 - 2V_r \cdot V_c + N \cdot V_c^2\right)}{N}}. \tag{15}$$

The ratio of rms voltage across the ON pixels to that across the OFF pixels is called the selection ratio. It is a measure of the performance of the addressing technique, and a high selection ratio is preferred to achieve a high contrast in the display. It is a maximum when

$$\frac{V_r}{V_c} = \sqrt{N} \tag{16}$$

$$\text{Maximum selection ratio} = \sqrt{\frac{\sqrt{N}+1}{\sqrt{N}-1}}. \tag{17}$$

It is the maximum selection ratio that is achievable by any addressing technique employed for driving the rms responding passive matrix LCD. A good contrast is obtained when the rms voltage across the OFF pixels in the display is biased near the threshold voltage of the LCD. The voltage V_c is obtained by equating the voltage across the OFF pixels to the threshold voltage $V_{\text{threshold}}$ of the liquid crystal display, i.e.,

$$V_{\text{OFF}} = \sqrt{\frac{31(2N - 2\sqrt{N})}{N}} \cdot V_c = V_{\text{threshold}}. \tag{18}$$

Hence

$$V_c = \frac{V_{\text{threshold}}}{\sqrt{62\left(1 - \frac{1}{\sqrt{N}}\right)}}. \tag{19}$$

The supply voltage of the drive electronics is determined by the maximum swing in the addressing waveforms. The amplitude of the scanning waveforms increases, and that of the data waveforms decreases as the number of address lines that are multiplexed is increased in multiline addressing techniques. Hence, the expression for the supply voltage when N is small is determined by the maximum swing in the data waveforms, whereas the supply voltage is determined by the maximum swing in the scanning waveforms when N is large.

The maximum amplitude of the data waveforms and scanning waveforms are as follows:

$$\text{Data voltage (max)} = \left(2\sqrt{6} + 4 + \sqrt{2}\right) \cdot V_c \tag{20}$$

$$\text{Scanning voltage (max)} = 2\sqrt{6}\sqrt{N} \cdot V_c. \tag{21}$$

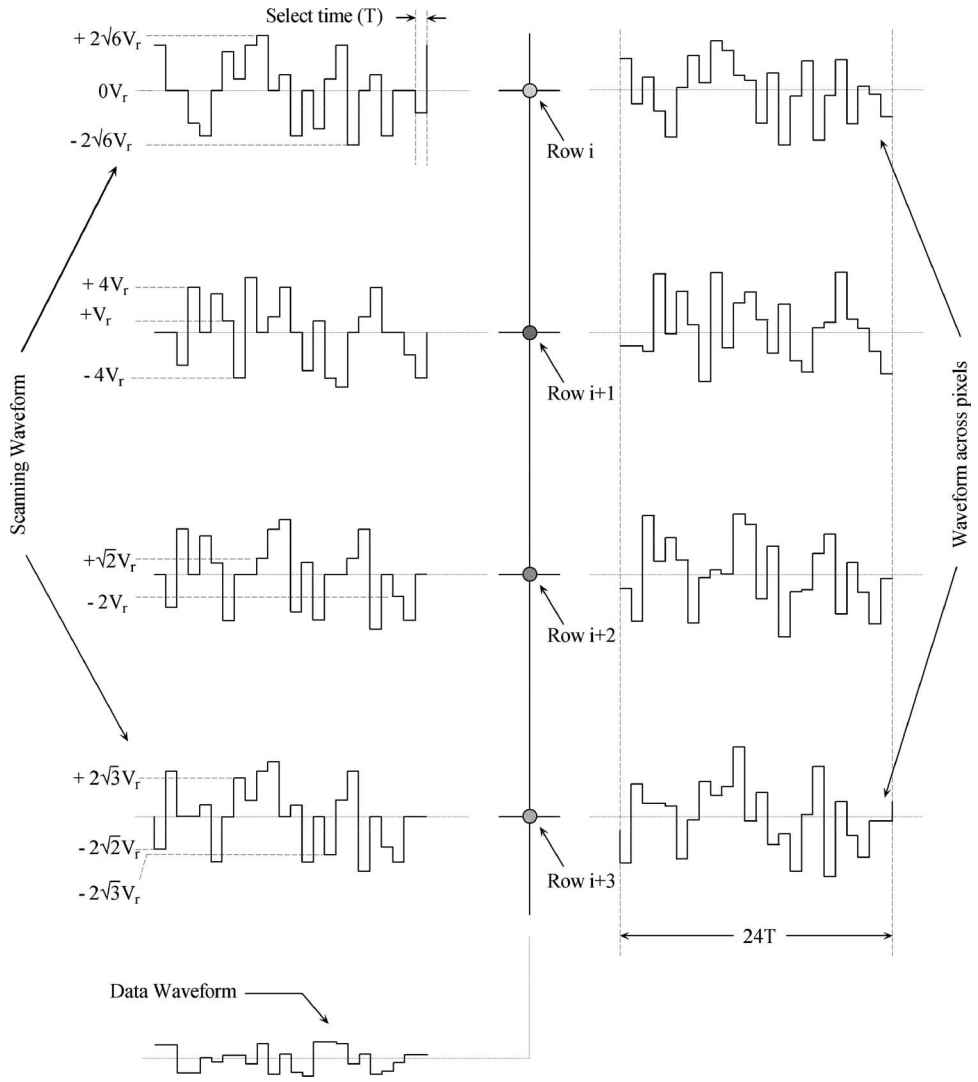


Fig. 1. Typical waveforms when slant (noninteger) wavelets are used to scan the rms responding matrix displays. The scanning and data waveforms have eleven and eighteen voltages respectively.

Hence, the supply voltage of the drive electronics is as follows:

$$V_s = \begin{cases} (\sqrt{96} + 8 + \sqrt{8})V_c, & \forall N < 5 \\ \sqrt{96N}\,V_c, & \forall N \geq 5 \end{cases}. \tag{22}$$

The supply voltage for most practical values $(N > 5)$ is given as follows:

$$\text{Supply voltage}_{(N \geq 5)} = \frac{\sqrt{96N}}{\sqrt{62\left(1 - \frac{1}{\sqrt{N}}\right)}} V_{\text{threshold}}. \tag{23}$$

A plot of the supply voltage for this range is shown in Fig. 2. The analysis presented in this paper is independent of the scanning sequence, which is the order in which the scanning electrodes are selected with select vectors. There are (24!) possible ways of selecting four address lines (a set) with the 24 select vectors. The $(N/4)$ sets (of address lines) themselves can be chosen in any one of the $(N/4)!$ ways. Although there

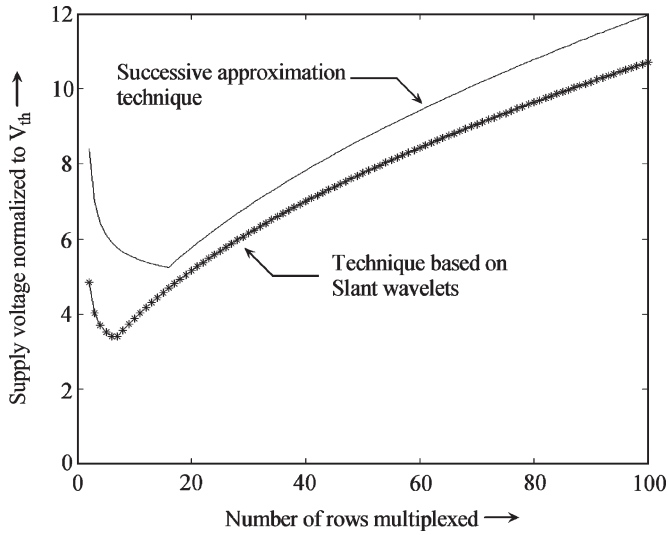


Fig. 2. Supply voltages of the technique based on slant wavelets as compared with that of successive approximation technique.

are many possible ways of selecting the address lines, the rms voltage across the pixels will be the same as long as the RC time constant of the drive circuit is small as compared to the select time T. Drive waveforms will get distorted (due to the ON resistance of the drivers and the capacitance of the pixels) whenever there is a transition in the waveforms. The number of transitions in the addressing waveforms is determined by the scanning sequence. If the RC time constant is large, then the rms voltages across the pixels will be less due to distortion in the waveforms. The number of transitions in the addressing waveforms also determines the power dissipated in the drivers. It is also preferable to have smaller amplitude of transitions to reduce the power consumption. The frequency spectrum across the pixels is also determined by the addressing sequence.

V. Hardware Complexity of the Drive Electronics

The technique is demonstrated with a 32×32 matrix twisted nematic (TN) LCD. Although we have used relatively more complex wavelets as compared to the modified integer Haar wavelets [7], [8], the hardware complexity of the drive electronics is about the same as that of the integer wavelets, as discussed in the following sections.

A. Reducing Hardware Complexity of the Row Drivers

The number of nonzero elements in each column of the orthogonal matrix in (8) is intentionally restricted to only three to reduce the hardware complexity of the row drivers. The number of voltages in the scanning waveforms is only four out of the 11 possible values at a given time. The 11 possible values are as follows:

$$+4, +2\sqrt{6}, +2\sqrt{3}, +\sqrt{2}, +1, 0, -2, -2\sqrt{2}, -2\sqrt{3}, -2\sqrt{6}, -4.$$

Hence, it is adequate to have the following elements in each stage (corresponding to one output) of the row driver integrated circuit (IC).

1) A 2-bit shift register to enable serial transfer of data into the driver IC.
2) A 2-bit latch to hold the data stable during a select time (and allow serial transfer of the data in the shift register) so that the desired voltage can be applied to the address lines. One of the four voltages corresponds to the zero in the orthogonal matrix, and it is the same as the nonselect voltage.
3) A $4:1$ analog multiplexer to select one of the four voltages on the internal bus of the driver IC. The select input of the multiplexer is the output of the 2-bit latch of the same stage.

Two $4:1$ analog multiplexers and a $2:1$ analog multiplexer are provided to reduce the hardware complexity of the drivers. They are common to all stages of the row drivers. They connect the three nonzero select voltages to the voltage bus in the row drivers, and they may be located outside the data driver ICs because multiple number of driver ICs may be used in the displays. A block diagram of the row driver circuit that can be used to scan the display is shown in Fig. 3. Hardware complexity

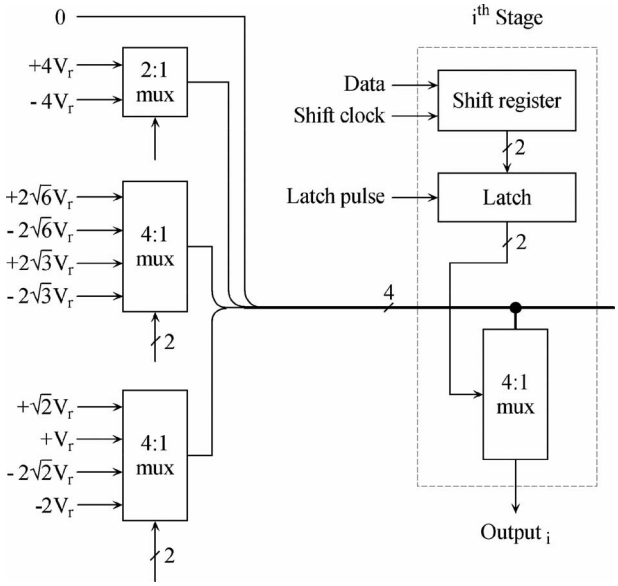


Fig. 3. One stage (i) of the row drivers having a $(4:1)$ analog multiplexer, 2-bit latches, and a stage of the 2-bit shift register (to shift in the data serially) is shown inside the box. Two $4:1$ analog multiplexers and a $2:1$ analog multiplexer that are common to all the stages of the row drivers are useful to reduce the hardware complexity of the row driver circuit.

of the shift register, latch, and multiplexer is reduced by 50%, 50%, and 64%, respectively, as compared to using a driver that is capable of selecting one out of eleven voltages using 4-bit shift register, 4-bit latches, and $11:1$ analog multiplexers in the driver IC. Addition of three multiplexers (as shown in Fig. 3) does not increase the hardware complexity of the drive circuit significantly because the number of rows N in the matrix display is usually large.

B. Reducing Hardware Complexity of the Column Drivers

The number of voltages in the column (data) waveforms is 24, and a 5-bit shift register, a 5-bit latch, and $24:1$ analog multiplexers may be used to generate the column (data) waveforms. However, only four or eight voltages are necessary at a given time, depending on the number of zeros (two or one) in the select vector. Hardware complexity of the column drivers can be reduced by using eight $4:1$ analog multiplexers that are common to all the data drivers, along with driver ICs (with 3-bit shift register, 3-bit latch and $8:1$ analog multiplexer in each stage) that are capable of applying any one of the eight voltages depending on 3 bits of the data. Hardware complexity in the column drivers is reduced by 40%, 40%, and 66% for the shift registers, latches, and analog multiplexers, respectively. The increase in hardware complexity due to the eight $4:1$ multiplexers is not significant because the number of columns (data electrodes) in a display is usually large. A block diagram of the column driver circuit is shown in Fig. 4.

C. Generation of Data for the Column Driver

Although the column voltage is proportional to the dot product of the select vector and the data vector, it is not necessary to compute this dot product repeatedly while scanning the display. The result of the dot product of a select vector with any data

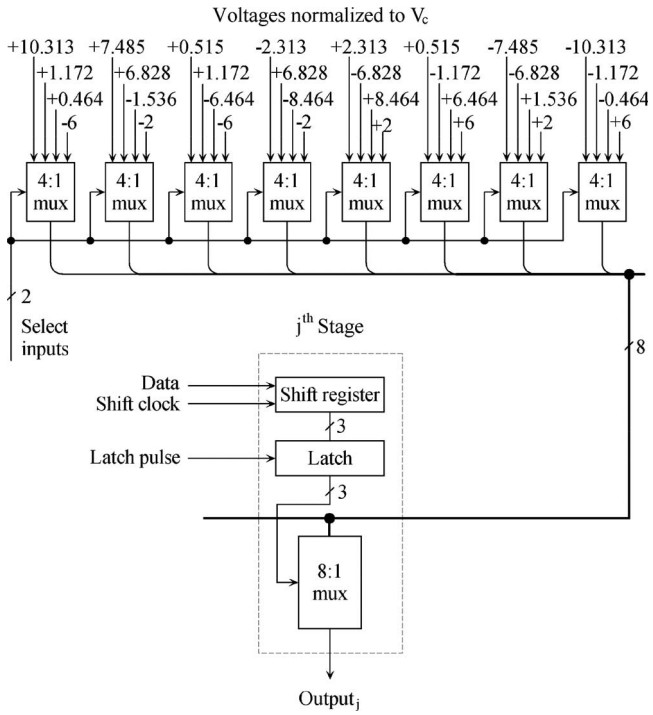


Fig. 4. Drivers with a 3-bit shift register, a 3-bit latch, and an 8 : 1 analog multiplexer are used as the column drivers considering the fact that the number of voltages corresponding to each select vector is either eight or four, although the number of voltages in the data (column) waveforms is 24. We have used eight 4 : 1 analog multiplexers that are common to all the stages of the data drivers to avoid using drivers with a 5-bit shift register, a 5-bit latch, and 24 : 1 analog multiplexers. Input voltages to the eight (4 : 1) multiplexers are normalized to V_c.

vector is only one of the eight or four values for the following reasons.

1) The number of unique select vectors is limited, and the rotated versions of a select vector and the select vectors whose elements differ only in sign and not in magnitude are not considered to be unique. For example, the vectors in the following equation are not unique:

$$\begin{bmatrix} -4 \\ 0 \\ +2\sqrt{3} \\ +1 \end{bmatrix}, \begin{bmatrix} +1 \\ -4 \\ 0 \\ +2\sqrt{3} \end{bmatrix}, \begin{bmatrix} -4 \\ 0 \\ -2\sqrt{3} \\ +1 \end{bmatrix}, \begin{bmatrix} -2\sqrt{3} \\ +1 \\ -4 \\ 0 \end{bmatrix}, \ldots . \tag{24}$$

2) The number of nonzero elements in the select vectors is either three or two to reduce the hardware complexity of the column (data) drivers.
3) The elements of the data vectors are either $+1$ or -1 because they correspond to only 1 bit of the data.

The number of unique select vectors in the orthogonal matrix of (8) is only four. It is enough to compute the dot products during the design of the voltage level generator (VLG). Voltages from the VLG are inputs to the eight 4 : 1 analog multiplexers that are common to all column driver ICs. Outputs of the multiplexers are connected to the voltage bus in the column drivers. These eight multiplexer select voltages correspond to one of the four unique select vectors. The data bits corresponding to the nonzero elements are shifted into column driver to

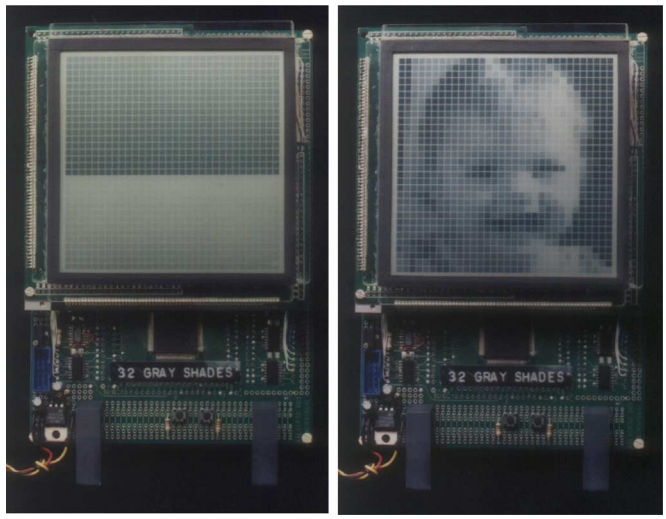


Fig. 5. Photographs of a 32 × 32 matrix display that is capable of displaying 32 gray shades.

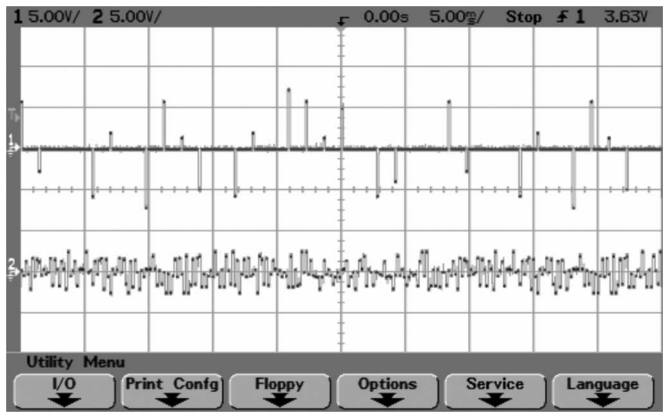


Fig. 6. Typical row (scanning) and column (data) waveforms when 32 gray shades are displayed in a 32 × 32 matrix LCD.

select one of the eight voltages in the bus. Hence, it is not necessary to compute the dot product, and complex wavelets (if they are advantageous for other reasons) could be used without increasing the hardware complexity of the drive electronics as compared to using integer wavelets [7]. Controller is also simple when the number of address lines is an integer power of 2, as explained in [8].

D. Implementation

The technique is demonstrated with a 32 × 32 matrix TN liquid crystal display, and the photographs of the prototype are shown in Fig. 5. We have used drivers that are capable of applying one of the eight voltages with an 8 : 1 multiplexer as both row and column drivers, although it is adequate to have drivers that are capable of applying only four levels as row drivers. A controller for refreshing the display was implemented in a complex programmable logic device (XCR 3256 XL) using 106 macrocells, 243 product terms, and 68 registers. Typical row and column waveforms are shown in Fig. 6, and the waveform across a pixel is shown in Fig. 7. Response times were measured when the pixels are switched from a gray to

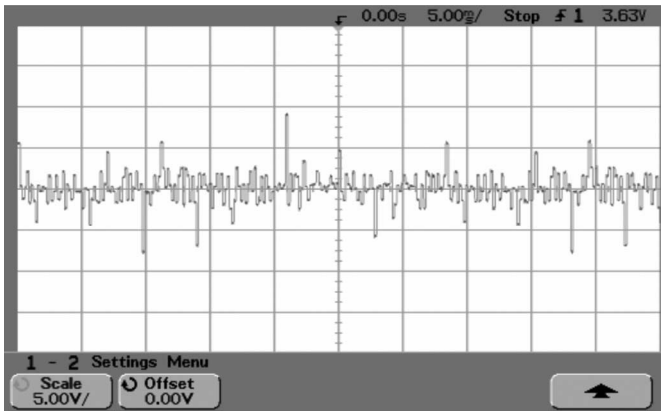


Fig. 7. Typical waveform across a pixel (row waveform minus column waveform) in the prototype of the display capable of displaying 32 gray shades.

TABLE II
RESPONSE TIMES (IN MILLISECONDS) WHEN PIXELS ARE SWITCHED TO DIFFERENT GRAY SHADES USING WAVELETS

Gray shade value	0	3	7	11	15	19	23	27	31 (ON)
0 (OFF)	-	72	65	60	55	52	50	44	40
3	75	-	68	70	56	61	58	55	52
7	70	78	-	72	57	54	52	50	50
11	61	75	75	-	73	58	55	48	40
15	60	73	64	80	-	78	63	55	53
19	58	75	60	65	90	-	65	54	51
23	50	70	58	66	75	87	-	60	55
27	45	60	56	60	58	73	72	-	44
31 (ON)	44	65	54	52	55	65	69	59	-

another, and the results are shown in Table II. The following information is useful for comparing the response times of the display under multiplexed (Table II) and nonmultiplexed conditions. The switch ON and switch OFF times of a cell of 3.9 μm and filled with the liquid crystal mixture RO-TN-403 were 30 and 12 ms, respectively. The voltage across the pixel was switched to 1.33 V (threshold voltage of the display) and 1.58 V (voltage across an ON pixel when the number of lines multiplexed is 32) alternately, by applying square waveforms.

VI. COMPARISON WITH OTHER TECHNIQUES

Amplitude modulation needs 62 voltages in the column waveforms and three voltages in the row waveforms to display 32 gray shades. It takes $4N$ time intervals (including dc-free operation) to complete a cycle when the gray shades are displayed using amplitude modulation technique [5]. A similar technique called pulse height modulation technique also needs a large number of voltages in the data waveforms [6]. It is more appropriate to compare the wavelet-based techniques with the successive approximation techniques [11], [12] because both these techniques are based on modulating the energy delivered to the pixels using several time intervals. A comparison of the wavelet-based technique with successive approximation techniques is given in Table III. Although the number of voltages in the waveforms is more when slant wavelets are used, the hardware complexity of drive electronics can be reduced, as discussed in this paper.

TABLE III
COMPARISON OF THE GRAY SHADE TECHNIQUES (32 GRAY SHADES)

Parameter	Successive approximation technique (Line-by-line) [12]	Successive approximation (MLA) 4 lines in a subgroup [11]	Technique Based on Integer Haar Wavelets [7], [8]	Technique based on modified Slant Wavelets
Number of time intervals in a cycle	10N	10N	8N	6N
Number of voltages in scanning waveforms	11 (16 for IAPT)	11	5	11
Number of voltages in the data waveforms	10 (16 for IAPT)	15	11	24

VII. MERITS AND DEMERITS

Some of the advantages of the technique are as follows.

1) Less number of time intervals as compared to using Haar wavelets.
2) The ratio of the maximum to minimum response times is about 2. It is less than that of other techniques.
3) The supply voltage of the wavelet-based technique is less even when it is compared with successive approximation technique that is based on selecting four address lines simultaneously (only three address lines are selected simultaneously although the number of rows in a set is four).
4) The hardware complexity of the data drivers is low (by a factor of $\sim$8) as compared to the amplitude modulation and pulse height modulation.

The disadvantage of this technique are as follows.

1) The number of time intervals to complete addressing is 20% higher than the successive approximation technique if the DC free condition is ignored.
2) The number of time intervals is 50% more than the amplitude or pulse height modulations.

VIII. Conclusion

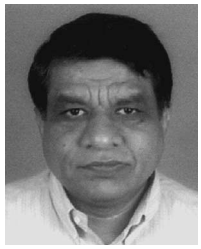
We have shown that the number of time intervals to complete a cycle can be reduced when the number of gray shades is 16, 32, etc., by using slant wavelets. We have also shown that the hardware complexity of the drive electronics does not increase when complex noninteger wavelets are used to scan the display as compared to the integer wavelets. The techniques for eliminating repeated computation of the orthogonal transform of the data and the reduction of hardware complexity can be applied even when other wavelets are used for scanning the display.

Acknowledgment

The authors would like to thank A. R. Shashidhara for fabrication of the display and for support in hardware implementation of the technique and the reviewer for suggesting to include some historical perspective and a discussion on merits and demerits of this technique.

References

[1] P. M. Alt and P. Pleshko, "Scanning limitations of liquid crystal displays," *IEEE Trans. Electron Devices*, vol. ED-21, no. 2, pp. 146–155, Feb. 1974.
[2] J. Nehring and A. R. Kmetz, "Ultimate limits for matrix addressing of RMS responding liquid crystal displays," *IEEE Trans. Electron Devices*, vol. ED-26, no. 5, pp. 795–802, May 1979.
[3] T. N. Ruckmongathan, "Novel addressing methods for fast responding LCDs," *Asahi garasu kenkyu hokoku*, vol. 43, no. 1, pp. 65–87, 1993.
[4] ——, "Recent developments in addressing passive matrix LCDs," in *Proc. CEOT*, 1994, pp. 302–306.
[5] ——, "Addressing techniques for RMS responding LCDs—A review," in *Proc. 12th Int. Display Res. Conf. (Japan Display)*, 1992, pp. 77–80.
[6] A. R. Conner and T. J. Scheffer, "Pulse height modulation gray shading methods for passive matrix LCDs," in *Proc. 12th Int. Display Res. Conf. (Japan Display)*, 1992, pp. 69–72.
[7] T. N. Ruckmongathan, R. P. Nanditha, and A. Prasad, "Wavelets for displaying gray shades in LCDs," in *Proc. Soc. Inf. Display Int. Symp. Dig. Tech. Papers*, 2005, pp. 168–171.
[8] T. N. Ruckmongathan, U. Manasa, R. Nethravathi, and A. R. Shashidhara, "Integer wavelets for displaying gray shades in RMS responding displays," *IEEE/OSA J. Display Technol.*, vol. 3, no. 3, pp. 292–299, Sep. 2006.
[9] S. Agaian, K. Tourshan, and J. P. Noonan, "Generalized parametric slant Hadamard transform," *Signal Process.*, vol. 84, no. 8, pp. 1299–1306, Aug. 2004.
[10] T. N. Ruckmongathan, M. Govind, and G. Deepak, "Reducing power consumption in passive matrix liquid crystal displays," *IEEE Trans. Electron Devices*, vol. 53, no. 7, pp. 1559–1566, Jul. 2006.
[11] K. G. PaniKumar and T. N. Ruckmongathan, "Displaying gray shades in passive matrix LCDs using successive approximation," in *Proc. 7th ASID*, Sep. 2–4, 2002, pp. 229–232.
[12] T. N. Ruckmongathan, "A successive approximation technique for displaying gray shades in liquid crystal displays (LCDs)," *IEEE Trans. Image Process.*, vol. 16, no. 2, pp. 554–561, Feb. 2007.



T. N. Ruckmongathan received the B.E. degree in electronics and communication engineering from the University of Madras, Madras, India, in 1976 and the M.E. and Ph.D. degrees in electrical communication engineering from the Indian Institute of Science, Bangalore, India, in 1978 and 1988, respectively. Driving matrix liquid crystal displays has been his main field of study.

He is a Professor at the Raman Research Institute, Bangalore, India. He was a Visiting Professor at the Chalmers University of Technology, Gteborg, Sweden, during 1998, a Guest Researcher at Asahi Glass Co. R&D, Yokohama, Japan, during 1991–1993, and an LCD Specialist at Philips, Heerlen, The Netherlands, during 1989 to 1991. His pioneering work on multiline addressing techniques, "A generalized addressing technique for rms responding LCDs," was presented at the 1988 International Display Research Conference, San Diego, CA. The analysis presented in this paper holds good for most of the multiline addressing techniques. His research work on multiline addressing is cited in 91 U.S. patents. His main interest is in the research and development of new addressing techniques for driving matrix LCD.

Dr. Ruckmongathan is a member of the Society for Information Display.

Deepa S. Nadig received the B.E. degree in electronics and communication engineering from Visvesvaraya Technological University, Belgaum, India, in 2005.

She is currently with Wipro Technologies, Bangalore, India.

P. R. Ranjitha received the B.E. degree in electronics and communication engineering from Visvesvaraya Technological University, Belgaum, India, in 2005.

She is currently with Infosys Technologies, Bangalore, India.