CHAPTER 3

HARDWARE DESIGN

The block diagram of the entire digital receiver system is shown in Fig. 3.1. Blocks which have not been explained earlier are

1. The Astronomical clock which displays sidereal time, Indian Standard Time and Julian Day.

2. A single channel correlator with display designed as a test equipment.

3. An HP printer with an interface to print out the correlation values.

This chapter discusses the hardware details of each block shown in Fig. 3.1.

3.1 PREAMPLIFIERS

4 rows of dipoles are combined with phase shifters to form a group. There are 23 such groups in the N-S array. Each group output has to be amplified before being brought to the receiver room on open wire transmission lines. The

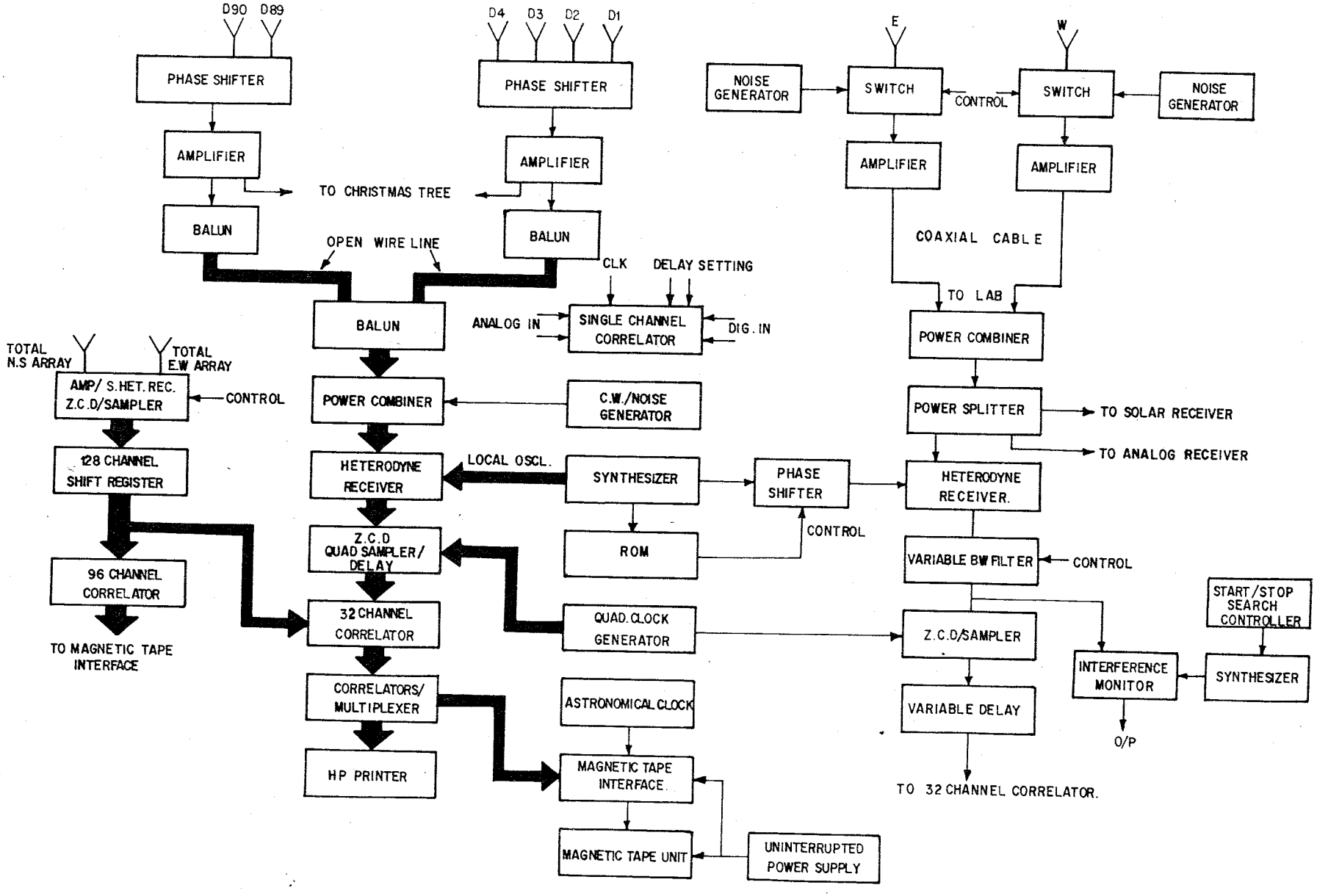


FIG. 3·1 BLOCK DIAGRAM OF THE MULTIBEAM FORMING RECEIVER SYSTEM.

total length of openwire transmission lines layed for this is more than 12 kms. Important specifications of the preamplifier are its gain, bandwidth, noise figure and intermodulation distortion.

3.1.1 Gain

1. Very high gain leads to instabilities. Generally it is common practice to put all the gain in the IF stage in most superheterodyne receivers. Higher gain, requires larger signal handling capability, and hence higher power. Since these preamplifiers are placed in the field, it is desirable to keep their power consumption to a minimum. This makes power distribution easy and on board regulation simple. A gain lower than the loss of the cable and other modules between this amplifier and the next amplifier stage will deteriorate the noise figure of the system. In the present case, the loss of the openwire transmission line carrying the signal to the lab is around 10 db. The openwire transmission lines are affected by weather and even lightning. Thus it may become necessary in the future to replace them by co-axial cables. Even then, the transmission loss will not be greater than 30db. Thus it is desirable to have a gain around 40 db for the amplifiers. These amplifiers will feed power to the existing christmas tree, and to the new digital receiver. Thus there will be an additional 3 dB loss in the hybrid splitting power to the two systems. Since the digital system uses a one-bit

correlator, the amplifier gains are not critical. But they have to be maintained the same for all the amplifiers to achieve uniform grading of the antenna for the analog receiver.

3.1.2 Band Shape

The bandshape is determined by the centre frequency of operation, the IF of the heterodyne receiver and the LO frequency. They are in the present case 34.5, 4 and 30.5 MHz respectively. It is preferable that the image frequencies are filtered in the first stage itself. It is also necessary that the broadcast band (below 15 MHz) is well suppressed. The bandwidth of the FET amplifiers preceding the phase shifters is around 2 MHz. All these considerations lead to the following specifications.

Centre frequency = 34.5 MHz

3dB bandwidth = at least 2 MHz

cut off at 30.5 MHz = 30 dB

(to reduce LO leakage)

Cut off at 27.5 MHz = 40 dB

(27.5 MHz is the highest frequency of the image of a 2 MHz band around 34.5 MHz)

Either a bandpass or a highpass amplifier can be designed to satisfy the above requirements. The present amplifier uses a bandpass network.

3.1.3 Noise Figure

The noise figure required depends upon the antenna temperature, noise figure and gain of the preceding stages. In the decametric region, the background temperature varies from around 40,000 K in the direction of the galactic centre to around 10,000 K in the direction of the poles. For a broad feature like the background, the antenna temperature will be equal to the sky brightness temperature. The Noise Figure of the FET amplifier is around 600 K, and its gain is 6 dB. The loss of the cable and phase shifters preceding this amplifier is around 4 dB. Thus it is essential that the NF of this stage is kept as low as possible. The following reasons led to the choice of a 'cascode' configuration (CE-CB) for the amplifier in order to obtain minimum noise temperature for the amplifier.

1. The noise figures for the common base and common emitter configurations are almost the same.

2. The source resistance (RSNF) for the minimum noise figure is approximately equal to the source resistance for maximum common emitter gain (RSG). The RSNF is always within a factor of 2 of the RSG. From the stand point of minimum low-frequency noise figure, together with the maximum low frequency gain, a common emitter configuration is the best choice. For any RSG within a factor of 2 of the RSNF, the noise figure will not increase by more than 0.5 decibel. For a factor of 5, the noise figure will not

increase by more than 2.5 dB (Neilsen 1957).

3.The value of emitter current (I_e) in the cascode was determined by the following considerations. The noise figure deteriorates slowly with increasing I_e. Usually, higher I_e is required for higher dynamic range and less distortion. For very low I_e, the noise figure deteriorates again. This is caused by the decrease in alpha at low currents.

3.1.4 Intermodulation Distortion (IMD)

The non-linear transfer characteristics of the active devices cause distortion. An exact knowledge of all the spurious signals is essential where an optimum trade-off between dynamic range and low noise is required in astronomical receivers. This has become very important because of the overcrowding of the frequency spectrum.

The IMD of amplifiers is specified by the "Third order Intercept", which is the point of intersection of the fundamental and the third order responses on a log-log scale (McVay, 1967). The fundamental responses are directly proportional to the level of the input signals. The second and the third order are proportional to the square and cube of the input amplitude. Thus if the three responses (1st, 2nd and 3rd order) are plotted on log-log scale, one gets straight lines with slopes in the ratio of 1:2:3. Thus if the "intercept point" and the signal level are known, the

spurious levels can be accurately predicted. Thus if the 3rd order intercept point of an amplifier is +30 dBm, for an output signal level of 0 dBm, the 2nd and 3rd order spurious signal levels will be -30dBm and -60 dBm respectively. At Gauribidanur, for an antenna temperature of 30,000K the power contained in a 500 KHz band is

KTB = (Boltzmann constant) (antenna temperature) (Bandwidth)
=-123dBm

Thus for a gain of around 40 dB, the output power is -83 dBm. The interfering signals around 10 MHz produce 2nd order spurious inband signals. Their input level is of the order of -80 dBm. For interference-free operation, the 3rd order harmonics must be less than -123 dBm (40 dB less than true signal level). For a -80 dBm input, the first order response is -40 dBm. For the 3rd order response to be less than -120 dBm, the "intercept" should be greater than 0 dBm. In the present case, apart from achieving the intercept point by increasing the emitter current, the spurious levels were maintained way below the permitted maxima by not allowing the low-frequency high level signals to drive the base of the 1st stage amplifier. This was achieved by using a band pass matching network at the input of the amplifier. A simple technique to assess the effect of the communication band on the amplifier is to precede the amplifier with a narrow band filter around 34.5 MHz and to monitor the output power either on a spectrum analyser or a power meter. This

should be same as the output power even if the amplifier precedes the filter.

3.1.5 Circuit Diagram

The circuit diagram is shown in Fig. 3.2. Two stages of cascode amplifiers provide the necessary gain. Each stage consists of a common emitter stage feeding into a common base stage. A Three-stage coupled resonator between the two amplifier stages helps to obtain the required band shape. The impedance of the different stages of the amplifier were measured by a vector impedance meter, and were coupled with proper matching networks. High input-output isolation of the cascode, makes matching the amplifier ports to other loads very easy. The stability does not depend on the local conditions. The common emitter stage has such a low value of collector load (the input resistance of the common base stage) that the voltage gain is limited to a value which makes instability via the collector-base capacitance impossible. The base of the common base stage is effectively earthed at signal frequencies, thus avoiding instability in this stage.

The parameters of the amplifier are as shown in Fig. 3.3. In a multichannel receiver, the gain and phase response of various channels must be identical. Fig 3.3 shows a comparison of 32 amplifiers. After installation, the digital ports were terminated with 50 ohms and a calibrating source transit was observed using the existing

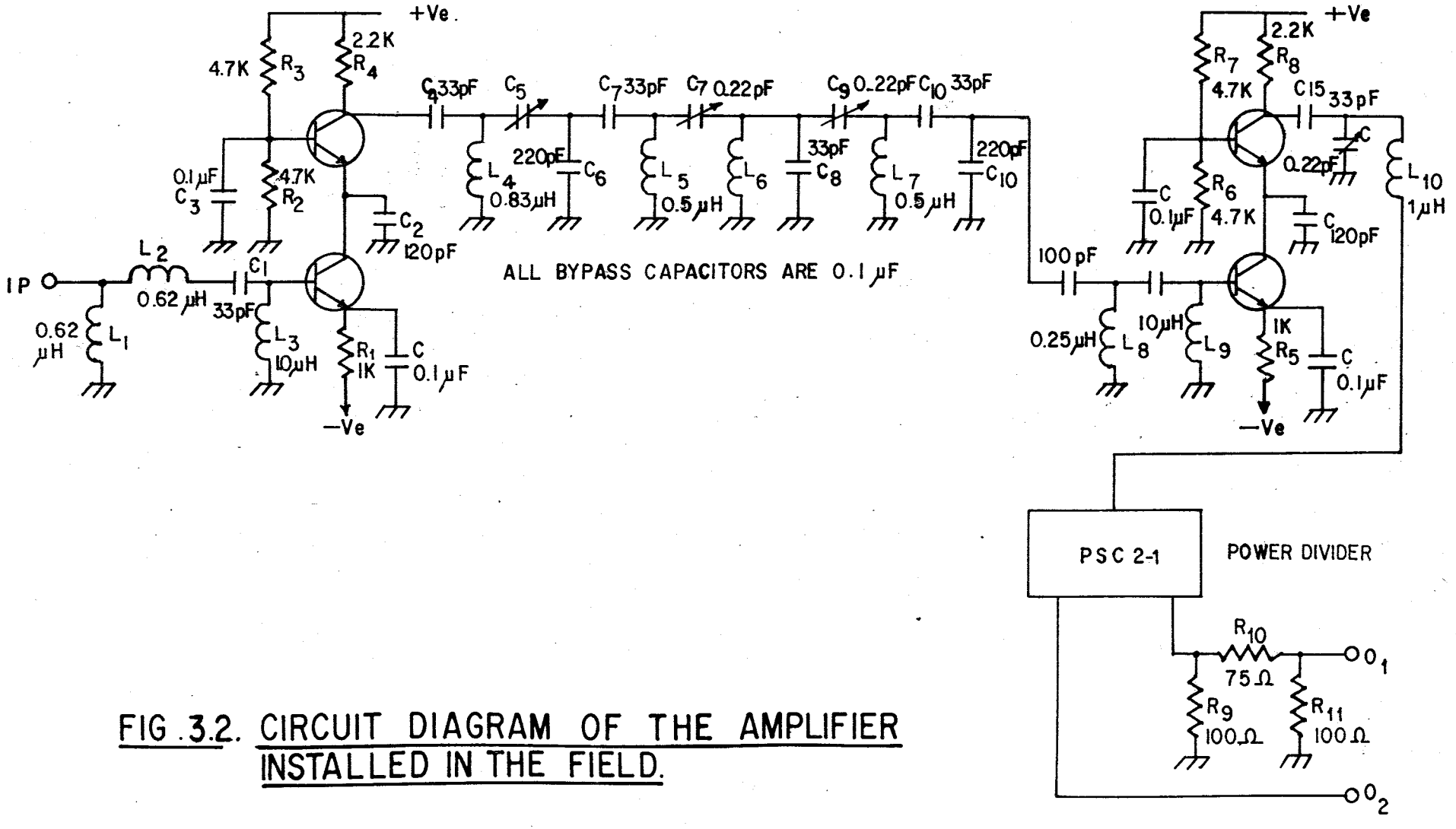


FIG .3.2. CIRCUIT DIAGRAM OF THE AMPLIFIER INSTALLED IN THE FIELD.

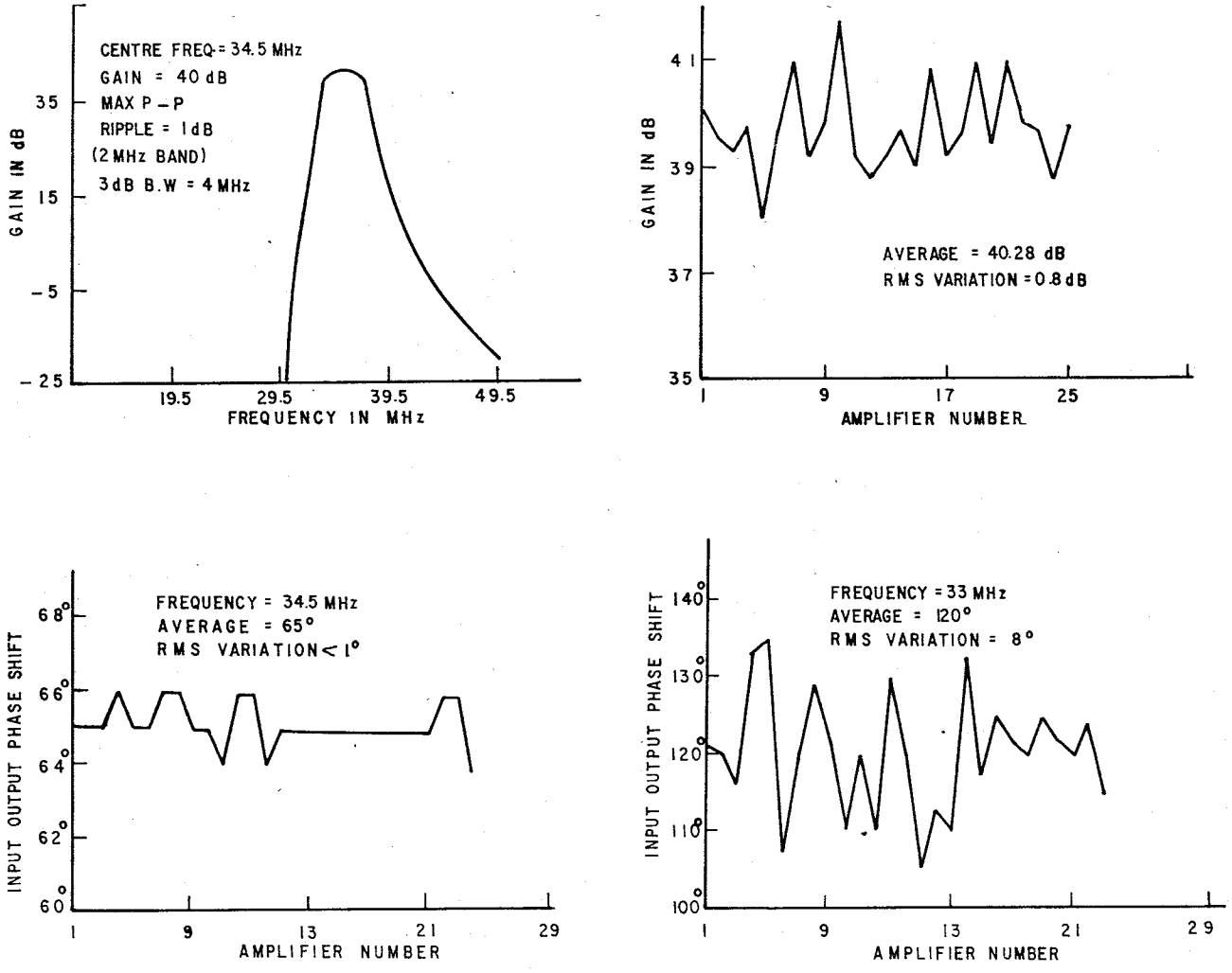


FIG 3.3 AMPLITUDE AND PHASE CHARECTERESTICS OF THE AMPLIFIERS IN THE FIELD

analog reciver. The SNR and grading were found to be satisfactory.

3.2 CRYSTAL OSCILLATOR,NOISE GENERATOR AND POWER COMBINER (FIG. 3.4)

This is an on-line test facility provided for checking the health of the system. It is very useful during installation, and in-between observations. Tests of the receiver that are often made are a) measurement of gain and phase of the superheterodyne receiver. b) testing of the correlators. This is done by injecting a continuous wave, or noise into the system. The test module is designed as an integral part of the system. Hence no additional connections need be made or removed for testing. Continuous wave or noise can be selected through a front panel switch. To select different levels of the signal, a resistive step attenuator has been provided on the front panel. The crystal oscillator frequency is 34.5 MHz. A continuous wave of any other desired frequency can be connected to the system externally. This will help in making distortion level measurements. The noise generator has a centre frequency of 34.5 MHz, and a bandwidth of around 2 MHz. Its temperature is around 10^6 K. After division by the power splitter, its temperature is very close to the temperature of the antenna as seen by the input of the superheterodyne receiver.

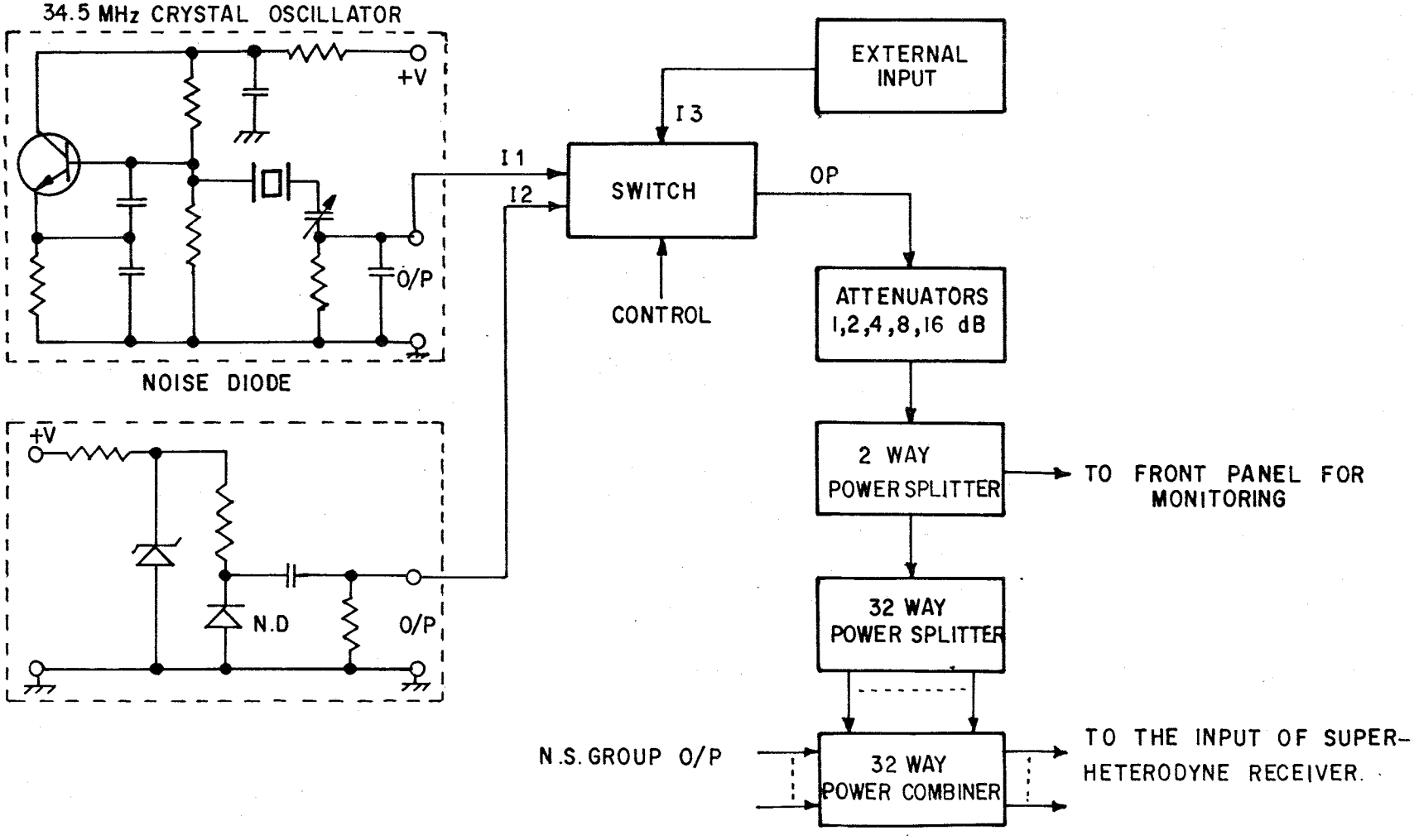


FIG. 3.4. CRYSTAL OSCILLATOR, NOISE DIODE AND POWER COMBINER.

The 23 N-S group outputs and the E-W output pass through power combiners before being fed into the superheterodyne receiver. Even though this involves a 3 dB loss, it does not deteriorate the noise figure of the system as the signals are amplified sufficiently by the field amplifiers.

The philosophy adopted in the system design was to build circuits which can be used as test equipment for the receiver. This makes the receiver system capable of generating signals required for its own testing and to indicate the state of its health. A Test Correlator, Interference monitor, Field test equipment are some of the circuits (described later in detail) which were designed to meet this goal.

3.3 SUPERHETERODYNE RECEIVER

A 32 channel superheterodyne receiver has been built. These are housed in four 7" chassis. The rear of each chassis gets the Lo signal and unregulated power supply. The LO signal is split by an 8 way power divider. Each chassis has a built in regulator. The LO and power supply are distributed to the 8 channels on a mother board.

3.3.1 Amplifier (Fig. 3.5)

Since a cascode design was already used in the field amplifiers, the same was chosen here. Its input is matched to 50 Ohms, and has a gain of around 18 dB. This along with the three stage coupled resonator gives the desired RF band shape.

3.3.2 Mixer (Fig.3.5)

A Wideband Balanced Modulator MC 1596 is used for heterodyning (Hejhall, 1974). An active mixer was preferred to a passive one for the following reasons.

1. Gain can be built into an active mixer stage while passive mixers have a typical Insertion Loss of around 6 dB.

2. Active mixers can operate at very low carrier levels (Typ -7dBm). Passive mixers require very high LO levels (Typ +7 dBm). In a multichannel superheterodyne receiver this is a serious disadvantage as the LO system will need a very high wattage amplifier to feed all the channels.

Passive mixers can operate without a power supply whereas active mixers need an external power supply. However, this is not a serious disadvantage in the present system where the mixing is done in the receiver room.

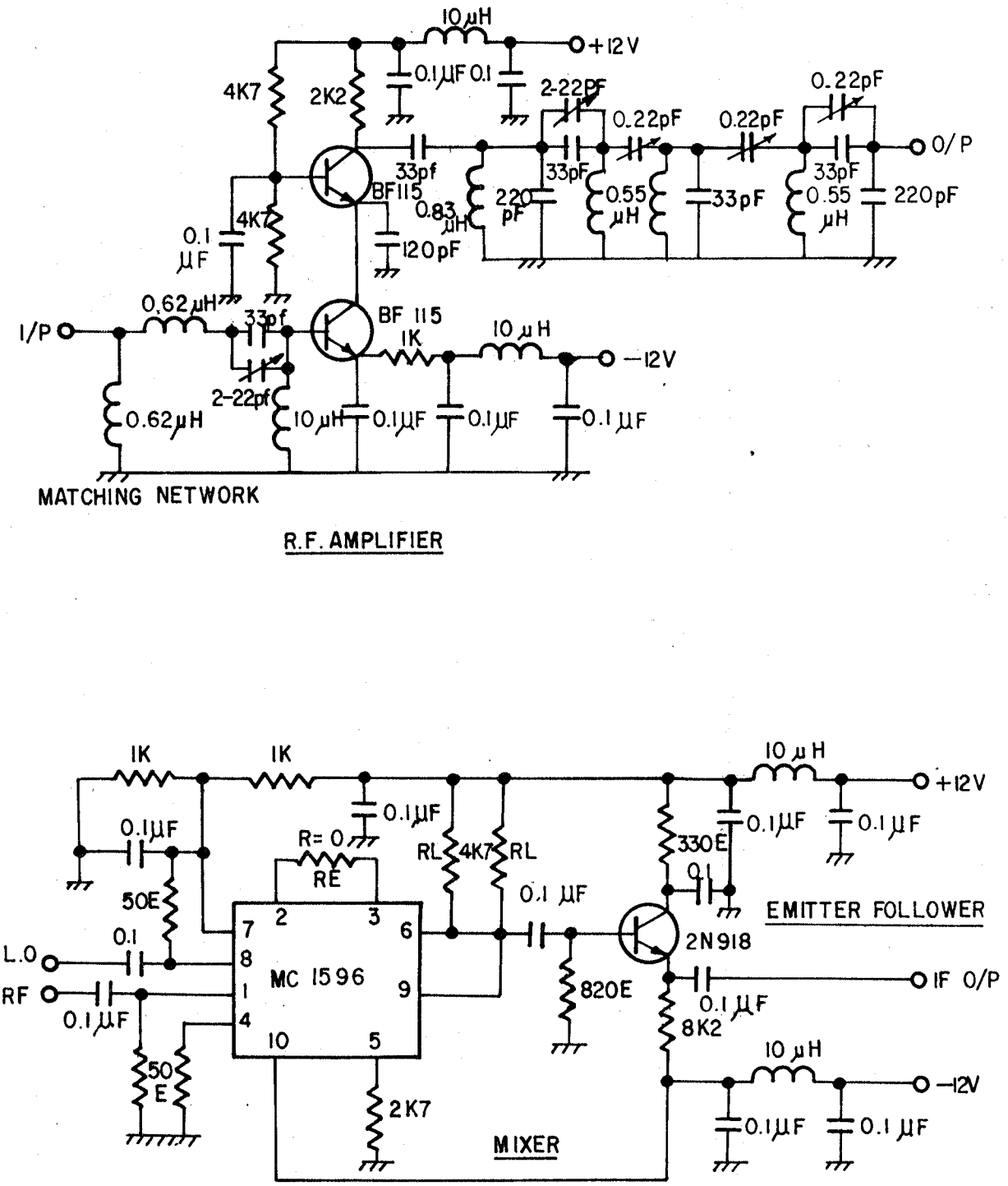


FIG.3.5 SUPERHETERODYNE RECEIVER-R.F STAGE & MIXER.

Some of the important design features of MC 1596 mixer stage are:

1. The mixer is biased for low level operation at both the carrier and modulating inputs. For low-level operation, the output signal will contain the sum and difference frequency components of the inputs. For high level carrier operation, along with the sum and difference frequency components, fundamental and odd harmonics of the carrier frequency also will be present at the output, which is not desirable.

2. For low level carrier operation an amplitude Variation of the carrrier signal will change the signal power at the output (Fig 3.7). This is used as a common gain control for all the channels. Changes that occur due to small instabilities in the LO system can be ignored for a one-bit correlator.

3. Gain is a function of load. The 50ohm load is buffered by using an emitter follower stage to increase the gain.

3.3.3 IF Filter (Fig. 3.6A)

This decides the final observing bandwidth. It is therefore essential that this stage satisfies the following characteristics.

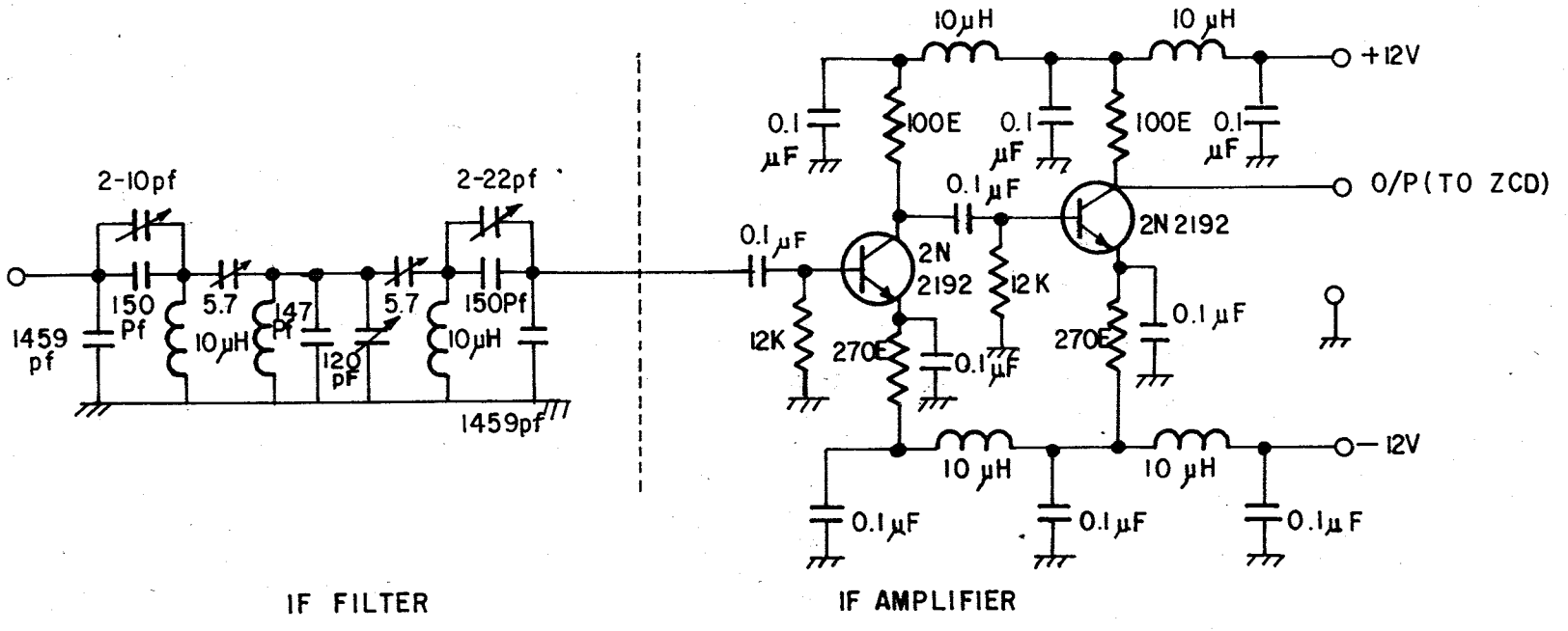
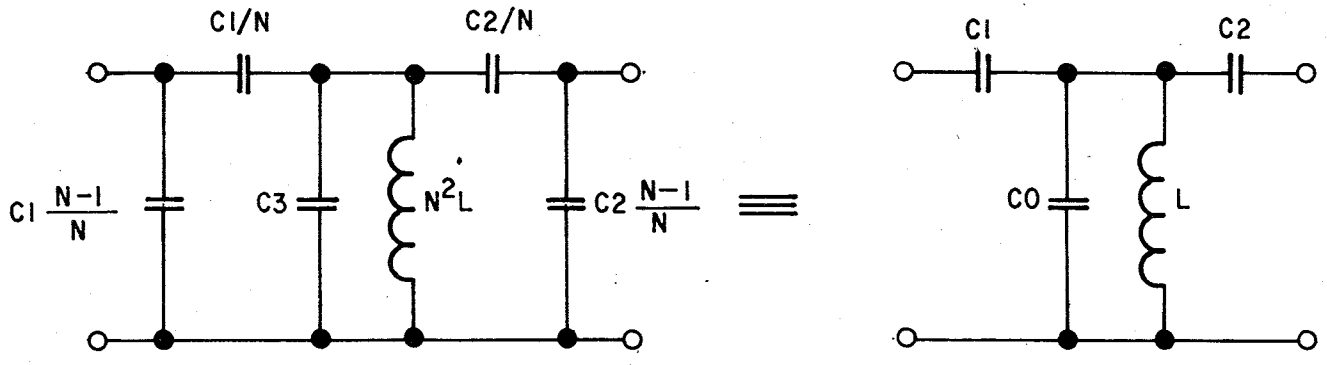


FIG.3·6A. SUPERHETERODYNE RECEIVER -I.F STAGE.

1. Band shape should be identical in all the channels. Phase response through out the band should be same in all the channels. In a one-bit correlator, variations of band shapes in different channels is equivalent to grading of the antenna. Different phase responses result in bandwidth decorrelation. This calls for a configuration for the filter whose band width and phase response are less sensitive to component variation.

2. The stopband should not have ripple. A ripple in the stop-band may pick up distant off-band strong interference.

The two requirements are more easily met by a Butterworth network than a Chebyshev or Elliptic network. But its disadvantage compared to the other two is that it has a slow roll off from pass band to the stop-band. This results in the need to use a larger number of stages. The present system uses a five stage filter. The main difficulty encountered in the design was that the values of inductance required were so low that the 'Q' obtainable with the coils were very small. This increases the insertion loss. This difficulty was overcome by an impedance transformation shown in Fig. 3.6B. This transformation increases the number of capacitors in the circuit. This is not a serious disadvantage since good quality capacitors are easily available. Inductors have to be wound and measured before they can be used in the circuit.



$$C_3 = \frac{C_0 - (N-1)(C_1 + C_2)}{N^2}$$

FIG. 3.6B IMPEDENCE TRANSFORMATION NETWORK.

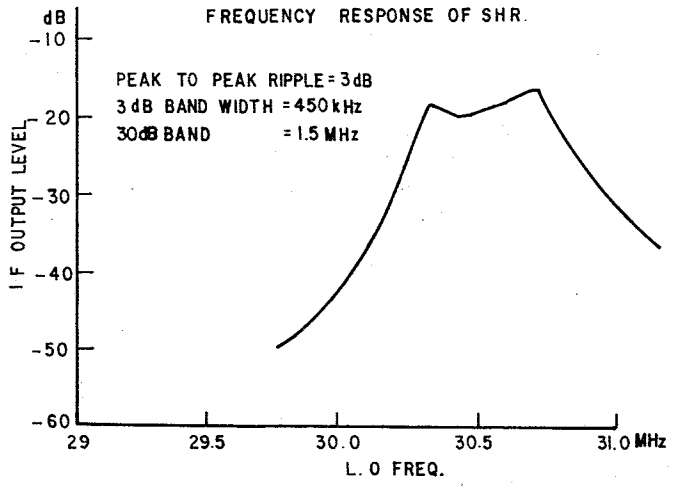
3.3.4 I.F. Amplifier (Fig. 3.6A)

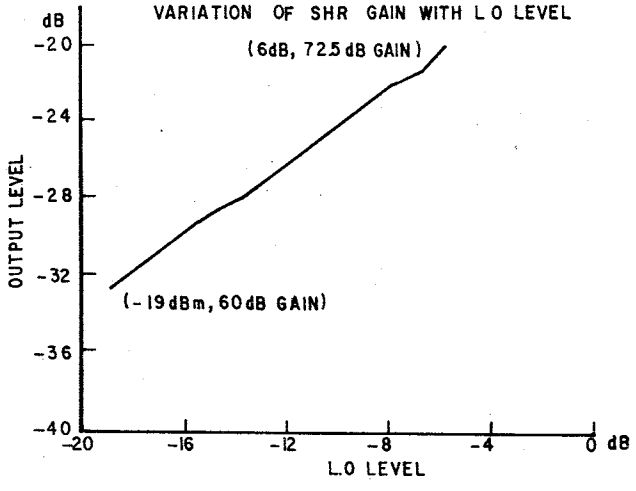
A common emitter amplifier is used in the last stage. This has a high gain and large signal handling capability. It is designed for equal saturation voltages for positive and negative inputs. If this is neglected, the final capacitor which removes the D.C. distorts the zero crossings of the input signal. But a balance which does not affect the zero crossings of the input signal is very difficult to obtain. So even this stage is operated in a linear mode.

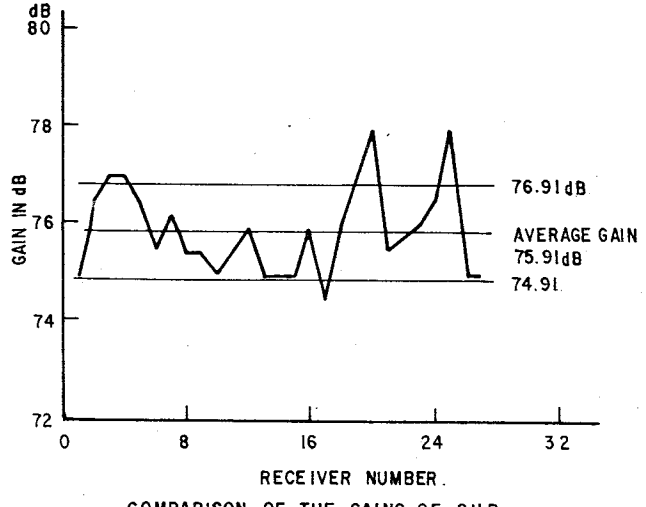
The IF band shape, the variation of the gain of the superheterodyne receiver (SHR) as a function of LO level, and the gains of the 32 channels are shown in Fig. 3.7.

3.4 VARIABLE BANDWIDTH RECEIVER

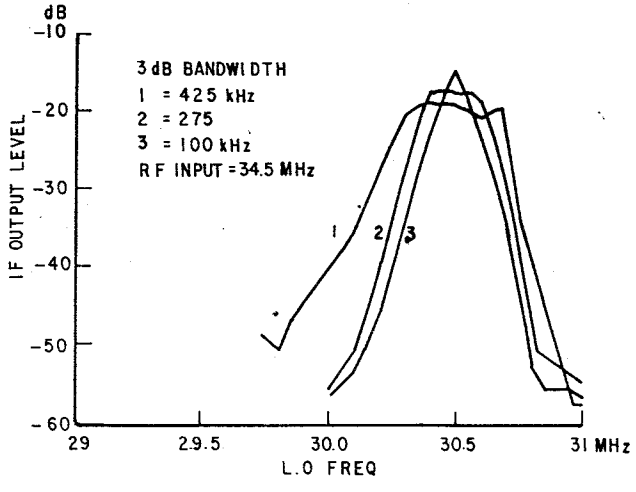
The signals from the East and West arms are brought separately to the Lab. After amplification they are combined and later split by a four way splitter. The splitter outputs are fed into the Analog Receiver, the Digital Multibeam Receiver, and the Solar Receiver. In the digital receiver, it passes through a heterodyne system which is exactly the same as described in the previous section. After heterodyning, the IF passes through a set of diode switches and filters of various bandwidths.







COMPARISON OF THE GAINS OF SHR.



FREQ RESPONSE OF VARIABLE B.W REC.

FIG. 3.7

1. The filters are meant to restrict the bandwidth of the receiver. The E-W output is multiplied with different N-S groups. Thus it is enough to restrict the bandwidth of one of the inputs to alter the bandwidth of the observation. If B_1 and B_2 are the two input bandwidths, the resultant bandwidth after multiplication is

$$B = \sqrt{B_i\ B_2} \qquad (3.1)$$

2. Capacitatively coupled resonators are used for filters. They are linear phase filters, and an equivalent phase gradient in the N-S can be easily introduced by a delay. In one-bit correlators, this can be easily obtained by shift registers.

3. The Diode switches used have a minimum isolation of 40 dB (Lacasse, 1980). A front panel Rotary Switch is used to control the diode switches and enables the selection of the bandwidth for observation. Fig. 3.8 gives the circuit details of the filters and diode switches. Fig. 3.7 shows the band widths of different filters.

3.5 LOCAL OSCILLATOR SYSTEM (FIG. 3.9)

1. This uses an advanced 4 and 3/4 digit modular synthesizer (Syntest make Model No. SM 105), which is commercially available.It is a low cost synthesizer and its use avoids the need for building one. It can provide 2 MHz to 32 MHz TTL signals with 500 Hz resolution into a 50 ohm load. Its frequency is digitally selectable by BCD-TTL

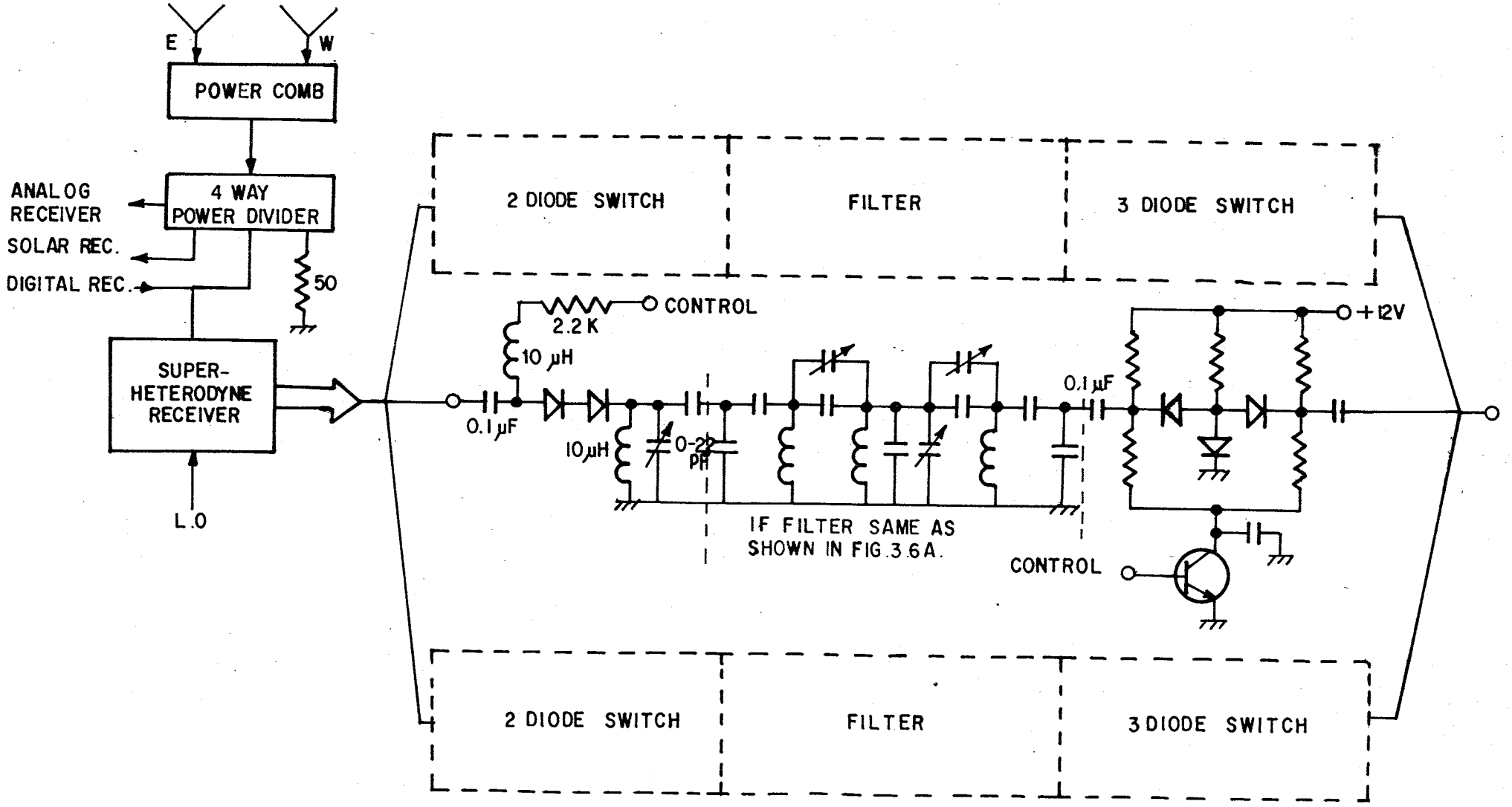


FIG. 3·8 VARIABLE BANDWIDTH RECEIVER FOR THE E-W ARRAY.

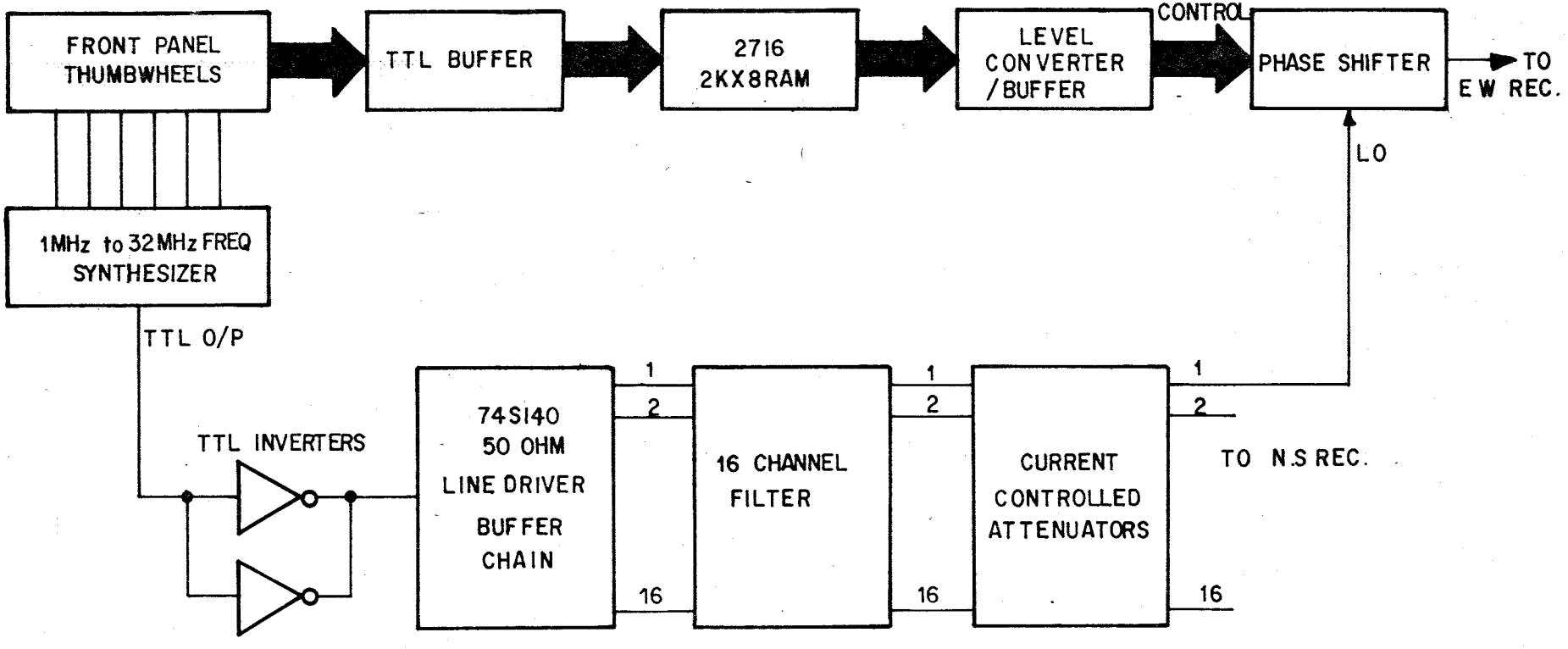


FIG. 3·9. LOCAL OSCILLATOR SYSTEM.

lines. It employs a high stability 1 MHz internal oscillator (10 x 10^{-6} over 0°-50° C). The spurious outputs are 60 dB below the full output. The receiver uses the synthesizer only from 29.5 to 31.5 MHz.

2. The output of the synthesizer has to be fed to the 32 channel heterodyne receiver. To allow for possible expansion at Gauribidanur to a 90 channel system, the LO is designed to be capable of feeding a 128 channel heterodyne receiver. Power splitting using conventional splitters results in power division at each stage of splitting (For 2 ports output, The output power will be 3n dB down with respect to the input). To compensate for this loss, one needs a high wattage amplifier before splitting, or a number of low wattage amplifiers after splitting. To avoid this problem, the 74S series TTL inverters are used as power dividers. Each inverter is used as a current amplifier. 16 outputs are provided by a buffer card. This uses the 74S140, inverter which is a 50 ohm line driver. The phase mismatch in this set up between various outputs is less than 8°. This is not high when compared to conventional hybrid splitters which have a 2° mismatch for 2 port division. More important than the phase mismatch is the "phase stability". This was checked by leaving the system on for a week. Phase drifts were comparable to the accuracy of the HP vector voltmeter used ($\approx 2°$).

3. After splitting, 16 filters are used for converting the TTL compatible signals to a sine wave. A three stage coupled resonator is used for this purpose. Good quality siemens pot cores ensure good phase stability of these filters. At the output, these are passed through current controlled attenuators to vary the level of the LO signal. These can be used to control the gain of any group of 8 heterodyne amplifiers. Each group of 8 amplifiers uses a PSC-8-1, an 8 way power divider on the mother board (Refer section 3.2).

4. The LO signal for the E-W passes through a phase shifter. This is to provide automatic phase correction when the centre frequency of observation is changed. The delay between the E-W signal and any of the N-S group signal is around 4μsecs. This results in a phase change of 360° for a 250 KHz frequency change. For a 10 KHz frequency change, the phase changes by 14° which is tolerable. Thus a 5 stage phase shifter with a 11°.25 resolution was used to obtain phase errors less than 6°. Between 29.5 to 31.5 MHz there are 200, 10 KHz steps. A 256 x 8 EPROM should be sufficient to store the phase shifts. As the thumbwheel settings are in BCD, this increases the memory requirement to 1 K. So a 2 K x 8 EPROM, which was readily available, was used in the circuit. The phase shift table required was obtained by feeding CW to representative dipoles in the E-W and N-S array of the antenna and measuring the phase difference as a function of frequency.

3.6 QUADRATURE SAMPLER AND 64 CLOCK PERIOD DELAY SHIFT REGISTER

A 32 channel quadrature sampler is housed in two 7.5" chassis. Clock distribution and power supply distribution are done using a mother board. The main features of this part of the receiver are (Fig.3.10)

1. The output of the superheterodyne receiver is fed as a differential input to the zero cross detector. A signetics NE 521 was chosen as the comparator for zero cross detection. Differential input facilitates the isolation of the analog and digital ground. Since the Van Vleck relation needs a true zero cross detector, Hysterysis cannot be built into the system. This increases the susceptibility of the system to oscillation. To suppress the oscillation the following precautions are taken.

i) a double sided card with a ground plane on one side is used.

ii) lead lengths of the analog input are kept very low.

iii) the power supply lines of the comparator are decoupled from other TTL ICS, and also bypassed to ground.

2. The output of the zero cross detector is sampled by using a D flip-flop. The sampling is done at 2 MHz. To obtain quadrature samples, the ZCD output is sampled by two clocks which are separated by 62.5 nanosecs. (1/4th the period of the IF frequency). Thus the flip flops must be

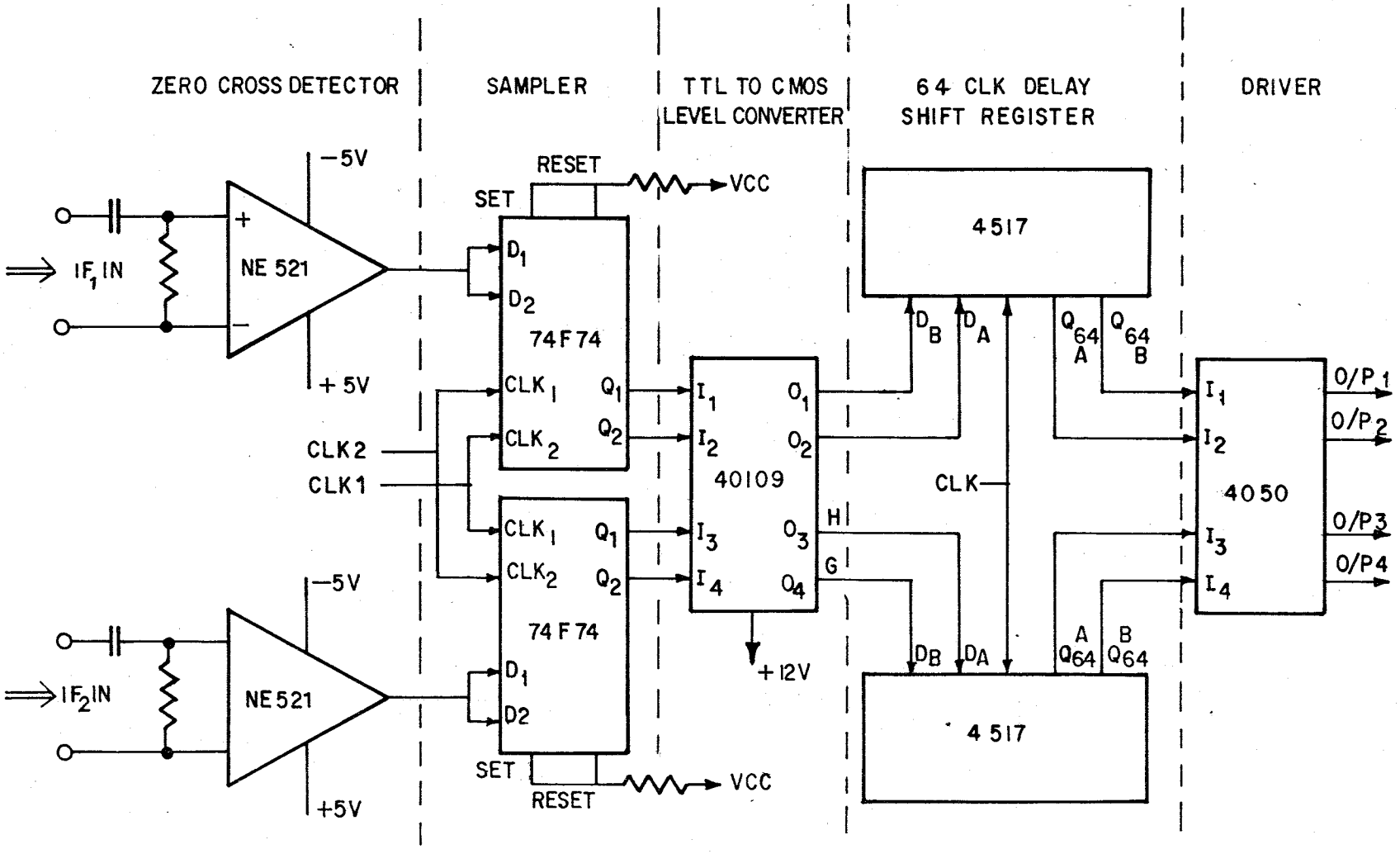


FIG. 3·10. QUADRATURE SAMPLER AND 64 CLOCK DELAY SHIFT REGISTER.

capable of sampling at 16 MHz. A TTL sampler was preferred to an ECL one because of its low cost, less noise due to edges, and better noise margin. To obtain best results, Fairchild advanced Schottky TTL samplers are used. These can toggle at typical rates of 125 MHz. Their propagation delay, set up and hold times are of the order of 2-3 nanosecs. To test the suitability of the samplers, a 500 KHz noise band centered around 4 MHz was sampled by two D flip-flops and the outputs were correlated. F series flip-flops gave only 1% decorrelation, compared to 5-6% with TTL and 3-4% with Schottky TTL flip-flops.

3.The 40109 is a TTL to CMOS level converter. The propagation delay for low to high and that for high to low changes are very different in the 40109. Thus the phase difference between the sampling clock and the 4517 clock is carefully chosen to avoid any resampling errors. The 4517 is a 64 stage shift register and introduces a gross delay of 64 clock periods before reaching the correlator input.

4. A 4050 buffer is used as a line driver in this application. Its ability to drive more than 10 feet of wire at a 2 MHz rate was ensured by testing before finalising the circuit. This ensures error free operation even if the correlator rack is some distance away.

3.6.1 Variable Delay Sampler

The N-S signal after sampling is delayed by 64 clock periods. This introduces a delay of 32 μsecs. when sampling is done at 2 MHz. The length of cable in the E-W arm delays its signal by 4 μsecs. as compared to the signal from the N-S dipoles. The variable bandwidth filter introduces an additional group delay, which is a function of the bandwidth chosen. The narrowest bandwidth is 100 KHz and it introduces a group delay of around 1/bandwidth = 10 μsecs. Thus the total delay of the E-W signal is at the most 14 μsecs. Since the N-S is delayed by 32 μsecs, the E-W signal has to be delayed further. Thus the E-W signal after sampling is passed through a variable delay shift register whose delay can be programmed by two octal thumbwheels. The circuit is shown in Fig. 3.11. It employs two level multiplexing. In the first stage, the signal can be delayed from 0 to 63 clock cycles in steps of 8 clock periods. In the second stage, delays from 0-7 clock cycles in steps of 1 clock cycle can be given to the signal. The E-W signal delayed by 64 clock periods is also made available at the back panel connector for receiver tests in the lab.

3.7 QUADRATURE CLOCK GENERATOR

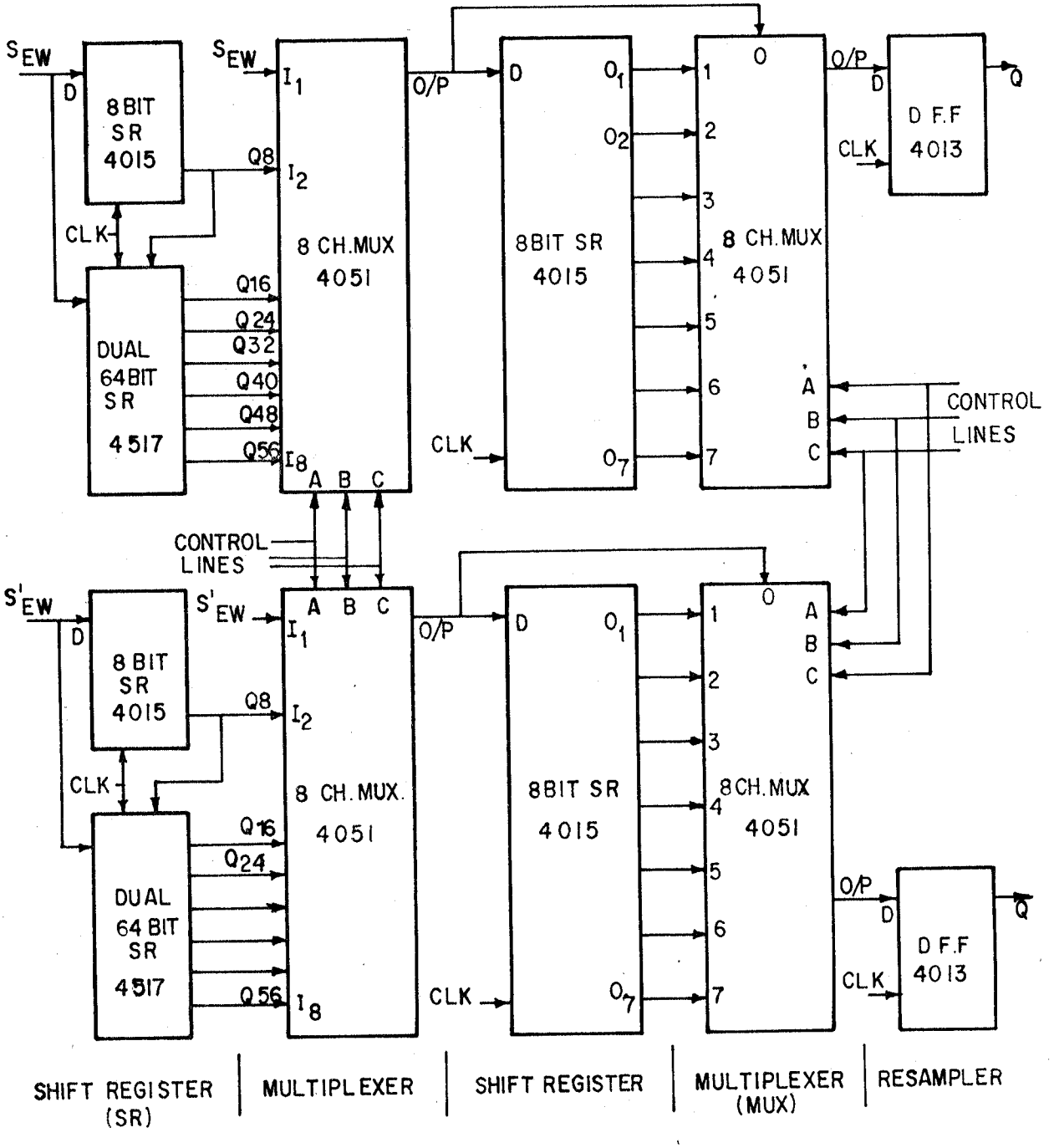


FIG. 3·11. VARIABLE DELAY SHIFT REGISTER.

3.7.1 Multiplier

Two clock trains which are separated in time by 62.5 nano secs are required for sampling. Thus a 16 MHz clock is divided to obtain the sampling frequency. This is obtained by multiplying the 1 MHz output of a crystal oscillator. The Crystal oscillator circuit and multiplier using a Motorola Phase Sensitive Detector are shown in Fig. 3.12. The 4024 is a voltage controlled multivibrator which produces TTL compatible logic levels. The maximum operating frequency of this device is 30 MHz. Frequency control is accomplished through a voltage variable current source which controls the slew rate of a single capacitor. The output frequency can be varied over a range of 3.5 to 1 of the free running frequency of the multivibrator. This requires a DC control voltage of 1 to 5 volts. As the present requirement is for a fixed 16 MHz oscillator, the Voltage Controlled Multivibrator (VCM) is set for a free running frequency of around 16 MHz. It is divided in a binary counter by 16 to generate a frequency near 1 MHz. This along with the 1 MHz reference are fed into the input of 4044 which has a phase frequency detector. If V input is lower in frequency or lags in phase, U, output goes low. Conversely, D output goes low when V input is higher in frequency or leads the R input. Duty cycles of the two inputs are not important since negative transitions control the system operation. The charge pump accepts the phase detector outputs and converts them to fixed amplitude positive and negative

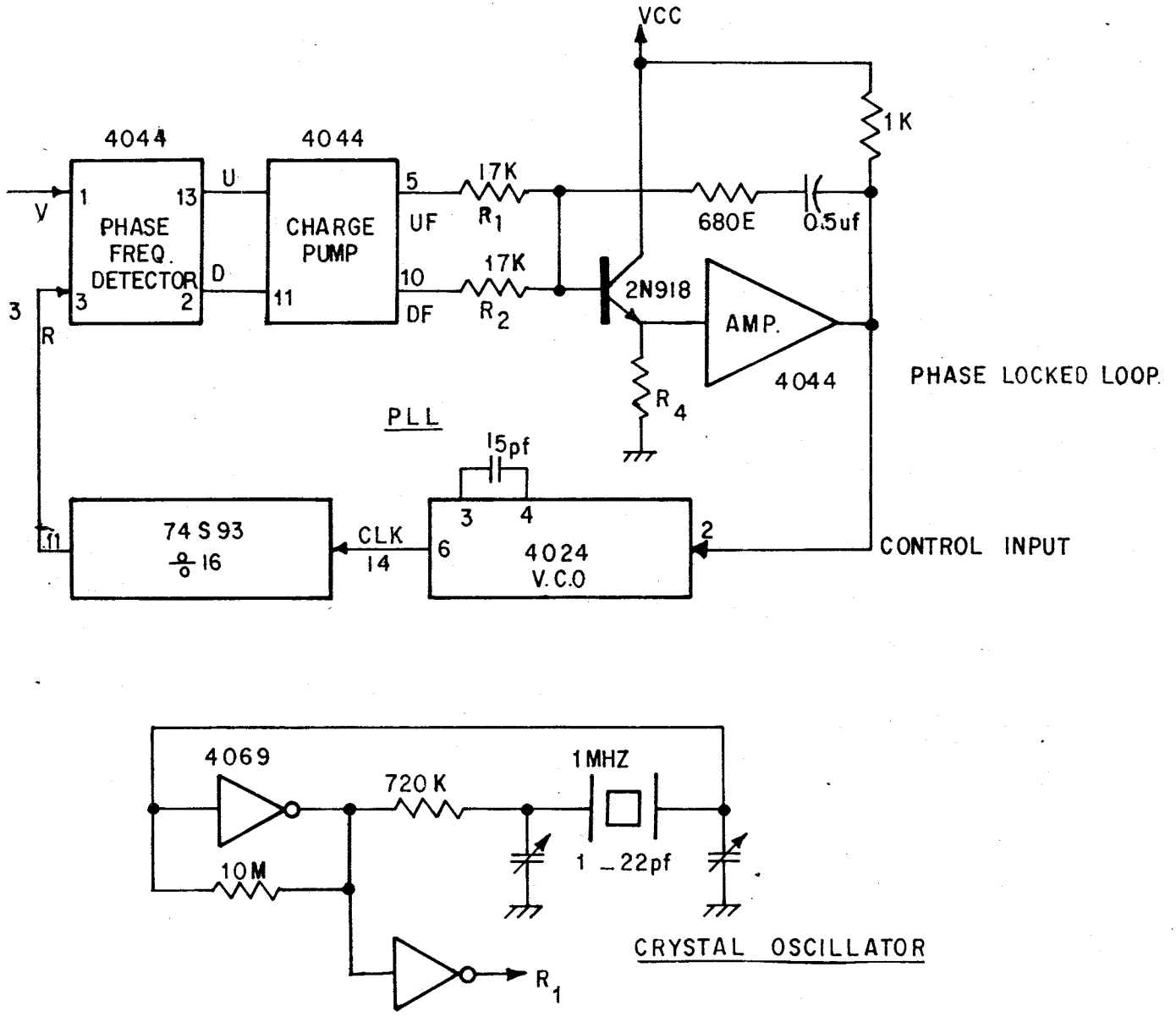


FIG. 3·12. 1 x 16 MULTIPLIER.

pulses at the UF and DF outputs. These are applied to an active filter which incorporates external components as well as the amplifier provided in the 4044. The filter has two poles and satisfies the requirements of a type 2 PLL. The filter was designed for a damping ratio ξ = 0.5 and for a peak overshoot less than 20% (Garth Nash).

3.7.2 Divider And Multiplexer

The 16 MHz is divided by two in a "D" flip-flop to obtain an 8 MHz square wave and the outputs of the D flip-flop are used to drive two sets of binary counters. The outputs of these binary counters will be staggered by 62.5 nanosecs. It is required that the two counter outputs retain the same phase relationship after every power on and any false triggering. This is achieved by electronically locking the two counters. A master reset pulse is generated by anding the clock and the Terminal Count (TC) output of one of the counters (Fig. 3.13). The counters are wired for down-counting and the TC output remains high as long as the counter output is zero. Two multiplexers with common control lines are used to select a sampling frequency. The Sampling frequencies that can be chosen are 0.5, 1,2, and 4 MHz. The maximum sampling frequency at which CMOS correlators can function comfortably is 2 MHz. The phased clocks required for a double sideband correlator are also generated here. To obtain trouble free operation without resampling errors, they are generated by a clock 4 times the

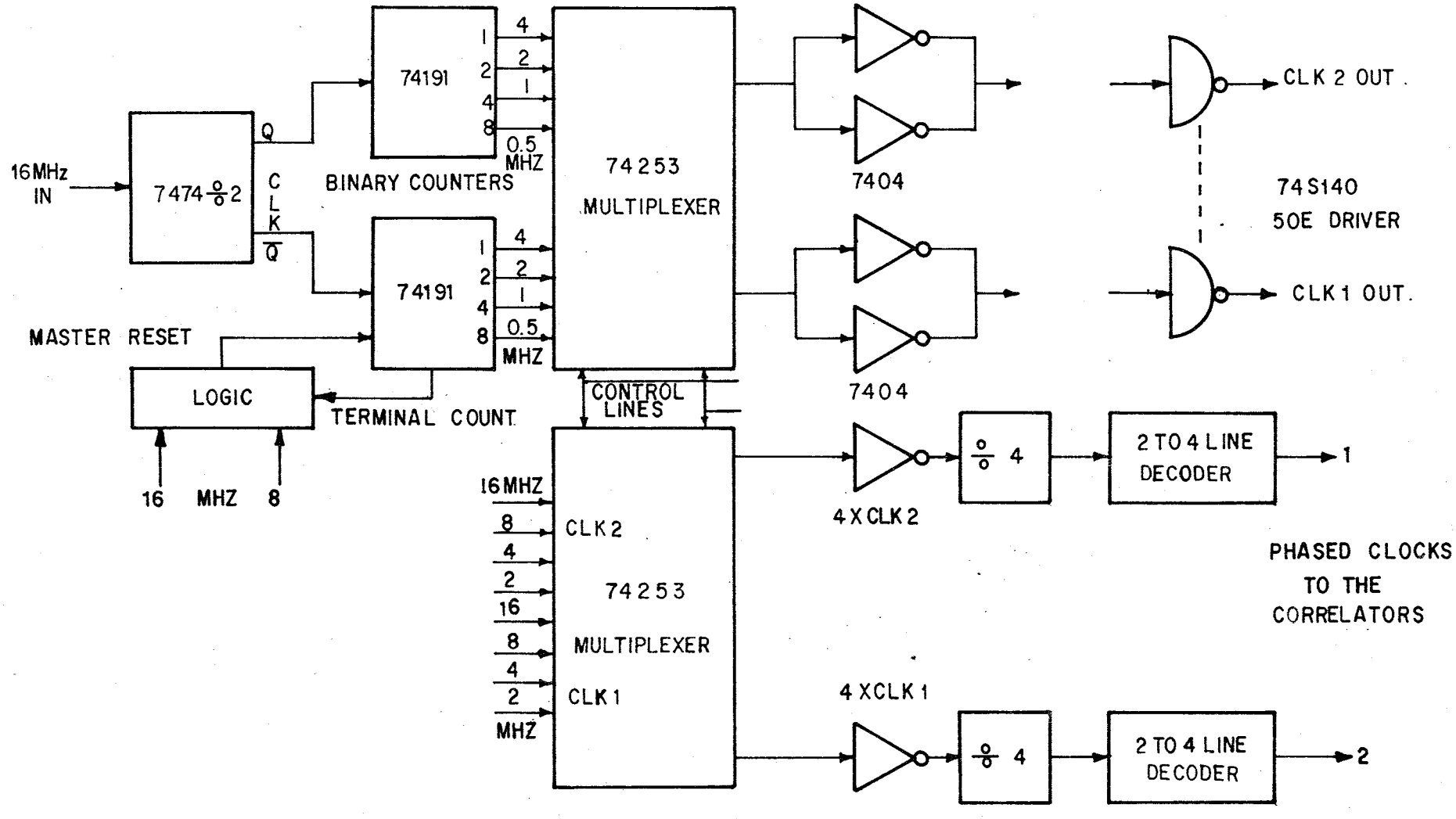


FIG. 3·13 QUADRATURE CLOCK GENERATOR.

sampling frequency.

3.8 ONE-BIT CORRELATOR (FIG. 3.14)

The quadrature samples of the E-W signal (S_E, S'_E) and different N-S group outputs (S_N, S'_N) are passed through a 4 stage shift register. A two bit code and a multiplexer permit delay compensation of the signal from the E-W or N-S array depending on the zenith angle of observation and the interferometer spacing. For cosine correlation, the signals are multiplied in exclusive Nor gates which measure the coincidence between its inputs. The sine correlation requires $\overline{S_E \; S'_N} \; \overline{-S'_E \; S_N} \cdot \overline{-S'_E \; S_N}$ is obtained by using exclusive OR gates whose output when clocked measures anticoincidence counts. Addition is performed by using two phase clock and upcounters. The input to the upcounter will be at a rate twice the sampling rate. This method of adding is very simple and inexpensive.

Adding before Van Vleck correction (which is non linear) is permissible because of the equality of the terms added (Sec 2.4).

$$2 \sin\left[\left(\tfrac{\pi}{2}\rho_{c_1} + \tfrac{\pi}{2}\rho_{c_2}\right)/2\right] = \sin\left(\tfrac{\pi}{2}\rho_{c_1}\right) + \sin\left(\tfrac{\pi}{2}\rho_{c_2}\right) \quad (3.2)$$

when $\rho_{c_1} = \rho_{c_2}$

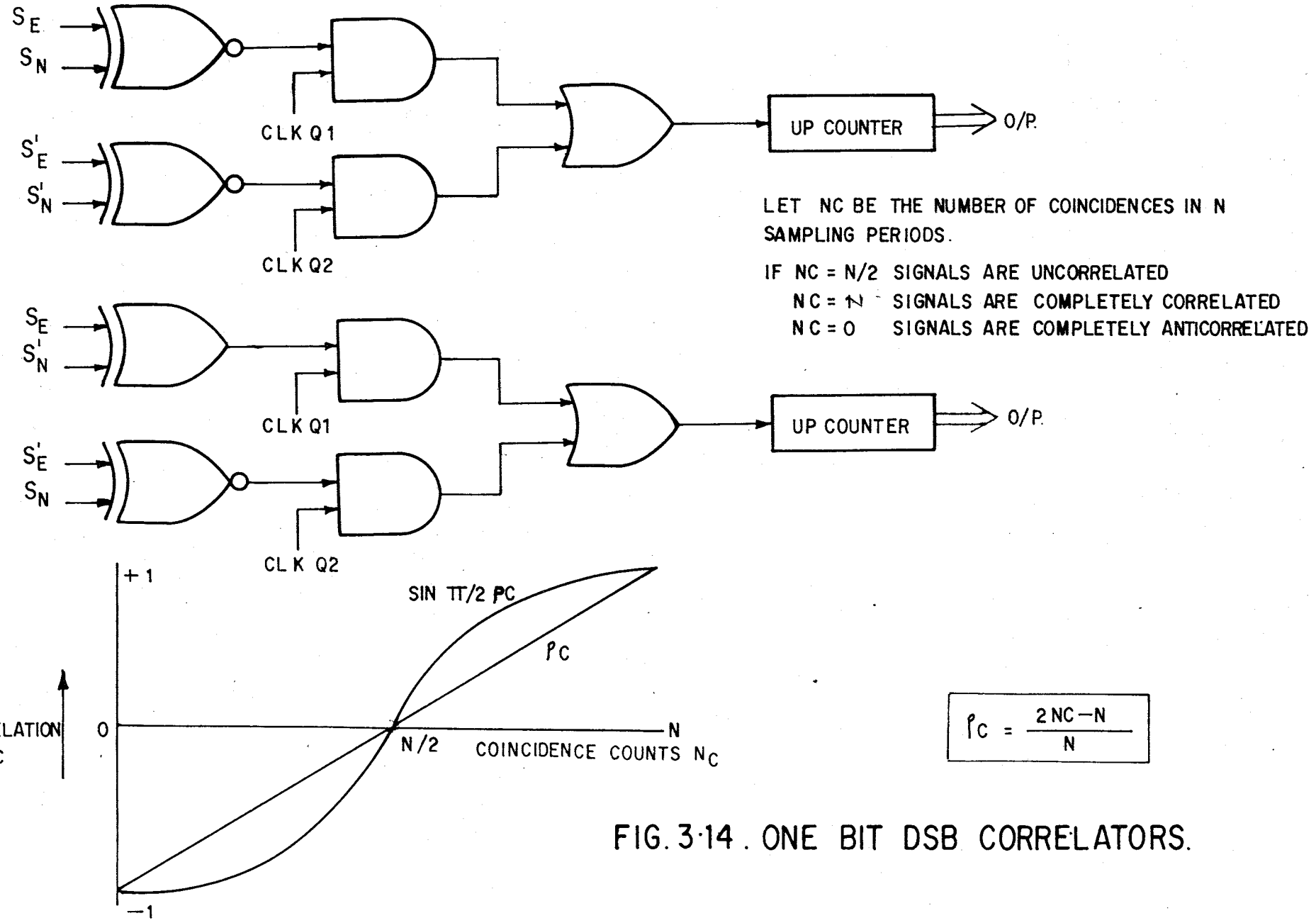


FIG. 3·14. ONE BIT DSB CORRELATORS.

For unity correlation a 4 MHz clock rate can fill a 20 bit counter in 256 msecs. (normally the rate for the counter inputs and integration time used for observation). To vary the integration time from 2 msecs to 256 msecs, the length of the counter should be variable from 13 to 20 stages. Fig. 3.15 gives the schematic for data integration and multiplexing. Independent of the integration time, only the 8 most significant bits of the counter are latched and recorded after each integration. To avoid loss of information, only these 8 bits are reset after each integration. The lower order bits of the counter are allowed to accumulate correlation for the next integration period without being reset.

All the 128 channel correlators are useful for the line observation. For continuum observations only 32 correlators are used.

3.9 ASTRONOMICAL CLOCK

Accurate sidereal time information is essential in astronomical observations. The astronomical clock described here was not built exclusively for the receiver system at Gauribidanur but as a general purpose instrument for any observatory (Udaya Shankar, 1981).

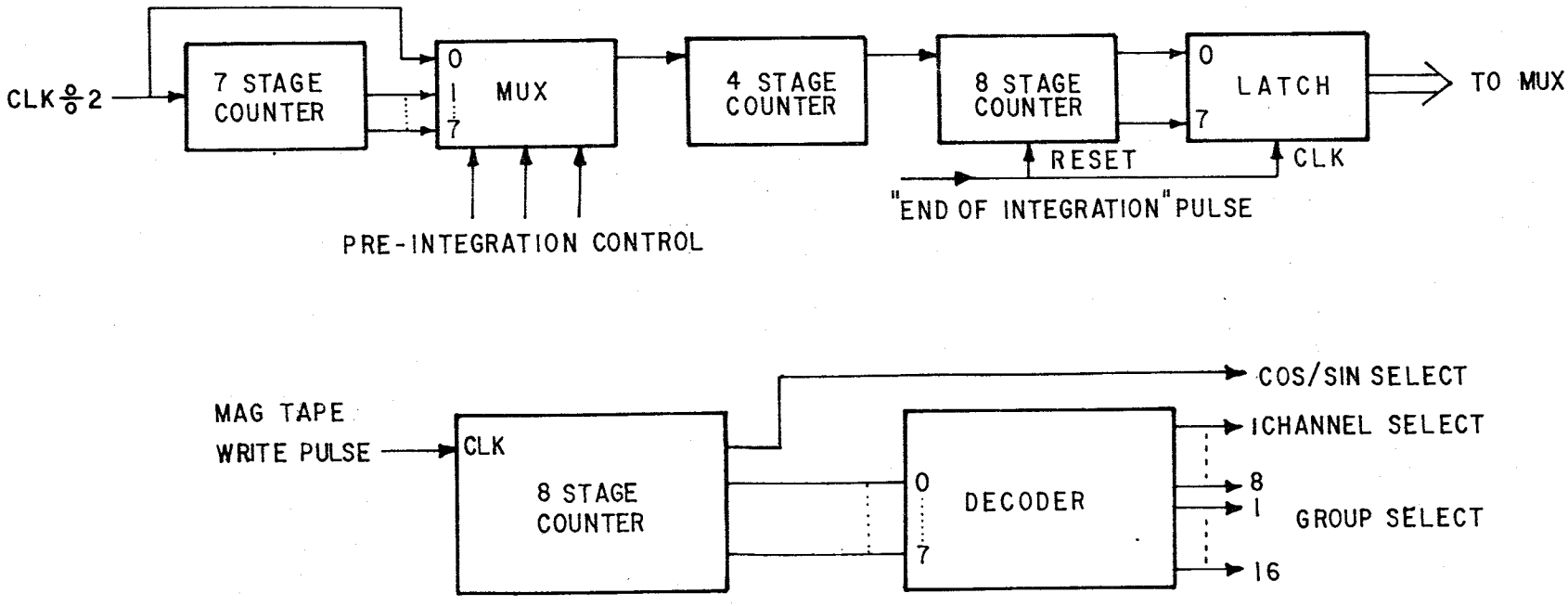


FIG. 3.15 DATA INTEGRATION AND MULTIPLEXING UNIT

3.9.1 Principle Of Operation

The sidereal second is a certain fraction (0.99726956) of a solar second and it is quite easy to build a clock based on appropriate frequency division from a crystal oscillator. However, it will be difficult to periodically correct the clock for accumulated errors, since accurate sidereal time signals are not readily available. If solar and sidereal times are generated from the same basic oscillator, a distinct advantage is obtained. When solar time is corrected against a standard time signal, the sidereal time will also be automatically corrected, as long as the "gear-ratio" between the two clocks is accurate, and the two are never de-coupled. There can be no cumulative error in the sidereal clock once the solar clock is updated. This approach is used in the present design. A block diagram of the clock is shown in Fig. 3.16.

3.9.2 Oscillator

The clock can be run on any stable 1 MHz source (Amplitude 0.5 to 5V P-P). The external input is made COS/MOS compatible by an amplifier. However if this input into the system fails for any reason a built in 1 MHz source takes over automatically and the clock continues to function without interruption.

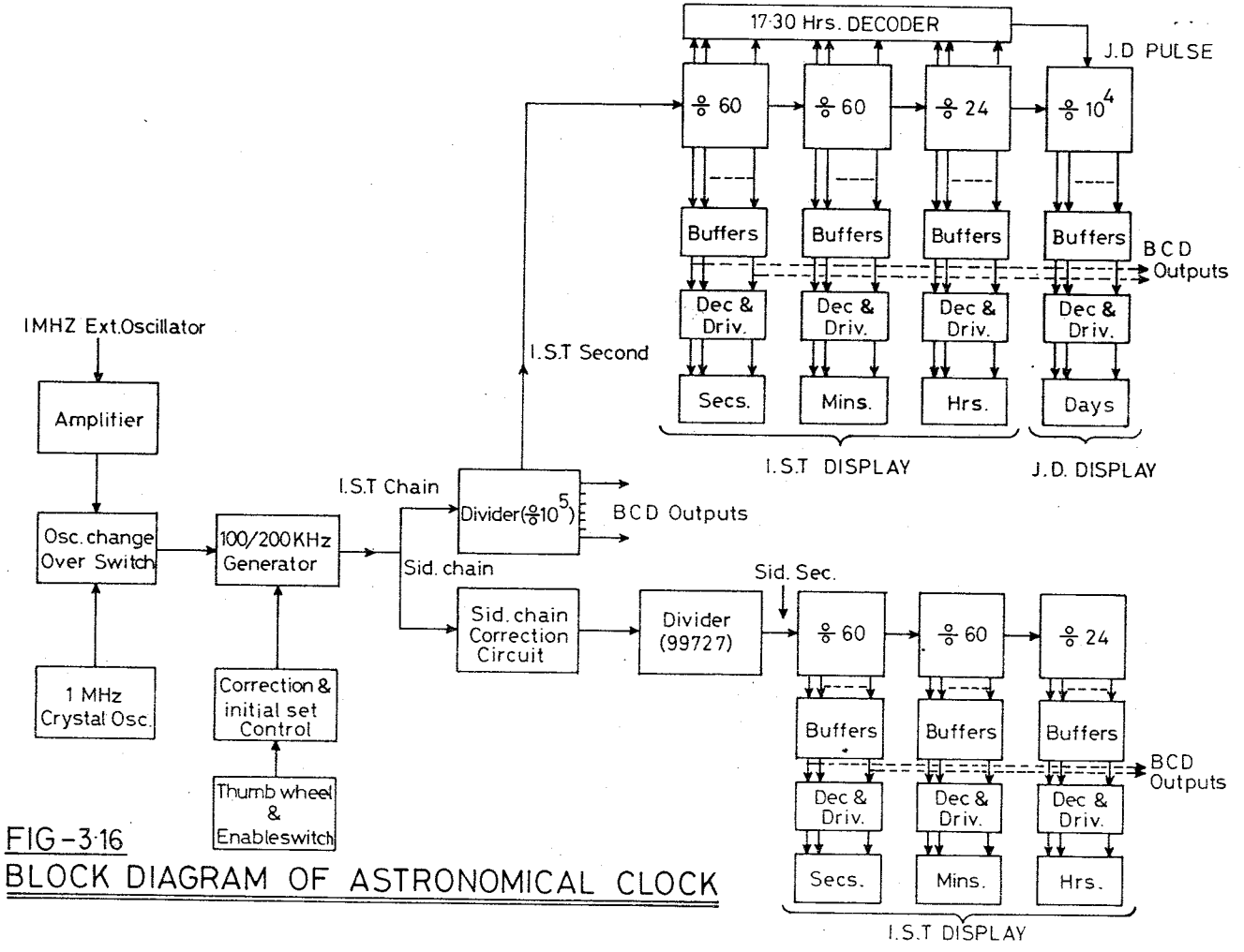


FIG-3·16

BLOCK DIAGRAM OF ASTRONOMICAL CLOCK

3.9.3 Initial Setting And Correction

The 1 MHz waveform is divided by 5 to obtain 200 KHz and further by 2 to get 100 KHz. For normal running of the clock, the 100 KHz is fed to both I.S.T. and L.S.T. chains. Correction is achieved by temporarily connecting 200 KHz signal to speed-up the clock or a "0-Hz" signal to slow it down. The gating pulse of the required width is obtained by a set of presettable counters. The minimum correction that can be applied is 10 μsecs.

These presettable counters also act as burst generators and provide the required number of clock pulses when setting the clock. L.S.T. and I.S.T. can be set to integral seconds only. Once in approximately, every six minutes the I.S.T. in integral seconds will correspond to an L.S.T. also in integral seconds to an accuracy better than two msecs. It is quite straight-forward to calculate corresponding I.S.T. and L.S.T. in this manner for initial setting for a given Julian day. After setting, the clock can be corrected to be within 10 μsecs of any standard time broadcast.

3.9.4 Sidereal Chain And Julian Day

The 100 KHz signal is divided by 99727 to get sidereal seconds. To obtain an average sidereal second, a pulse is added at the input of the divider chain every 23 sidereal seconds.

In this method of generating the average sidereal second, the short-time discrepancy is less than 10 μsecs in any 23 sidereal seconds period and the error accumulated over a year is less than 40 msecs. Julian Day is incremented at 17:30:00 hrs I.S.T.

3.9.5 Leap Seconds

This arises because standard times are maintained by atomic clocks but ultimately they have to be corrected with reference to the transit of astronomical sources.

Addition or omission of a second to or from I.S.T. without affecting the sidereal time is necessary whenever a 'Leap second" is introduced in I.S.T. This is possible and is achieved by decoupling the I.S.T. and sidereal chains and feeding 200 KHz or 0 Hz respectively to the I.S.T. chain only. An inserted second is called a +ve 'Leap-second'. A -ve/+ve leap second, when required, will usually be the last second of a U.T.C. month, like 31st December and/or 30th June. A +ve leap second begins at 23 hours, 59 minutes, 60 seconds and ends at 0 hour, 0 minute, 0 second of the first day of the following month. In the case of a -ve leap second, 23 hours, 59 minutes, 58 seconds, will be followed one second later by 0 hour, 0 minute, 0 sec. of the first day of the following month.

3.9.6 Lockable Switch

A lockable switch normally disables the Leap Second circuitry. This is necessary as the introduction of a Leap Second disturbs I.S.T. to sidereal time relation. This also disables the resetting and initial setting circuitry of the clock. This ensures that only authorized persons in the observatory can reset the clock.

3.9.7 Operation During Power Failure

The clock needs three DC power supplies: +5V, +5V and +12V. One +5V power supply is meant for the buffers used to make I.S.T, L.S.T. and J.D. information TTL compatible. The other +5V is used for the displays. The critical time-keeping circuits derive their power from the +12V supply. In the event of power failure, all critical time-keeping circuits continue to operate on the internal batteries provided in the clock. Two batteries are provided to ensure uninterrupted working of the clock, even if there is a mains failure at the time when one of the batteries is removed for replacement. The clock can be made to draw power from the older of the two batteries by operating a toggle switch.

3.9.8 Computer Interface

Interfaces to transfer the time information to the computers acquiring the astronomical data on line have been designed. Similar Astronomical clocks have been interfaced to a Varian Computer at the Radio Astronomy Centre, Ooty, an LSI 11-23 computer and a PDP-11/34 both at our institute and to the magnetic tape unit controller at Gauribidanur. The interface consists of

1. Latches to strobe the time information when the computer desires to acquire time.

2. Multiplexer to provide timing information from 10-μsec to Julian day in bits parallel, bytes, serialised mode.

3.9.9 Sidereal Rate Generator

The BCD outputs of the sidereal chain (below 1 sec) is not a true representation of sidereal rate. These counters run at I.S.T. rate till the generation of the average sidereal second . This will be a serious disadvantage in telescope systems which use sidereal rate clocks to drive stepper motors, for example to control the telescope pointing. Fig. 3.17 gives the block diagram of a sidereal rate generator. The task of this circuit is to generate 10^5 pulses in the same time as 1 average sidereal second (99727 pulse intervals). Such a generator was found extremely useful for the 90" optical telescope at Kavalur.

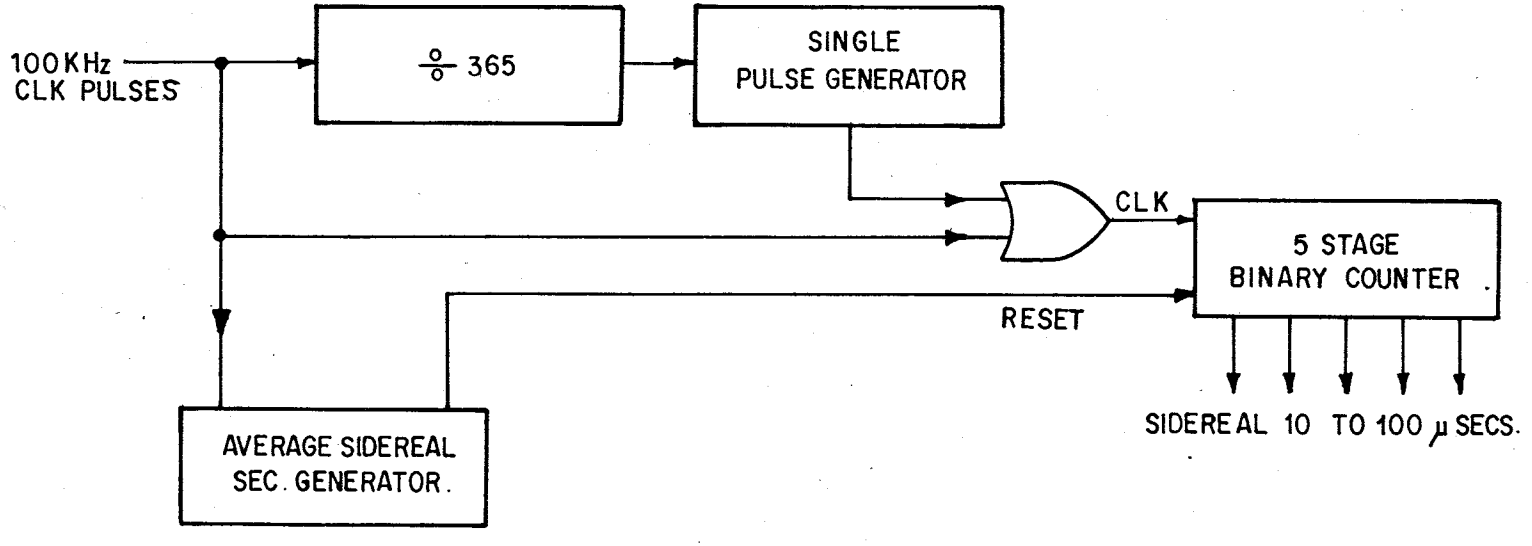


FIG.3·17. SIDEREAL RATE GENERATOR.

3.10 INCREMENTAL MAGNETIC TAPE RECORDER AND INTERFACE

The outputs of the correlators are recorded using an incremental magnetic tape unit. At the beginning of each file, time information, and at the end of each file amplifier gain and zero cross detectors threshold calibrations are recorded on the magnetic tape. There is no computer centre yet at the Gauribidanur field station. Thus start-stop tapes which requires large and costly memory were not procured. An incremental recorder was chosen for the following reasons:

1. It is an inexpensive but a reliable device.

2. It can be easily interfaced with a digital receiver system.

3. Information can be written as though it is written into a R.A.M . Data characters are evenly spaced, parity bits are internally generated and gaps of standard length are inserted on command. Information for further processing can be retrived by mounting the tape on standard computer tapedrives and read as though they were written by the computer itself.

The only disadvantage of this system of recording is the difficulty of checking the interface. A computer is required to ensure the quality of data recorded on the tape. To avoid running to a computer centre, each time a system check has to be performed, a printer and its interface are

included as a part of the receiver system.

The magnetic tape interface circuit is shown in Fig. 3.18. Some of the salient features of this interface are

1. It synchronizes the start of an observation with the start of a sidereal minute. It also immediately latches the astronomical clock output and writes a header containing sidereal time and J.D. information. After the header is written, it writes a "record gap". The Header length can be varied from 8 to 99 bytes. Details of observation if any can be loaded into a R.A.M. before the recording begins. These details along with the timing information gets written on the magnetic tape as header.

2. The circuit enables the observer to choose the following options:

a) Recording speed can be varied. Pulses of period 4 msec, 10 msec and 100 msec. which are derived from the astronomical clock are made available. It can accept external write pulses also.

b) It can generate record gaps at intervals of 10 secs, 20 secs. or 1 mt. It can also accept an external E.O.R. (end of record) pulse.

3. It automatically writes a file gap at the end of every hour. It goes through the following sequence of operations

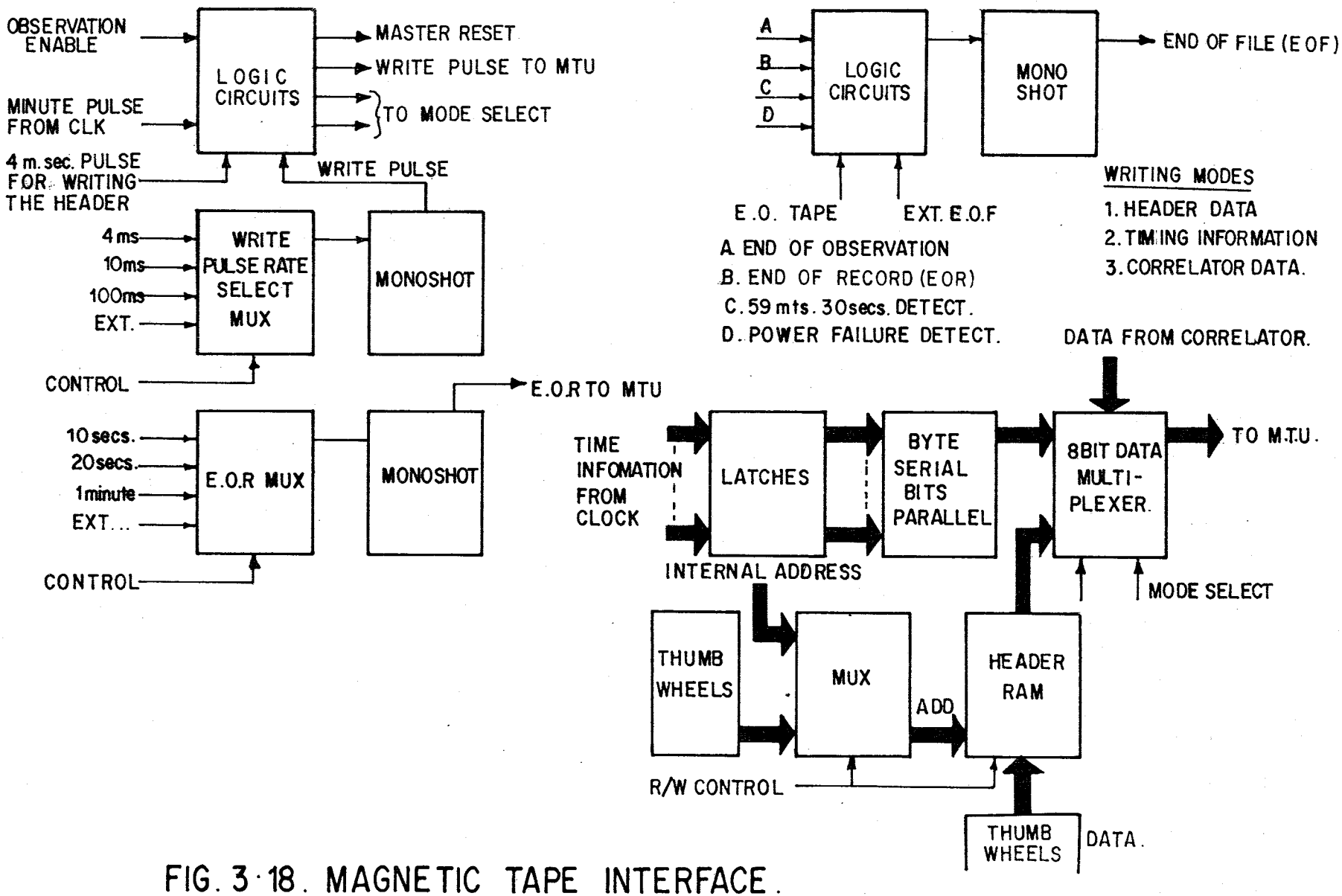


FIG. 3·18. MAGNETIC TAPE INTERFACE.

a) After 59 Mts and 30 secs of each hour it waits for a record gap.

b) After a record gap has been written it automatically switches on the noise diodes in the field (Ref figs 2.21 and 2.22). It writes one record containing information about the gain of the amplifiers and the thresholds of the comparators.

c) After calibration is recorded, it writes a record gap followed by a file gap.

d) Recording commences automatically after the next end of minute/hour with the acquisition of time.

4. If there is a mains power failure, the astronomical clock, M.T.U. and its interface automatically switch over to a battery supply. A record gap and a file gap are immediately written. When the mains power returns, recording is enabled at the end of the next minute.

5. Gap in process, write error, beginning and end of tape are indicated on the front panel by a set of L.E.D's.

3.11 FIELD TEST EQUIPMENT (F.T.E)

Before one embarks on a long stretch of observation, antenna testing is essential. In particular, the E-W grading has to be made perfect before one dimensional synthesis is done in the N-S direction. At Gauribidanur the E-W antenna is 1.5 km long. To check the antenna, one needs

a signal generator, noise diode, vector voltmeter and a counter. To power these instruments one needs batteries and an inverter . The low efficiency of the inverters increases the power consumption. The number of instruments mentioned is almost one jeep load and are also expensive instruments to be carried around often in a jeep. A simple inexpensive instrument which can replace all the above mentioned units has been designed. This can directly operate on batteries and reduces the power consumption. It can also work on A/C - power wherever it is available.

3.11.1 Signal And Noise Generators (Fig. 3.19)

A single frequency sinewave is enough to test the amplifiers and phase shifters in the field. To test the average gain and phase characteristics over the entire band, a Noise Generator can be used. The Signal Generator part of F.T.E. consists of a 34.5 MHz crystal oscillator and a Noise Generator. A front panel switch enables the user to select continuous wave or noise for antenna measurement. The fixed attenuators with diode switches permits the user to choose the signal strength (-10,-20,-30 dBm). An amplifier (Motoral a make MHW 590) can be switched on for additional gain (+30 dBm). A variable attenuator permits alteration of the signal level in 1 dB steps.

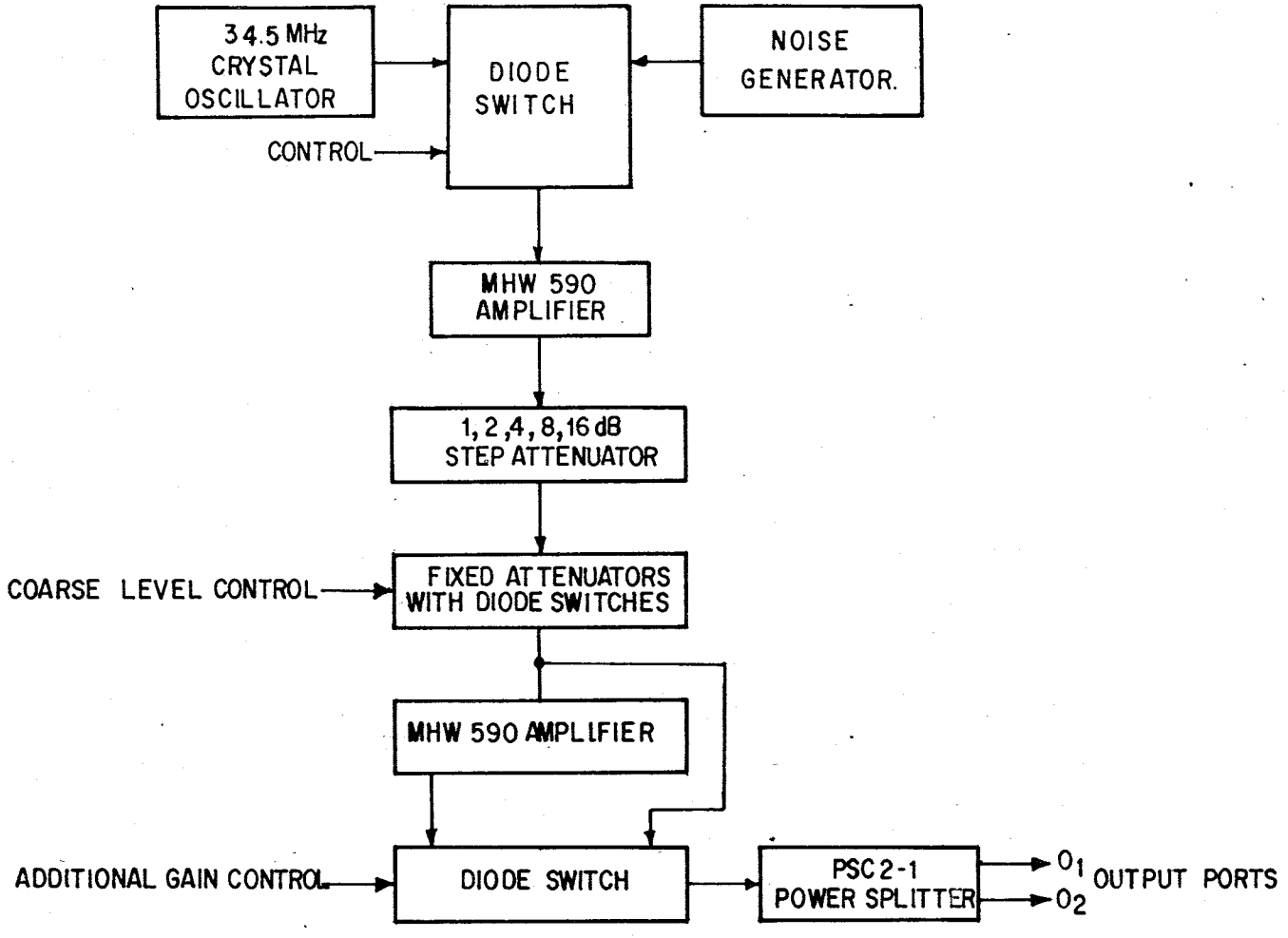


FIG. 3·19. FIELD TEST EQUIPMENT - SIGNAL AND NOISE GENERATOR.

3.11.2 Superheterodyne Receiver (Fig. 3.20)

The outputs of the devices under test (Antenna, Amplifier, Phase shifter, cables), or a reference signal and the output of a device under test, can be fed to the instrument through front panel BNC connectors. They are heterodyned to 4 MHz for amplitude and phase measurement. One of the heterodyne receivers has a phase shifter in the path of the L.O. This permits introduction of a differential phase shift between the channels. This part of the unit also has a 2 MHz Crystal Oscillator circuit. This TTL/CMOS compatible clock is used for sampling.

3.11.3 Amplitude Measurement

The signal is brought to 0 dBm level by adjusting the variable attenuator. It is fed to a detector, and after integration it is fed to a window detector. $VREF_1$ and $VREF_2$ are apriori obtained by feeding +.5 dBm, -.5 dBm calibrated 4 MHz signal to the detector. A set of 3 light emitting diodes indicate whether the signal level is $\leqslant$ 0.5 dBm, $\geqslant$ -0.5 dBm or in between the two. The reading of the attenuator gives a measure of the signal level.

3.11.4 Phase Measurement (Fig. 3.21)

The signal from the signal conditioner is fed into Z.C.Ds. and multiplied using exclusive Nors. The number of coincidences between the two pulse trains is measured in a

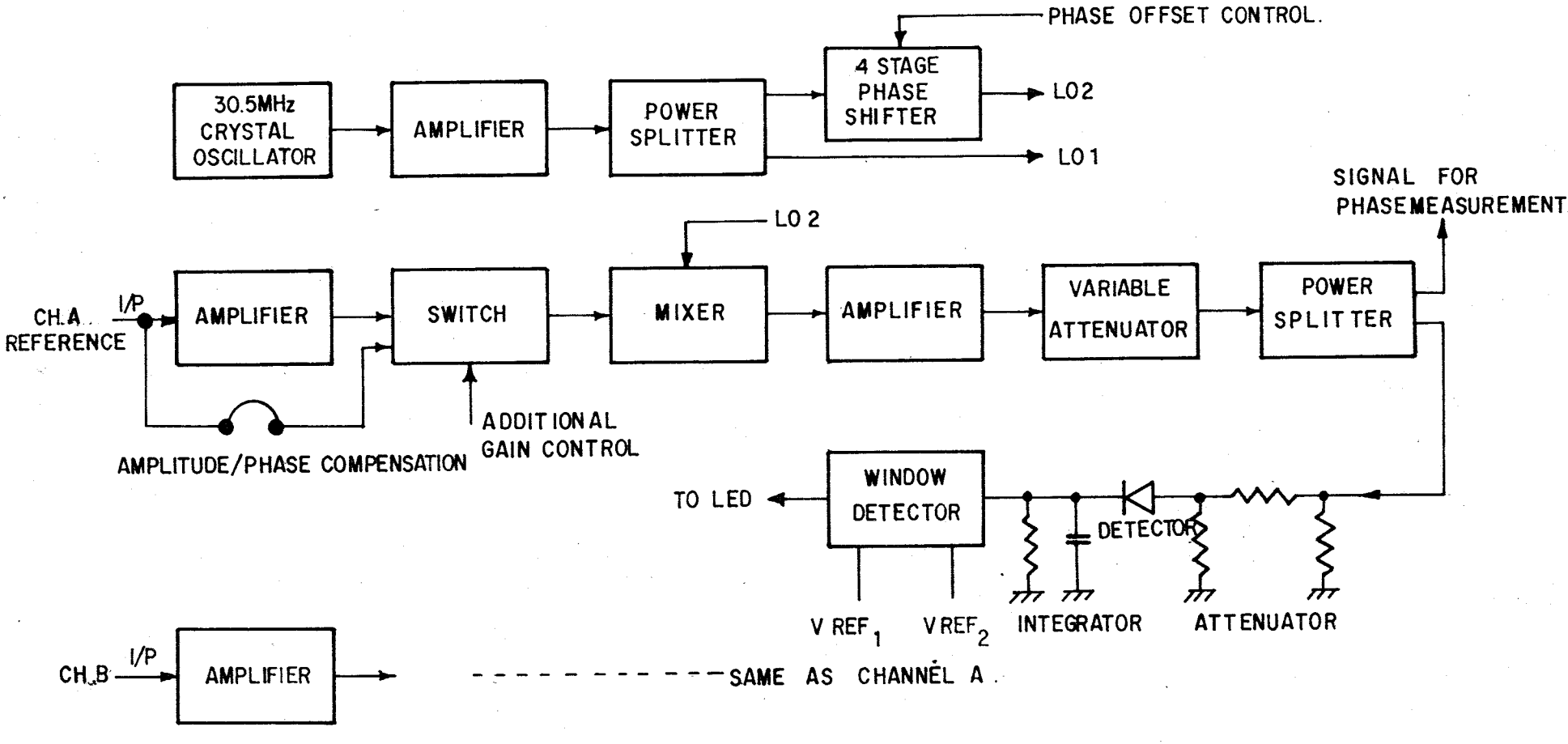


FIG. 3·20. FIELD TEST EQUIPMENT – SUPERHETERODYNE RECEIVER.

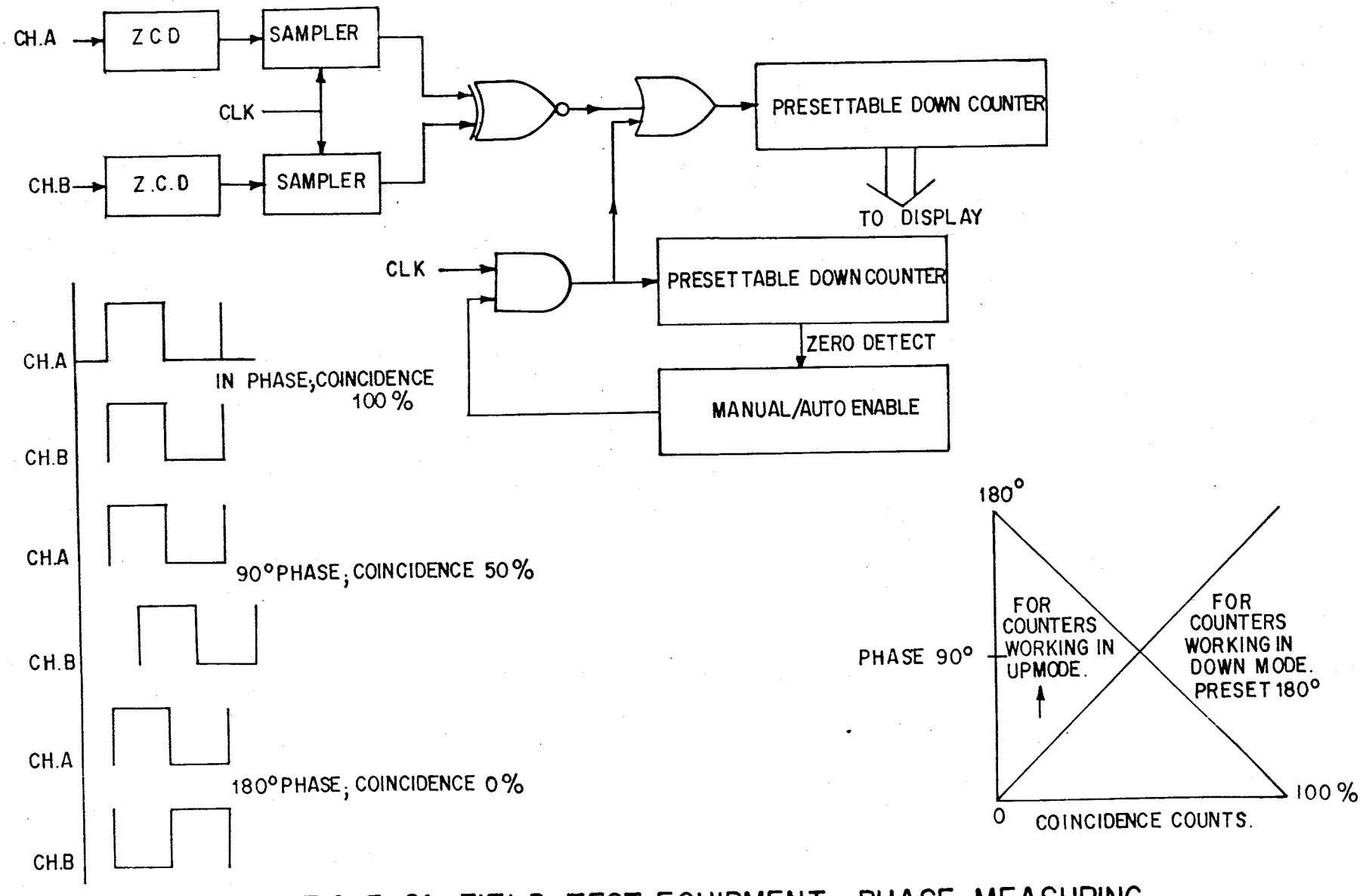


FIG. 3·21. FIELD TEST EQUIPMENT - PHASE MEASURING SCHEME.

counter. Only the three most significant digits of the counter are displayed. If the signals are completely in phase, the coincidence count will be 100%. For 90° phase shift, the count will be 50%. For 180° phase shift, coincidence counts will be zero. To get a measure of the phase directly, the counters are preset to 180,000 (a six stage B.C.D. counter) and are operated in the down mode. A burst generator which generates exactly 180,000 pulses is designed using presettable counters. The output of the burst generator is used for sampling the output of the multiplier. After the burst is complete, the counters give a measure of the phase directly. The burst generator can be set to auto/man mode. In the automode, the burst is restarted at the end of every 4 seconds. In the manual mode, the burst operates only when enabled.

The sign of the phase is indicated by sampling the output of the Z.C.D. by using the output of the reference Z.C.D. as the clock. This equipment has been tested and is now ready for use. It will reduce the need for expensive test equipments. When the noise generator is used for testing, the gain calibration will be different and can be read from a standard table. The display does not indicate the phase directly, since Van Vleck correction has to be applied for noise like signals.

3.12 CORRELATOR

The correlator is a single channel one-bit correlator which displays coincidence counts directly. (a six digit display). The circuitry is the same as the phase measuring part of the field test equipment. Here the burst is preset to 100,000 counts. Some of the special features are

1. It can accept both analog and digital inputs (switch selectable).

2. It has a built in 1 MHz crystal oscillator for sampling. It can accept both a TTL or CMOS compatible external sampling clock.

3. It can delay one of the inputs by an integral period of the sampling clock and can measure the correlation. This will be helpful in measuring the delay between signals.

3.13 H.P. PRINTER INTERFACE

While testing, it is essential that the performance of the receiver system be evaluated. As there is no computer facility at Gauribidanur to read a magnetic tape, a 10 column H.P. printer which can print 10 lines/sec was interfaced to the correlator. The input data lines to Mag-tape and printer are parallel (separated by a buffer). While printing the correlation values, the channel address sin and cos identifications are also printed. Facility

exists to select the start and stop address of the channels. This is very handy when performing system checks at any time.