CHAPTER 4

EXPERIMENTAL WORK

4. EXPERIMENTAL WORK

A number of new addressing techniques for multiplexing matrix LCDs with rms response have been proposed in the previous chapter, along with the theoretical analysis in each case. The hardware realization of some of these techniques, viz., BAT, HAT, IHAT, IHAT-S4, RPAT-NC and RPAT-PC is taken up in this chapter, in view of the importance of the same. The block diagrams of the display systems using these addressing techniques and the approach to their realization are discussed first. This is followed by the details of the implementation and discussion of the results obtained by using these techniques.

4.1 APPROACH TO REALIZATION

4.1.1. BAT

The BAT is suitable for single row alphanumeric displays, where the number of lines to be multiplexed (N) is small (Appendix 6.a).

a) <u>Block diagram</u>

The block diagram of a display system using BAT is shown in Fig.4.1. The character information is stored in the memory. The standard ASCII code is used for storing the alphanumeric characters to be displayed. This information in the memory is updated through the interface, which connects the display to an input equipment (computer, keyboard, etc.) depending on the application. The Character Generator (CG) converts the ASCII code to pixel information. A column-wise output is required for the BAT. The 2^N row-select patterns required for BAT are obtained from the Sequence
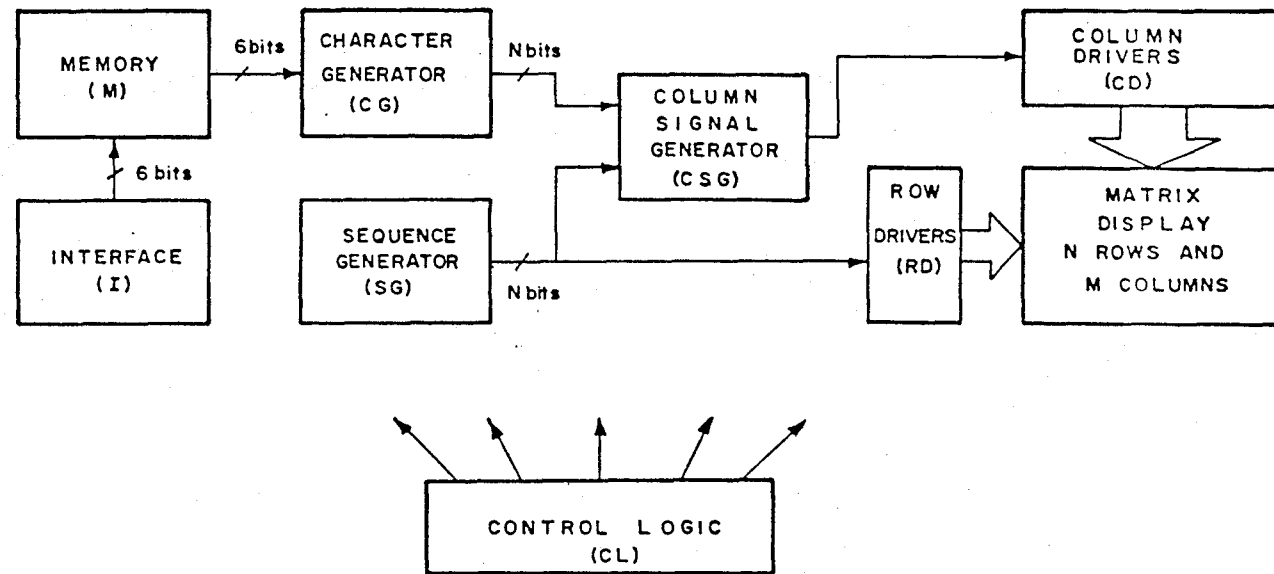
Fig. 4.1. Block diagram of display system using BAT.

Generator (SG). The Column Signal Generator (CSG) compares the data from the CG and the row-select pattern from SG bit-by-bit and generates the data for the Column Drivers (CD). This requires a majority decision as discussed in section 3.1.2. The Row Drivers (RD) obtain the row-select pattern from SG. The row-select pattern and the column data should be simultaneously applied to the matrix display. This is ensured by providing a buffer and latch in both the row and column drivers. The Control Logic (CL) synchronizes the display refresh, by generating the appropriate address and control signals using a clock.

b) Approach to Realization

The possible realization of the various blocks along with alternatives, if any, are discussed below.

- Character Generator (CG)

The segment or pixel information of the alphanumeric characters is stored in the CG. An UV-EPROM, EEPROM or ROM could be used here depending on the application.

- Sequence Generator (SG)

An N-bit binary counter generates all the 2^N combinations of row-select patterns required for the BAT. However, the frequency of the counter outputs (row waveforms) increases from MSB to LSB by a factor of two for each bit. This large variation in the frequency of the row addressing waveforms will lead to brightness non-uniformity of the pixels (contrast variation) as discussed in section 2.4.3. While the use of Gray-code will be helpful to reduce frequency variation in the row waveforms, the Pseudo

Random Binary Sequence (PRBS) is a better alternative for the SG. The PRBS and its delayed versions have identical wave shape and hence identical frequency components. But, these sequences have only (2^N-1) states and they do not include the state with all zeros. A sequence generator with all the 2^N states can be obtained by inserting the state with N zeros in the PRBS generator [79]. Such a sequence generator for two values of N, viz., N = 3 and 5 are shown in Fig.4.2 as examples.

- ### Column Signal Generator (CSG)

The row-select and the data patterns are compared bit-by-bit using Exclusive-OR gates. The column voltage is decided using a majority decision as discussed in section 3.1.2. The majority decision can be implemented using gates, multiplexers or adders. Programmable Logic Array (PLA) and UV-EPROM are the other possible alternatives for the CSG. Here, both the bit-by-bit comparison and the majority decision can be absorbed into a single block.

- ### Alternatives for CG and CSG

The CG and CSG can be combined into a single block and can be realized using a single ROM, UV-EPROM or EEPROM. The column signal can be directly stored for all the combinations of row-select patterns, column data and the characters.

- ### Drivers

Driver ICs commonly used for directly driven displays are suitable for BAT. The schematic of a typical driver IC is shown in Fig.4.3. The
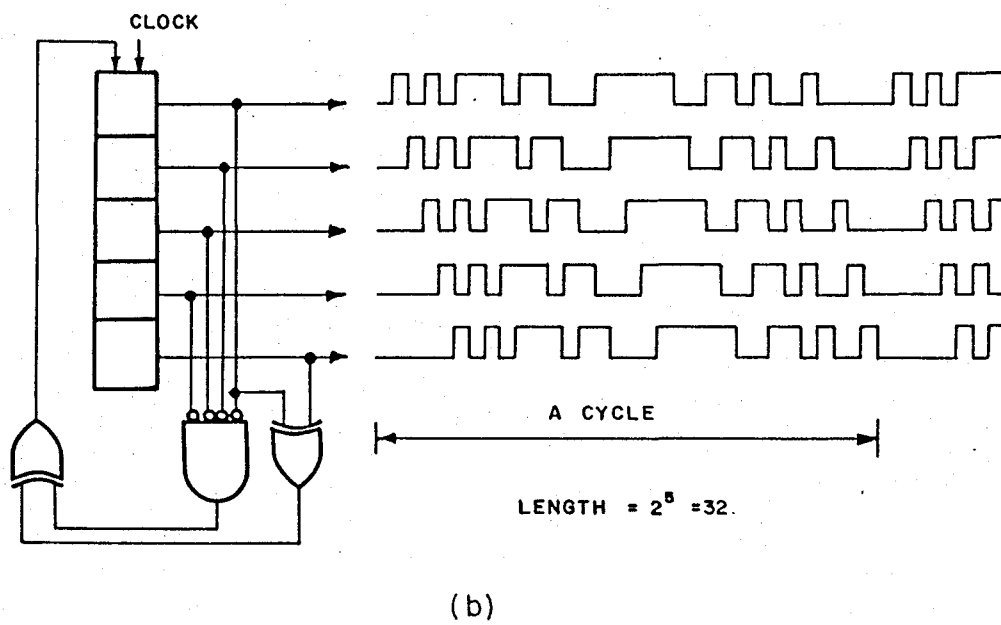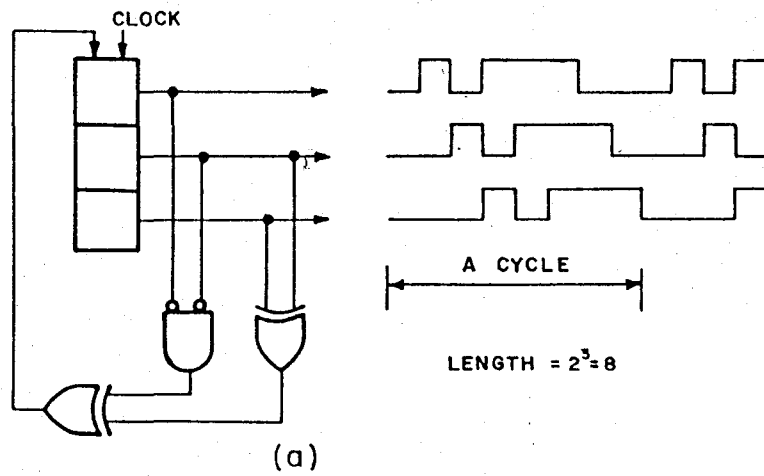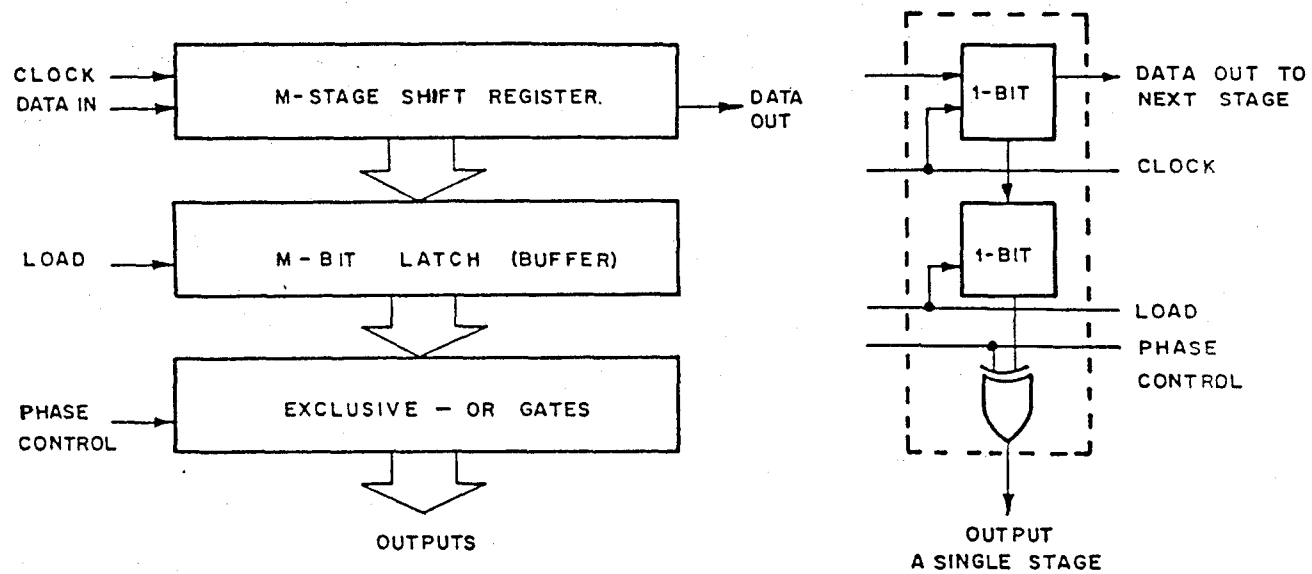
Fig. 4.2. Sequence generators for N = 3 and 5.

Fig. 4.3. Schematic of a typical driver IC used in directly driven displays.

Exclusive-OR gates are provided to enable phase-reversal, in order to ensure a dc-free operation. But, as the BAT has a natural dc-free operation (as discussed in section 3.1) the phase control input of the EX-OR gates can be permanently tied to logic 0 or 1. Alternatively, the drivers can be implemented using shift registers and latches. The length of the shift register and the number of latches required in the row and column drivers is equal to the number of row and column address lines respectively.

4.1.2. Hybrid Addressing Techniques (HATs)

The HAT (see Appendix 6.b) IHAT, IHAT-S3 and IHAT-S4 discussed in chapter 3 have many common features, since they are based on the same principle. The basic difference between these techniques is the number of voltage levels in the column waveforms as shown in Table 3.19. Hence the block diagram and the approach to realization of the different versions of HAT are discussed here.

a) Block Diagram

The block diagram of the display system using HATs is shown in Fig. 4.4. The information to be displayed is stored in the memory and this can be updated through the interface. The data to be displayed in the selected sub-group of rows (l rows) is loaded into the Re-Circulating Register (RCR) temporarily, for comparing it with the row-select pattern. Hence the size of this register is $l \times M$ bits. The Sequence Generator (SG), generates 2^l, l-bit row-select patterns, for selecting l address lines in the selected sub-group. The Column Signal Generator (CSG) compares the column data pattern in the selected sub-group of rows bit-by-bit with the
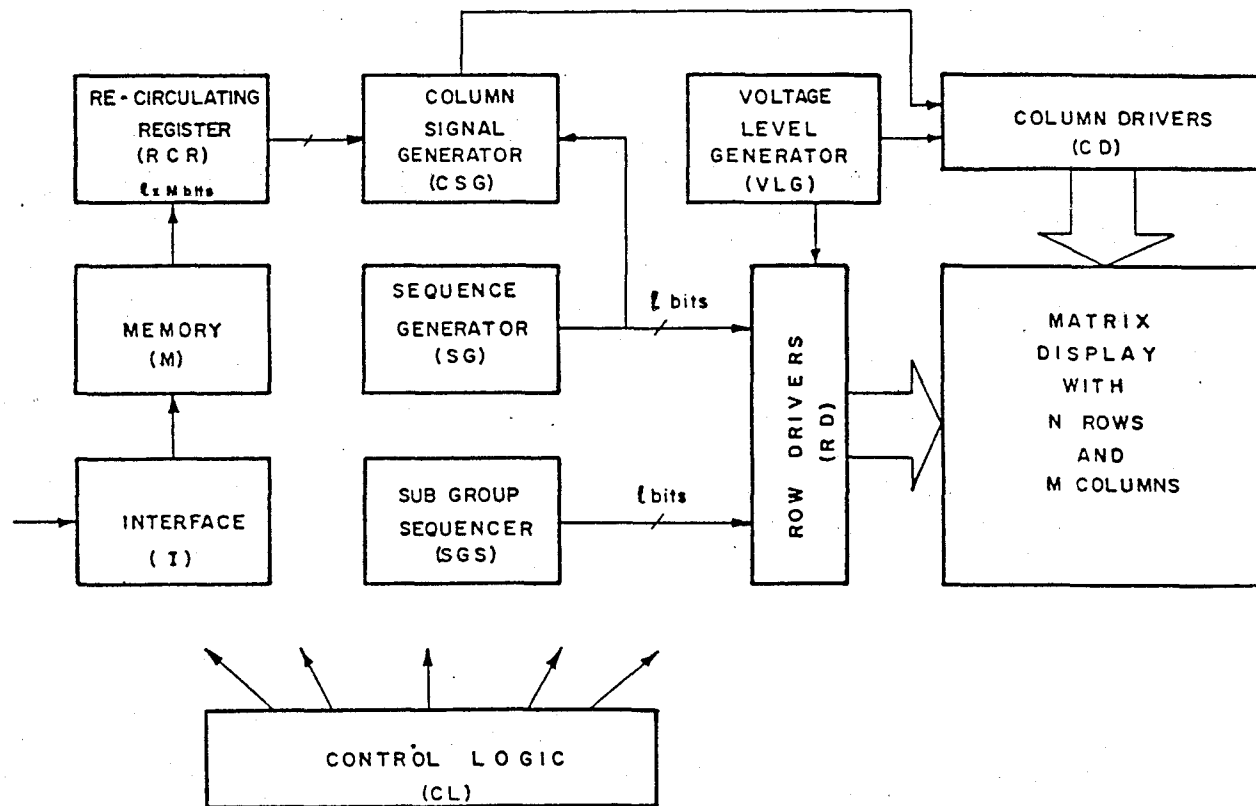
Fig. 4.4. Block diagram of the display system using HATs.

row-select pattern and generates the data for the column drivers. The Sub-Group Sequencer (SGS) determines the l address lines to be selected with voltages corresponding to the l-bit row-select pattern. The data in the RCR corresponds to these selected address lines. The Voltage Level Generator (VLG) is used to generate the various voltage levels in the row and column addressing waveforms. The Row Drivers (RD) are connected to the row address lines of the display and the row voltages are controlled by the row-select pattern obtained from SG and SGS. The Column Drivers (CD) are connected to the column address lines and the column voltages are controlled by the column signal from the CSG. The control logic governs the operation of the various sub-blocks described above and synchronizes the flow of information for refreshing the display.

This block diagram is common for the hybrid addressing techniques, viz., HAT, IHAT, IHAT-S3 and IHAT-S4 discussed in chapter 3. The primary difference between these techniques is the number of voltage levels in the column waveform. This gives rise to different values of relative V_r/V_c for these techniques. The differences in the implementation of the following blocks depend on the particular version of HAT as discussed below:-

- **VLG.** The number of voltage levels generated for the column drivers depends on the grouping of errors in the addressing technique. The number of voltage levels is 2, $(l+1)$, 3 and 4 for the HAT, IHAT, IHAT-S3 and IHAT-S4 respectively. The relative amplitudes of the column voltages with respect to that of V_r, also depends on the technique as discussed in chapter 3.

- *CSG.* The number of bits transmitted as signal to the column drivers depends on the addressing technique. The number of bits is 1 for HAT and 2 for IHAT-S3 and IHAT-S4. This value depends on l in the case of IHAT and is $log_2 (l+1)$, rounded off to the next higher integer when fractions are encountered.

- *CD.* Analog multiplexers are used in the column drivers to switch the column voltages depending on the signal from CSG. The type of multiplexer required for the addressing techniques are $2 : 1$, $(l+1) : 1$, $3 : 1$ and $4 : 1$ for the HAT, IHAT, IHAT-S3 and IHAT-S4 respectively.

The rest of the blocks, viz., Memory, Interface, RCR, SG, RD and the control logic are common to all the addressing techniques discussed above.

b) Approach to Realization

The possible realization of the various circuit blocks along with alternatives, if any, are discussed below.

- **Re-Circulating Register (RCR).**

The hybrid addressing techniques require a bit-by-bit comparison of the data to be displayed with the row-select pattern. The RCR facilitates this by storing the data temporarily for repeated comparison with the different row-select patterns. The RCR requires l (= the number of address lines in the selected sub-group) shift registers, each of length M (= the number of columns in the display). Alternatively FIFO (First-In-First-Out) memories can be used along with a feed back for re-circulating the

data. The RCR is provided only for the ease of accessing the same data repeatedly and is optional. An l-bit buffer is adequate, if repeated memory access can be accommodated to fetch the data from the memory.

- ### Sequence Generator (SG)

The SG generates all the 2^l, l-bit row-select patterns required for selecting a sub-group. The SG can be an l-bit binary counter, Gray code generator or PRBS generator with 2^l states as discussed earlier for BAT. Here again, a Gray code generator or PRBS generator is preferred to achieve the brightness uniformity of the pixels.

- ### Column Signal Generator (CSG)

The l-bit data from the RCR and the l-bit row-select pattern from the SG are compared bit-by-bit to determine the number of errors. The column voltage depends directly on the number of errors in IHAT. This value is transmitted to the column drivers for a proper choice of the column voltage. The number of column voltages is restricted to 2, 3 and 4 in HAT, IHAT-S3 and IHAT-S4 respectively by grouping of errors in CSG and an appropriate signal is transmitted to the column drivers.

- ### Voltage Level Generator (VLG)

The various voltage levels required for the chosen addressing technique are generated by potential division using a resistor network as shown in Fig.4.5 for IHAT-S4. The ratio between the amplitudes of the row and column voltages as demanded by the addressing technique is ensured by a proper choice of the value of the resistors. The potentiometer allows for changing the absolute value of the row and column voltages without
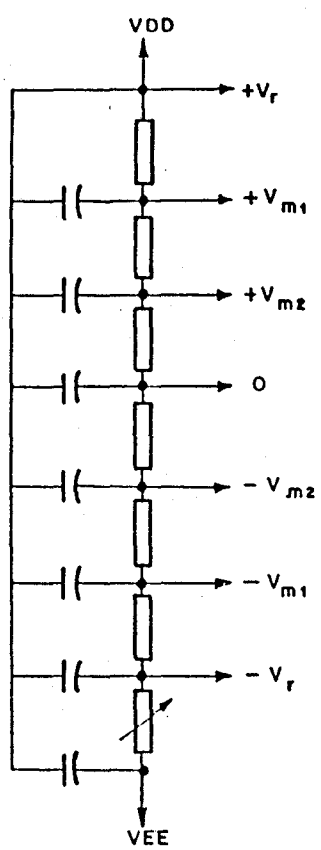
Fig. 4.5. A typical VLG. (IHAT - S4)

altering their ratios. Optional buffer amplifiers can be used for the row and column voltages to reduce the source impedance and is especially useful in large-area displays.

- Column Drivers (CD)

Analog multiplexers are used in the column drivers to switch the different voltages depending on the signal from the CSG. The schematic of a typical CD for HATs is shown in Fig. 4.6. The column signal from the CSG is serially shifted into the shift register. The number of bits (n_c) for each column driver depends on the addressing technique. The value of n_c is 1 for HAT, log_2 $(l+1)$ rounded off to the next higher integer for IHAT and 2 for IHAT-S3 and IHAT-S4. The length of these registers is equal to the number of columns in the display, i.e., M. The row-select pattern applied to the selected subgroup and the column voltages are synchronized using a buffer register. The size of the buffer register is the same as that of the shift register. Analog multiplexer of the types 2:1, $(l+1):1$, 3:1 and 4:1 are required for HAT, IHAT, IHAT-S3 and IHAT-S4 respectively to drive each column in the display. The column voltages are derived from the VLG.

- Row Drivers

The HATs require one of the three voltages, viz., $-V_r$, 0 and $+V_r$ (or 0, V_r and $2V_r$ for unipolar addressing waveforms.) These voltages are switched using a 3:1 analog multiplexer. The rows in the unselected subgroups get a voltage 0 and this is controlled by a single bit from the SGS. The voltages $\pm V_r$ to be applied to the rows in the selected subgroup are
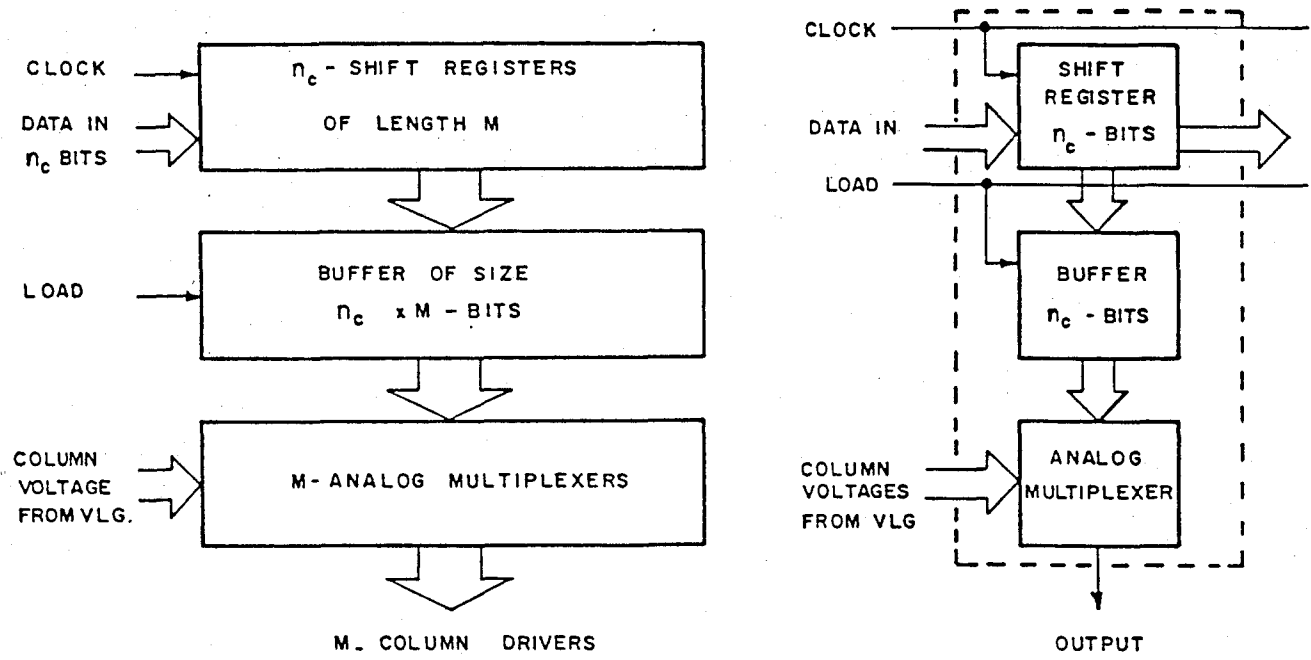
Fig. 4.6. Schematic of a typical column driver for HATs.

controlled by an additional bit for each row from the Sequence Generator. Alternatively the row-select pattern from the SG can be level shifted to $\pm U_r$. Only a 2:1 multiplexer controlled by SGS is required here as compared to a 3:1 multiplexer in the previous case. The total number of multiplexers required is equal to the number of rows in the display, i.e., N. The three voltage levels required here are derived from the VLG.

- **Sub-Group Sequencer (SGS)**

The SGS determines the sequence in which the subgroups are selected. This in its simplest form is a ring counter of length (N/l). The SGS can be hardwired for a successive or random selection of the subgroups. However, the control logic should be designed to place the data corresponding to the selected subgroup in the column drivers. A digital de-multiplexer can be used as an alternative to the ring counter.

- **Control Logic (CL)**

The control logic governs the flow of information and synchronizes the various blocks in the display system. They can be implemented using gates, flip-flops and counters.

4.1.3. RPATs

As already discussed in section 3.6, the selection ratio of RPATs is independent of the matrix size. This enhances the usefulness of LCDs for displaying **multiple waveforms** in oscilloscopes, Logic Analyzers and other display applications without sacrificing the high resolution required in such displays.

a) Block Diagram

The block diagram of a digital oscilloscope is shown in Fig.4.7 as a typical example of RPAT applications. The waveforms are acquired through the Waveform Acquisition Module (WAM), which consists of Amplifiers with Programmable gain,. Analog Multiplexers, Sample and Hold Circuit and ADC. These waveforms are stored in Waveform Memories (WM-1 to WM-w). The ASCII code of the alphanumeric information forming the legends to be displayed is stored in a separate memory, called Legend Memory (LM). The Character Generator (CG) converts the ASCII code from this memory to the pixel information. The display is refreshed from a Bit-Mapped Frame Memory (BFM). The Display Data Formatter (DDF) loads the pixel data of the waveforms and legends into the BFM. The Row Drivers (RD) and the Column Drivers (CD) generate the addressing waveforms, that are applied to the row and column address lines. The various voltage levels required for the row and column drivers are obtained from the Voltage Level Generator (VLG).

b) Approach to Realization

The possible realization of the various blocks along with alternatives, if any, are discussed below:-

- **Waveform Memory (WM)**

The WM consists of a RAM or Shift registers organized as recirculating memory. The size of the memory depends on the resolution of the ADC and the number of sample points to be displayed. It should be at least $M \times R$ bits, where M is the number of columns in the matrix display
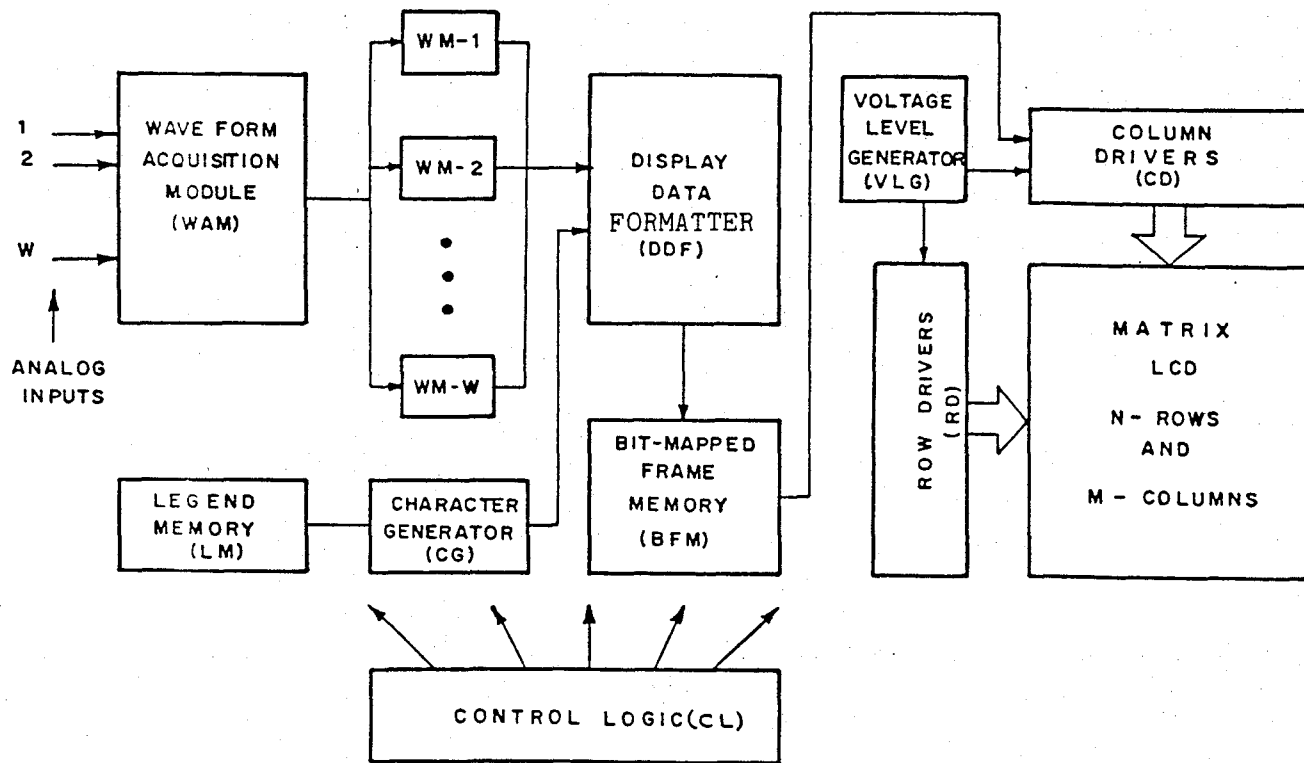
Fig. 4.7. *Block diagram of a digital oscilloscope.*

and R is the resolution of the ADC. A memory of size $2M \times R$ per waveform, enables pre-trigger display of the acquired waveform.

- **Legend Memory (LM)**

The alphanumeric characters and special symbols that are to be displayed as legends are stored here. A RAM is useful for the implementation of the LM.

- **Character Generator (CG)**

The pixel information corresponding to all the alphanumeric characters and special symbols are stored in the CG. An UV-EPROM, EEPROM or ROM could be used here, depending on the application.

- **Display Data Formatter (DDF)**

The pixel information of the waveforms and legends to be displayed is loaded into the BFM using the DDF. The scaling of the amplitude and shifting of the waveforms (required to avoid any overlapping among them) are performed in the DDF. The data loaded into the BFM should be in the format as that required on the display. A microprocessor-based DDF is preferred here as compared to a hard-wired logic, since various steps requiring intelligence are involved in this block. Apart from this, a number of useful measurements on the waveform data can be performed, if a microprocessor is used here.

- **Bit-mapped Frame Memory (BFM)**

The BFM is a RAM and each bit here corresponds to a pixel in the matrix display. The size of this RAM should be $(N+d) \times M$. The additional

d-rows correspond to the dummy rows which are included to keep the number of selected pixels in a column constant, when two or more waveforms intersect as discussed in section 3.6.

- **Voltage Level Generator (VLG)**

The VLG consists of a resistor network and the various voltage levels are generated through potential division by using appropriate values of resistors. This is similar to the VLG discussed for the HATs.

- **Row Drivers (RD) and Column Drivers (CD)**

The same type of RD and CD as used in multiplexed displays, using IAPT are adequate here. Fig.4.8 gives the schematic of HD44100 (Hitachi), LCD driver with 40-channel output as an example. It consists of two sets of 20-stage bidirectional shift registers to convert the serial data at the input into parallel form. Two sets of 20-bit latches are provided to synchronize the row and column waveforms, applied to the matrix display. The two sets of 20 LCD drivers consist of analog multiplexers to generate the addressing waveforms by switching the voltage levels from the VLG. The first set of 20 drivers can switch the output voltage to any one of the four levels, viz., V1, V2, V3 and V4 while the second set of 20 drivers can switch the output voltage to any one of the four levels, viz., V1, V2, V5 and V6. The first set of 20-drivers are primarily designed as column (segment signal) drivers. The second set of 20-drivers can either be used as column drivers or as row (common signal) drivers and is preselectable using the FCS input. The M input is provided to reverse the polarity of the addressing waveforms (for the IAPT discussed in chapter 2) in order

Fig. 4.8. Schematic diagram of HD44100 (LCD Driver IC)
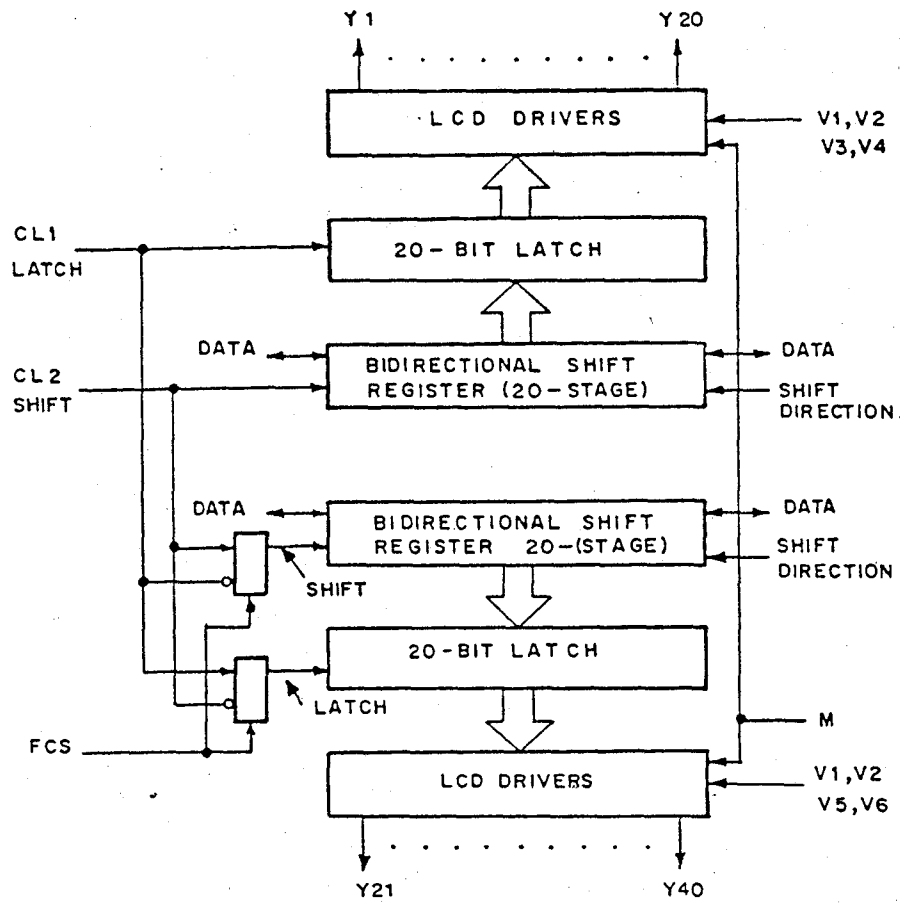
TRUTH TABLE

FCS	DATA	M	Y1 – Y20	Y21 – Y40
VCC (1)	1	H	V1	V2
		L	V2	V1
	0	H	V3	V6
		L	V4	V5
GND (0)	1	H	V1	V1
		L	V2	V2
	0	H	V3	V5
		L	V4	V6

to ensure a dc-free operation. All the 40-LCD drivers can also be used as row drivers instead of column drivers, if the voltages V3, V4, V5 and V6 correspond to those of row drivers and if the appropriate control signals, viz., CL1, CL2 and M are generated externally. The truth-table in Fig.4.8 gives the LCD driver outputs for all the combinations of FCS, Data and M.

- **Control Logic (CL)**

Although the control logic can be hard-wired using SSI and MSI ICs, a microprocessor-based CL is appropriate here since both the control functions and data formatting can be performed by using the same microprocessor.

4.2   IMPLEMENTATION

The implementation of BAT, HAT, IHAT, IHAT-S4, RPAT-NC and RPAT-PC in the laboratory are discussed in this section. This is followed by the experimental results.

4.2.1   BAT

The BAT is demonstrated using a four character, 16-segment TN LCD (Appendix 6.a).

a) *Display*

A 16-segment font is used here to display alphabets (upper case), numerals and some special symbols. The identical segment patterns on each of the top and bottom glass plates are interconnected to form a matrix. Here the interconnection in each glass plate should be in one plane without

any crossings and is similar to the layout on a single sided PC board without any jumpers. This restricts the choice of the matrix organisation. An interconnection scheme for a four character array which results in a 4 x 16 matrix is illustrated in Fig.4.9. The number of external connections here is 20 (4 row and 16 column connections) as compared to 65 (1 back-plane and 16 x 4 segment connections) in the case of a directly driven display. The specifications of the display are as given below:-

- Character size : 18 x 12 mm
- Active Area : 70 x 20 mm
- Connector pitch : 5.08 mm
- Threshold Voltage : 2.03 V
- Sharpenss parameter : 12.8 %

The majority decision in BAT demands the number of lines (rows) multiplexed to be odd as discussed in section 3.1.4. Hence, N is chosen to be 5 here. The selection ratio as calculated using eqn. (3.15) is $R = 1.483$. It is evident from the specifications that the value of the sharpness parameter of the NLC mixture (RO-TN-619, a commercial mixture from F.Hoffmann La Roche & Co., Switzerland) is quite adequate for the present application. The N_{eq} for BAT when $N = 5$ is 7.111 (using eqn. 3.19).

b) Hardware

The schematic diagram of the display system is given in Fig.4.10. The display is interfaced to a keyboard (RCA VP-601). The 8-bit parallel ASCII codes from the keyboard are stored in CD 4036A, a 4 x 8 bit CMOS RAM.

ROW 1
ROW 2
ROW 3
ROW 4

C 3   C 4   C7   C8   C 11   C12   C 15   C16

C1   C 2   C5   C6   C9   C1O   C13   C14
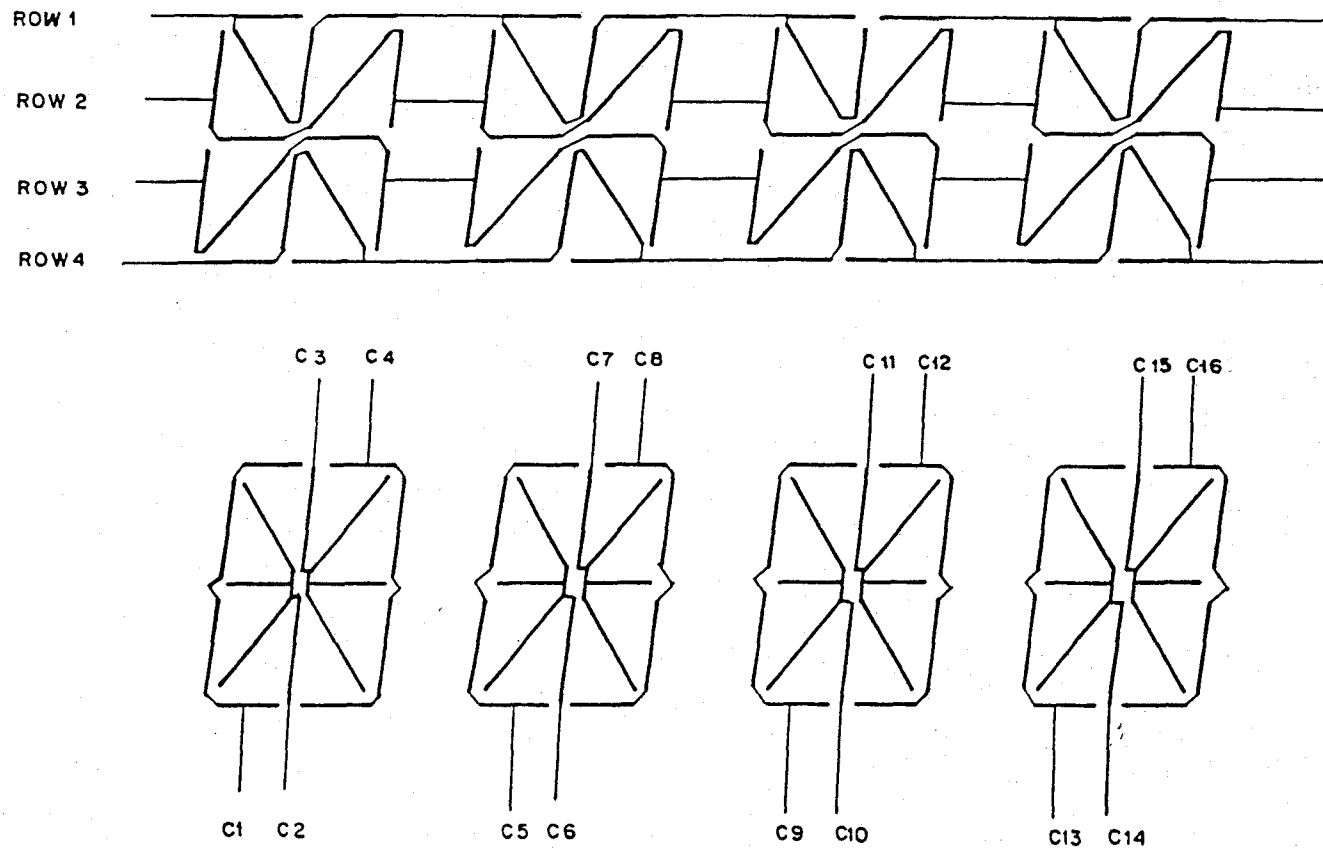
Fig. 4.9. Interconnection scheme for 16 segment 4-character LCD.

Fig. 4.10. Schematic diagram of a display system using BAT.

The Sequence Generator (SG) of length 32 is implemented using CD4015B (Dual 4-stage shift register with serial input and parallel outputs), CD 4030 (Quad Exclusive-OR gate) and CD 4002 (Dual 4-Input NOR Gate).

The Character Generator (CG) and the Column Signal Generator (CSG), shown in Fig.4.1 are combined into a single block as discussed in section 4.1.1 and the same is implemented using a ROM. The 6-bit ASCII code from the RAM (CD4036) together with the 5-bits from the SG (row-select pattern) form the address input to this ROM. The four column signals corresponding to a single character and a row-select pattern are stored in one location of the ROM. The total memory requirement here is $2^{(6+5)} \times$ 4-bits, i.e., 8-K bits. 27C32, a 4K x 8-bits CMOS UV-EPROM is used here.

The column signals from the EPROM are loaded into CD4035, a 4-stage parallel-in/parallel-out shift register. They are serially shifted out of CD 4035 into a 16-bit serial-in/parallel-out shift register. This is implemented using two CD 4015, a dual 4-stage serial-in/parallel-out shift register. Four CD 4054s (4-segment display driver commonly used in directly driven LCDs) are used here, as column drivers. Each one of these drivers is connected to the corresponding 4-bit column signal loaded into the CD 4015s. An additional CD4054 is used as the row driver with a 4-bit input (RS0 to RS3) from the Sequence Generator (SG).The RS4 output of the SG (corresponding to the dummy row) is used for the generation of the column signals only and is not connected to the display. The row and column signals are loaded simultaneously into the latch provided in each of the CD 4054 drivers. The amplitudes of the addressing waveforms can be varied using the level shifts in the CD 4054 driver. The supply voltage required

for BAT, when N = 5 as determined using eqn. (3.23) is 1.789 V_{th}. Hence the amplitude of the addressing waveform should be 3.632 V since the V_{th} of the NLC mixture used in the display is 2.03 V, as given in the specifications. The supply voltage for the display system here is not constrained by amplitude of the addressing waveforms since this value is lower as compared to 5V, required for the keyboard, EPROM and the logic circuits. The potential difference between VDD and VEE terminal is maintained at 1.789 V_{th} in order to achieve the required amplitude for the addressing waveforms.

Some important signals generated in the Control Logic (CL) to synchronize the operation of the display system are given below:-

- 2-bit multiplexed address for read/write operation of the CD 4036,

- P/S control to the CD 4035, required for parallel-loading and serial shifting of information,

- CLK1 for the CD 4035,

- CLK2 for shifting the data in CD 4035,

- L for loading the latches in CD 4054,

- CL to control the display refresh rate.

The control logic is implemented using CD 4047 (a Monostable/Astable Multivibrator), CD 4013 (Dual D Flip-Flop with Set/Reset), CD 4520 (Dual Binary Up Counter) and CD 4053 (Triple 2-Channel Multiplexer/Demultiplexer). The display is refreshed at a rate of about 50 Hz, which is adequate to ensure both the rms response and flicker-free operation of the display.

c) Results

The photographs of the 4 character 16-segment alphanumeric display are shown in Fig.4.11. Both the positive and negative contrast modes in TNLCDs are demonstrated here. From these photographs it is evident that the contrast in the display is good in spite of the lower selection ratio of BAT, this is possible because of a proper choice of the NLC mixture. Typical addressing waveforms as well as the typical waveforms across the ON and OFF pixels in the display given in Fig.4.12. The selection ratio, which is the most important parameter of an addressing technique can be determined by measuring the rms voltage across the ON and OFF pixels. HP 3467A Logging Multimeter, capable of measuring true-rms voltage was used for this purpose. The V_{ON} (rms) and V_{OFF} (rms) were measured for various supply voltages (amplitude of the drive waveforms). Fig.4.13 shows the experimental values of these rms voltages vs. the supply voltage along with the theoretical curves for the same (using eqns. 3.18 and 3.22), for comparison. The value of the selection ratio obtained from the measurements agree with the theoretical calculations within ±1%.

4.2.2. HAT

The HAT is demonstrated using a 32 x 32 matrix TNLCD.

a) Display

The specifications of the 32 x 32 matrix TNLCD are given below:-

- Pixel size   :   2 x 2 mm
- Active area   :   72 x 72 mm
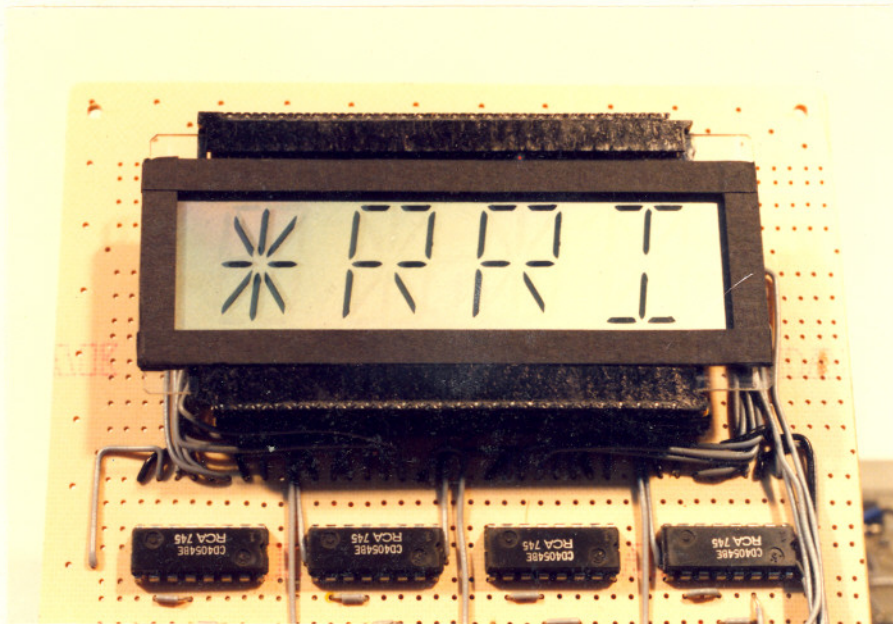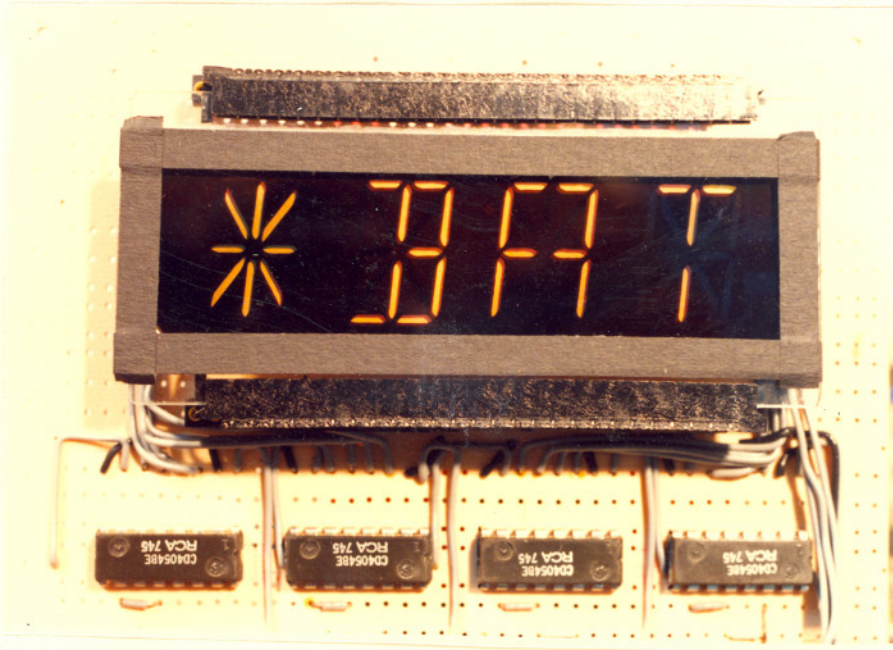
Fig. 4.11. Photographs of a display addressed with BAT (N = 5).
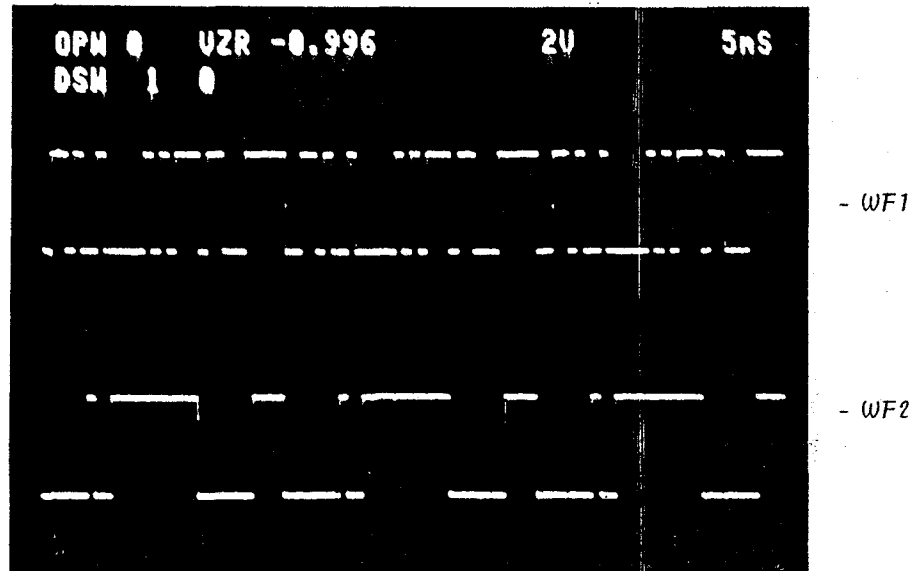
a) *Typical addressing waveforms. WF1 - row and WF2 - column.*
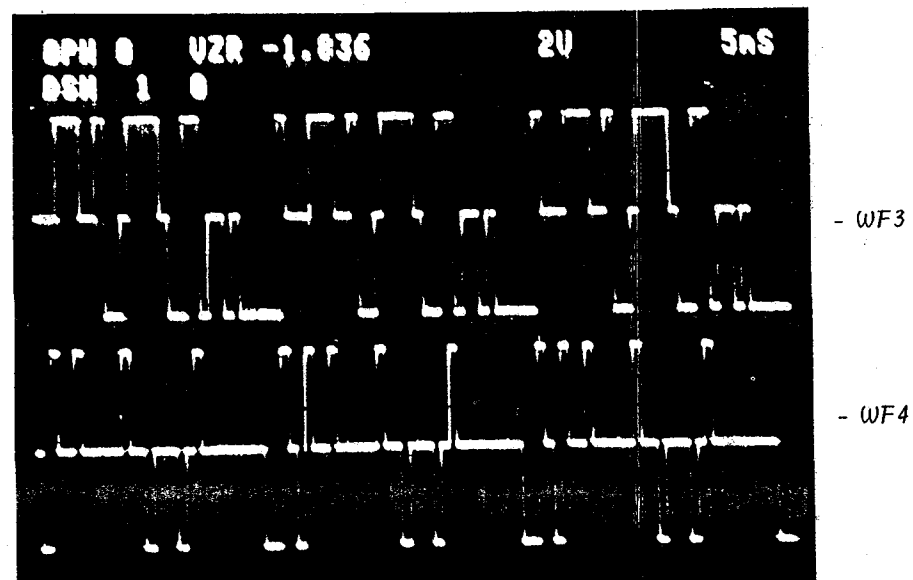
b) *Typical waveforms across pixels. WF3 -ON and WF4 - OFF*

Fig. 4.12. Waveforms of BAT when N = 5 .

BAT with N = 5
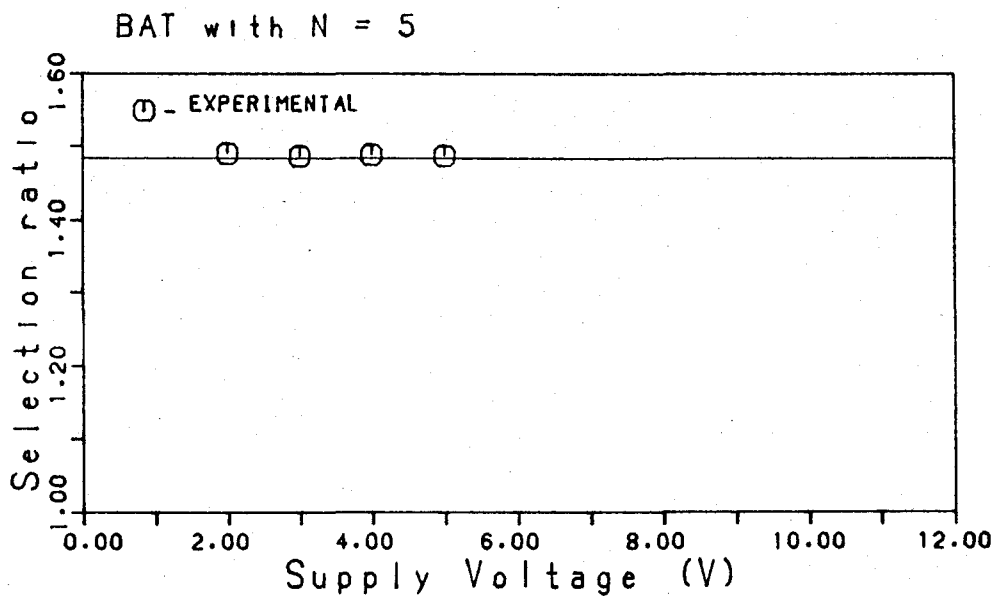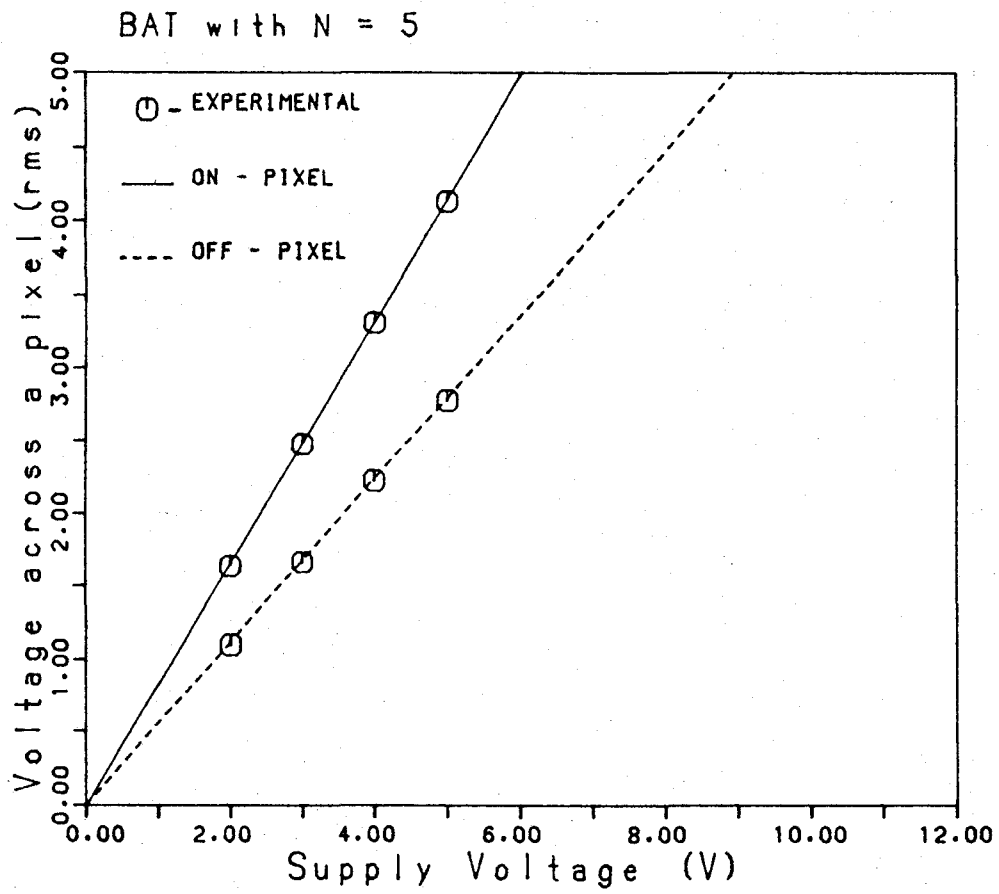
BAT with N = 5

Fig. 4.3: Experimental results of BAT, with N = 5.

- Connector Pitch   :   2.54 mm

- Threshold voltage   :   1.76 V

- Sharpness parameter   :   12.5 %

- Rise time   :   66 ms

- Fall time   :   50 ms.

The HAT demands the value of l to be odd as discussed in section 3.2. The value of l is chosen to be 3 here, since N_{eq} is minimum in this case (Table 3.6). The value of N is chosen to be 33, since N should be an integral multiple of l as discussed in section 3.2. The additional dummy row is not connected to the display and is used only for the generation of the addressing waveforms. The value of N_{eq} for HAT, when N = 33 and l = 3 is 44 (using eqn. 3.41). The selection ratio as calculated using either the value of N_{eq} and eqn. (2.20) or eqn. (3.37) is R = 1.164. It is evident from the specifications given above, that the value of the sharpness parameter is adequate for this application.

b) Hardware

A detailed block diagram of the display system using HAT is given in Fig.4.14. The information to be displayed is stored in 2716, a 2K x 8-bit UV-EPROM. Pixel information corresponding to a single row of the matrix display is stored in 4 successive bytes of this memory. Hence, the first two address inputs are used to acquire the pixel information corresponding to a row. The next five address inputs correspond to the 32 rows of the matrix displays. The remaining 4 address inputs are used to select one of the 16 frames stored in the memory. An EPROM is used here, since the display system is designed to demonstrate the HAT. A RAM and suitable
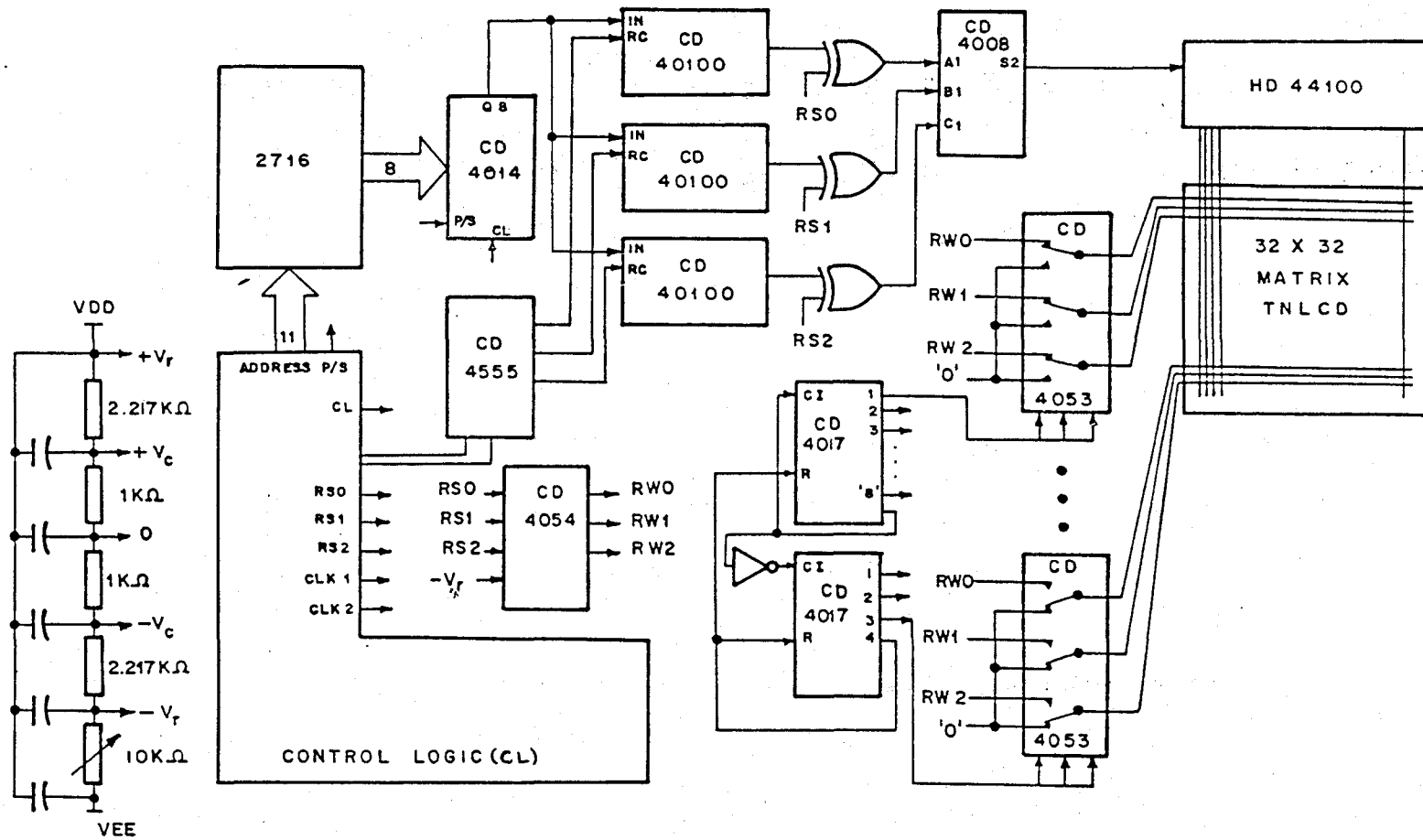
Fig. 4.14. Schematic diagram of a display system using HAT .

interface must be provided in case the display system has to be used as a peripheral device.

The 8-bit parallel output from the 2716 is connected to serial data using CD 4014, an 8-stage Synchronous Shift Register with Parallel or Serial Input/Serial Output. The serial data from the CD 4014 is loaded into a Re-Circulating Register (RCR). This is implemented using CD 40100, a 32-stage static Left/Right Shift Register. The Re-circulate Control (RC) required for the CD 40100s is generated using CD 4555, Dual Binary to 1 of 4 Decoder/Demultiplexer. The data in the CD 40100s corresponds to the subgroup of rows to be selected next.

The outputs from the RCR are compared with the row-select pattern (RS0 to RS2) bit-by-bit by using CD 4070, Quad Exclusive-OR gate. A full-adder can be used as a majority decision circuit, with the output of the three Exclusive-Or gates as the input to the adder and the carry-output of the full adder give the majority decision. This is implemented using CD 4008, a 4-bit Full Adder. The bit-by-bit comparison along with the majority decision forms the Column Signal Generator for HAT as discussed in section 4.1.

HD 44100, an LCD Driver with 40-channel output is used as the column driver. Fig. 4.8 gives the schematic diagram of HD 44100. The data from the CSG is shifted serially into the shift register. The voltage levels $-V_c$ and $+V_c$ from the Voltage Level Generator (VLG) are connected to the 44100 and the outputs are switched to one of these two voltage levels.

The 3-bit row-select patterns (RS0 to RS2) are generated using a

counter and a binary to gray code converter using CD 4520 and CD 4070. The row-select patterns are level shifted to form the row-select waveforms (RW0 - RW2) using a CD 4054, a 4-segment LCD driver. The VEE terminal of CD 4054 is connected to $-V_r$ of VLG so that the outputs of CD 4054 swing from $+V_r$ to $-V_r$ as required for the selected rows in HAT.

The Sub-Group Sequencer (SGS) is implemented using CD 4017, Decade Counter/Divider with 10 Decoded Decimal Outputs (Ring Counter). The length of this counter is extended to 11 (total number of subgroups) by using two CD 4017 along with Clock Inhibit (CI) and Reset (R) as shown in Fig.4.14. The outputs of this SGS select 1- of the 11- subgroup of rows. The SGS is synchronized with the address input of 2716, so that the data in the column drivers corresponds to the selected subgroup.

The row drivers consist of one CD-4053, Triple 2-channel Multiplexer/ Demultiplexer per subgroup. The rows in the selected subgroups are connected to one of the row-select waveforms (RW0 to RW2), while the rows in the unselected subgroups are connected to voltage level '0' from VLG (as discussed in section 3.2). The subgroups are selected using CD 4017 as discussed above. The VEE terminal is connected to the negative supply rail VEE, so that it can switch the row-select waveforms with an amplitude swing $+V_r$ to $-V_r$.

The value of V_r/V_c for N = 33 is 3.317, as calculated using eqn. 3.36. The values of the resistors used in the VLG are given in Fig.4.14. Trimmed resistors with their values accurate to the 3rd decimal position are used here.

Some important signals generated in the Control Logic (CL) for

synchronizing the various blocks in the display system are given below:-

- 11-bit address for reading the pixel information from 2716.

- P/S control of CD 4014 for the parallel load and serial shift of the information from 2716.

- CL, the clock for CD 4014.

- 2-bit control signal to CD 4555 to select the load/Re-circulate mode of CD 40100s.

- 3-bit row-select pattern (RS0 to RS2) with output sequence in Gray code.

- CLK2 to serially shift the data from CSG into the column driver.

- CLK1 to latch the row-select CD 4054 and column data in HD 44100.

The control logic is implemented using astable multivibrator (using CD 4047 as the basic clock), counters, flip-flops and gates. The control logic is hard-wired for the following row-select sequence.

- The selected subgroups are subjected to addressing with all the $8 \ (=2^3)$ row-select patterns successively before selecting the next subgroups.

- The subgroups are selected sequentially in the same order as they are in the matrix display.

The display is refreshed at about 50 Hz, which is quite adequate to ensure the rms response as well as the flicker-free operation of the display.

c) Results

The photographs of the 32 x 32 matrix TNLCD, addressed with HAT

are shown in Fig.4.15. The SG based on Gray code and the sequential scann-ing of subgroups were found adequate to give a good pixel brightness unifor-mity (without any contrast variation) as it is evident from the photographs of Fig.4.15. The photographs of a 32 x 32 matrix display (having the same specification of the display addressed with HAT) addressed with IAPT are shown in Fig.4.16 for a comparison. The brightness non-uniformity of pixels addressed with IAPT depends on the image being displayed and this is illustra-ted in Fig.4.16. This non-uniformity can easily be identified by observing the grey level of the background pixels. The brightness uniformity of the pixels in the display addressed with HAT is superior as compared to that of IAPT although the contrast is lower as compared to that of IAPT as shown in Fig.4.15 and Fig.4.16. Typical addressing waveforms applied to the row and column of the matrix display as well as the typical waveform across the ON and OFF pixels are shown in Fig.4.17. The rms voltage across the ON and OFF pixels were measured using HP 3467A, Logging multi-meter capable of measuring true-rms voltages. Fig.4.18 gives the plot of rms voltage (across ON and OFF pixels) vs. supply voltage. The theoreti-cal curves in this plot are obtained using eqns. (3.46) and (3.37). These curves are provided for a comparison with the experimental results. The value of the selection ratio obtained from the measurements agree with the theoretical value within ±1%.

4.2.3 IHAT

The IHAT is demonstrated using a 64 x 64 matrix TNLCD.
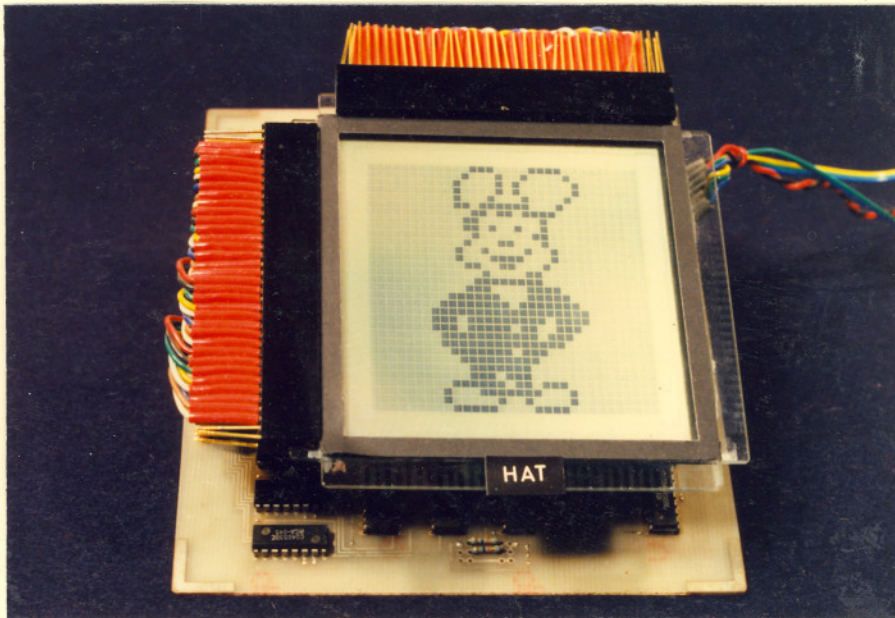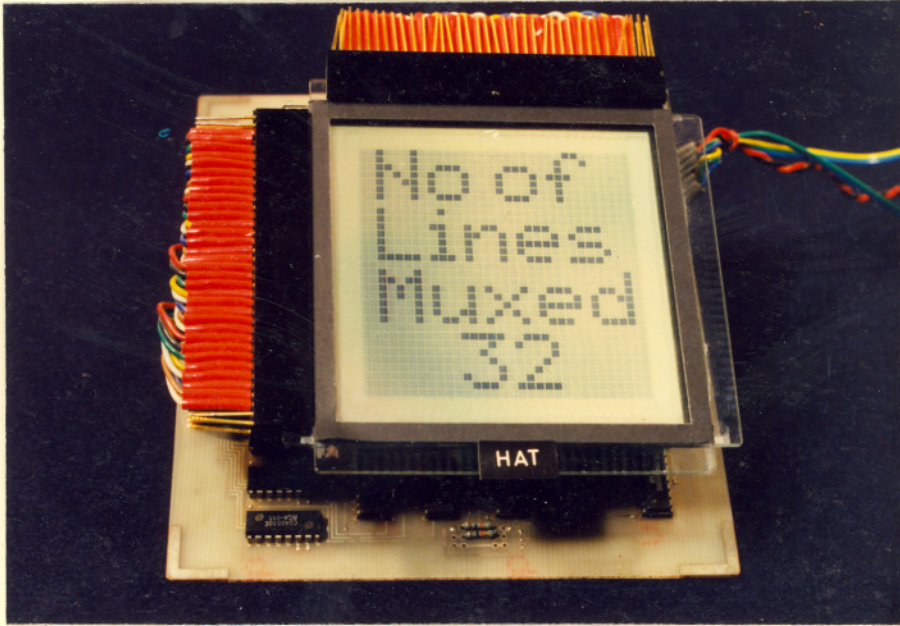
Fig. 4.15. Photographs of a display addressed with HAT
(N = 33 and l = 3).
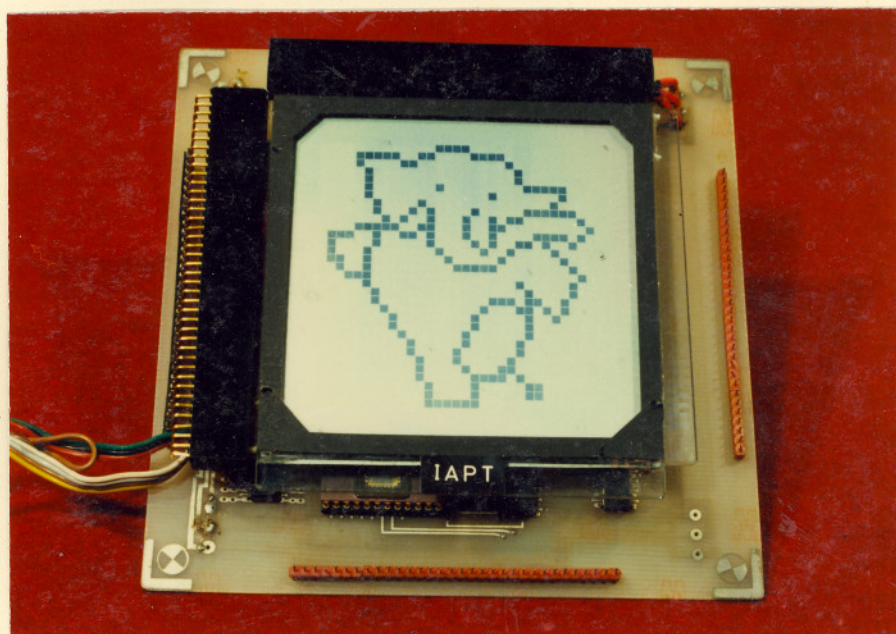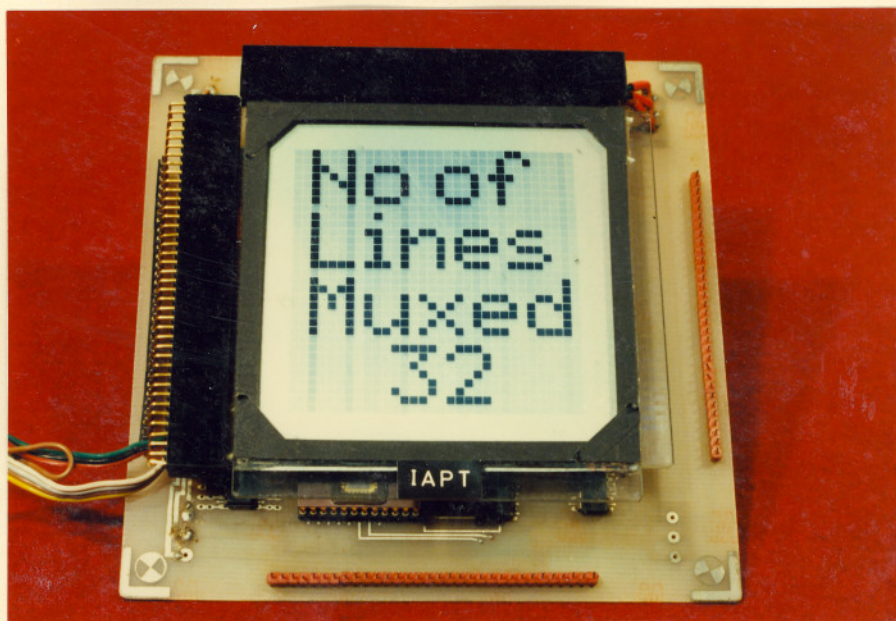
Fig. 4.16. Photographs of a display addressed with IAPT
(N = 32).
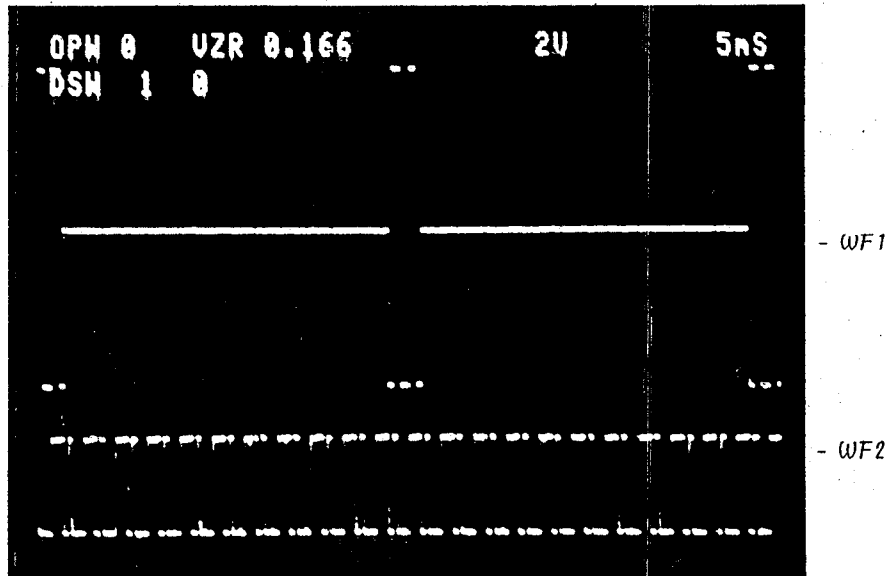
a) Typical addressing waveforms. WF1 - row and WF2 - column.
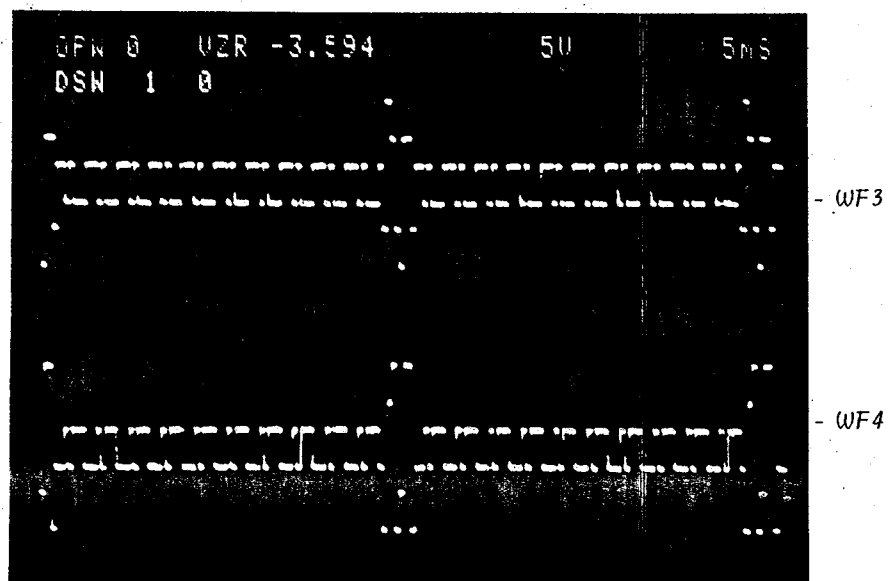
b) Typical waveforms across pixels. WF3 - OFF and WF4 - ON.
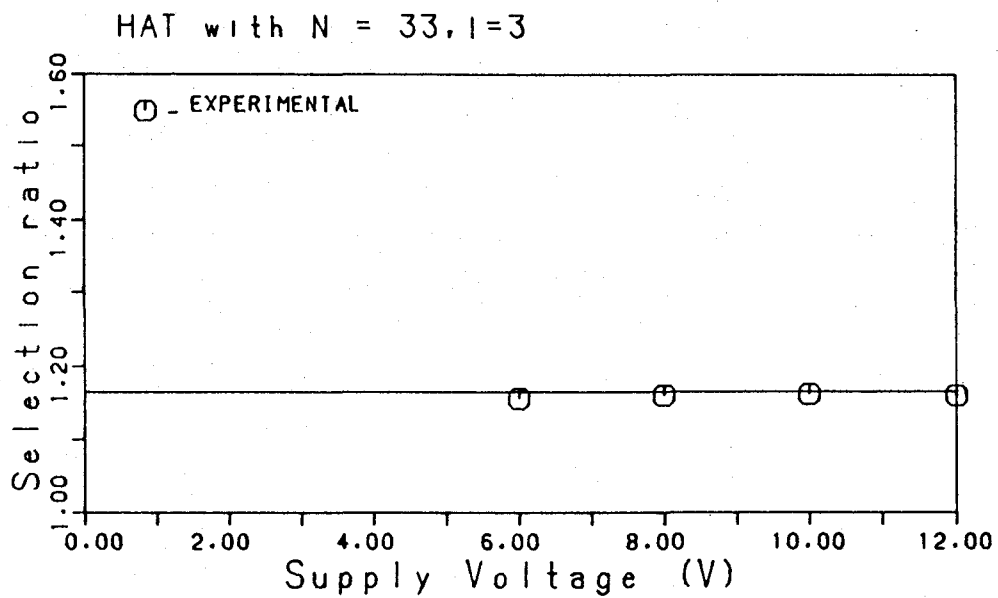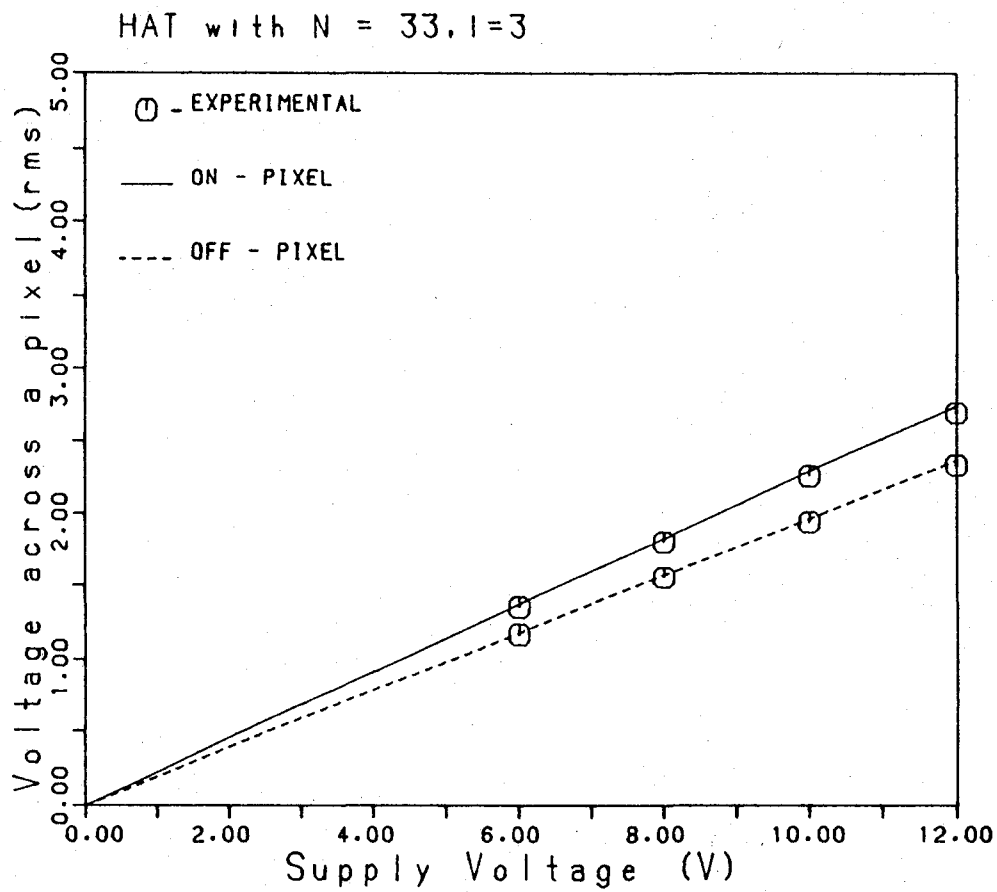
Fig. 4.17. Waveforms of HAT when N = 33 and l = 3 .

HAT with N = 33, l=3

HAT with N = 33, l=3

Fig. 4.18. Experimental results of HAT, with N = 33 and l = 3.

a) _Display_

The specifications of the 64×64 matrix TNLCD are given below:-

- Pixel size   : 1×1 mm

- Active area   : 80×80 mm

- Connector pitch   :   2.54 mm

- Threshold voltage   :   1.76 V

- Sharpness parameter   :   12.5 %

- Rise time   :   66 ms

- Fall time   :   50 ms.

The value of l is chosen to be 7 here, since it leads to a good reduction in the supply voltage requirement as shown in Fig.3.6. The value of N, the number of lines multiplexed should be an integral multiple of l as discussed in section 3.3. Hence, N is chosen to be 63, a number close to the number of rows in the matrix display. The selection ratio of IHAT is the same as that of APT or IAPT and hence N_{eq} of IHAT is N, as discussed in section 3.3. The selection ratio is 1.135, for $N = 63$. It is evident from the specifications given above, that the value of the sharpness parameter of the NLC mixture is just adequate for this application. The supply voltage requirement of IHAT when $N = 63$ as calculated using eqn. (3.99) is 4.538 U_{th}. This value is only 67.13% of the supply voltage requirement of IAPT.

b) _Hardware_

A detailed block diagram of the display system using IHAT is given in Fig.4.19. The information to be displayed is stored in HN 462532, a
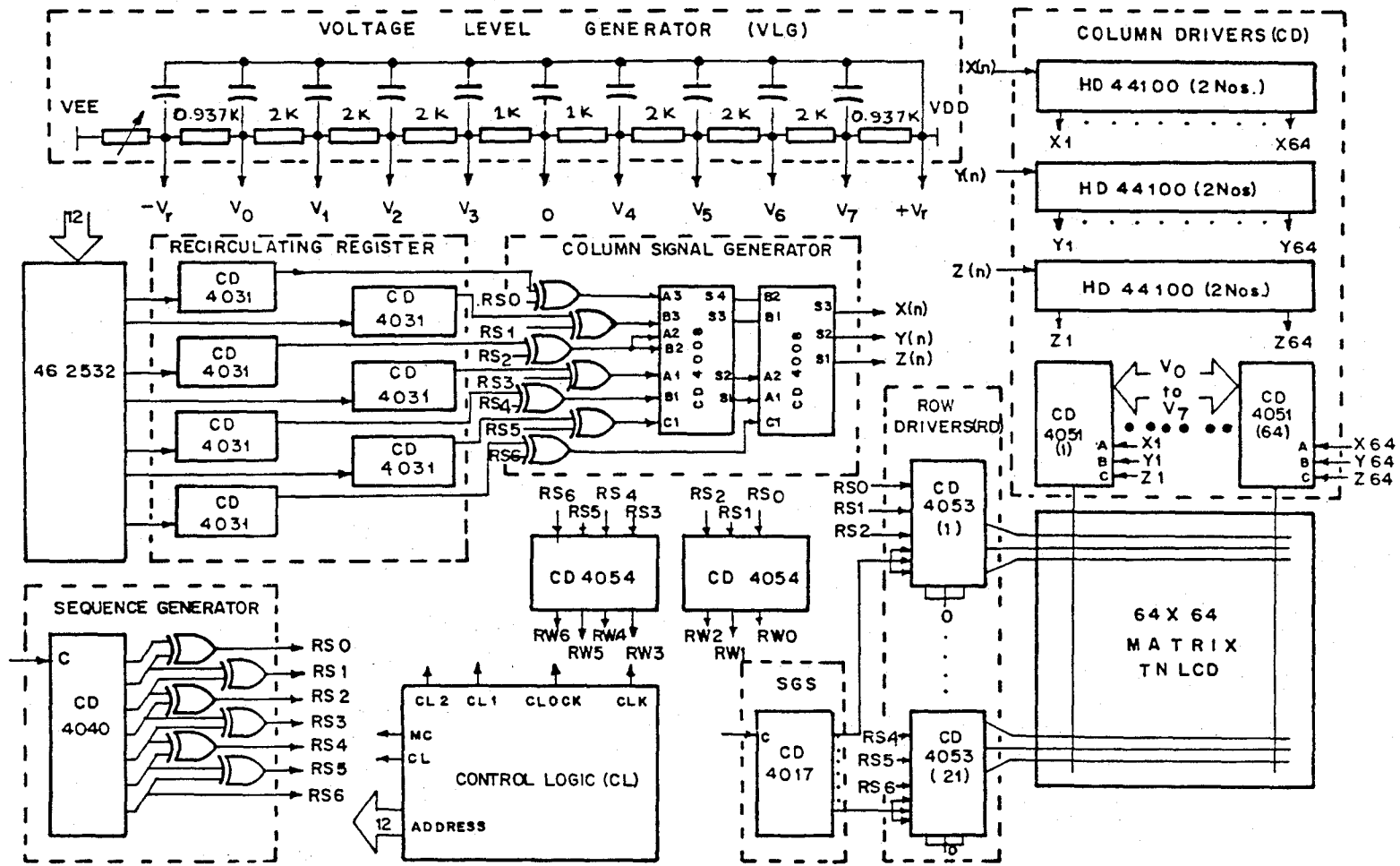
Fig. 4.19. Schematic diagram of a display system using IHAT.

4Kx8-bit UV-EPROM. An EPROM is used here, since the display system is designed only to demonstrate the IHAT. A RAM and suitable interface must be provided in case the display is to be used as a peripheral device. A 7-bit data in a byte of this memory corresponds to the pixel information of a column in a subgroup. This data format eliminates the need for a parallel to serial conversion, which is required if the pixel information is stored row-wise. The first 6-bits of the address input to the memory corresponds to the 64-columns in the matrix display. The next 4-bits correspond to the nine subgroups of rows in the matrix display. The remaining 2-bits are used to select one of the four frames stored in this memory.

The 7-bit parallel data from the memory is loaded into the Re-circulating Register (RCR). This is implemented using seven CD 4031, 64-stage Static Shift Registers. The data in this RCR corresponds to the subgroups of rows to be selected next. The mode-control and the clock for the CD 4031s are generated in the control logic.

The Sequence Generator is implemented using CD 4040, 12-stage Ripple-Carry Binary Counter/Divider and CD 4070, Quad Exclusive-OR Gate as shown in Fig.4.19. The output sequence corresponds to a 7-bit Gray code.

The Column Signal Generator (CSG) is implemented using CD 4070 and CD 4008, 4-Bit Full Adder. The 7-bit output from the RCR is compared bit-by-bit with the row-select pattern (RS0-RS6) using the Exclusive-OR gates. The number of errors (logic 1 at the output of the Exclusive-OR gate) is counted using two CD 4008 as shown in Fig.4.19. The unused input

of the adders are connected to logic 0 and it is important to note that all the inputs to these adders have equal weightage. The 3-bit output, viz., $X(n)$, $Y(n)$ and $Z(n)$ of the adder gives the number of errors (which ranges from 0-7 depending on the row-select pattern and the data to be displayed in a column of the selected sub-group).

The Column Driver consists of sixty-four CD 4051, Triple 2-Channel Analog Multiplexer/Demultiplexer and six HD 44100, LCD Driver with 40-channel outputs. It is important to note that the HD 44100s are used here only to serially shift in the data from the CSG and to latch them in parallel, using the shift register and the latch available in the HD 44100s. They are not used as LCD drivers since HD 44100 can switch only two voltage levels corresponding to the 1-bit data in the latch while the IHAT requires 8-voltage levels to be switched in this application as discussed earlier. The CD 4051 is used to switch one of the eight voltage levels (V_0-V_7) from the VLG.

The row-select pattern is level-shifted using CD 4054 to form the Row waveforms (RW6-RW0). These waveforms are applied to the selected subgroup of rows and their amplitude is either $-V_r$ or $+V_r$ depending on the row-select pattern. The row waveforms are synchronized with the column waveforms by latching the row-select pattern corresponding to the data in the column drivers into the CD-4054 simultaneously as the column data.

Twenty-one CD 4053, Triple 2-channel Multiplexer/Demultiplexer are used as Row Drivers (RD). The CD 4053 either connects one of the row waveforms (RW0-RW6) or the voltage level 'O' from the VLG depend-

ing on the control from the Sub-Group Sequencer (SGS). The rows in the selected subgroup are connected to the row waveforms, while the rows in the unselected subgroups are connected to the voltage level 0 as discussed in section 3.3.

The Sub-Group Sequencer (SGS) is implemented using CD 4017, Decade Counter/Divider with 10 Decoded Decimal Outputs. The SGS selects 1 of the 9- subgroup of rows. The SGS is synchronized with the address input of the memory, so that the data in the column drivers corresponds to the selected subgroup.

The ratio V_r/V_0 for $N = 63$ is calculated from eqn. (3.84). The relative magnitudes of the column voltage are as per eqn. (3.85) and are shown in Table 3.9. The VLG implemented using trimmed resistors, with their values accurate to ± 1 ohm is shown in Fig.4.19.

Some important signals generated in the Control Logic (CL) for a proper function of the various blocks in the display system are given below:-

-   12-bit address to the HN 462532 for reading the pixel information from the memory.

-   CL, the clock to CD 4031s.

-   MC, the mode control to the CD 4031s to load the data from HN 462532 or to recirculate the data in the CD 4031s.

-   CL2, to HD 44100s to serially shift in the data from the CSG.

-   CL1 to load the data into the latch of HD 44100.

-   Clock to the CD4040.

-   CLK, the clock to CD 4017 .

The CL is hard-wired for the following row-select sequence:-

-   Each sub-group is selected with four row-select patterns before the next sub-group is selected.

-   The subgroups are selected sequentially one after the other.

    The CL has flexibility (switch selectable) to change the four row-select pattern either when a new subgroup is selected or at the end of selecting all the nine-subgroups. The subgroups are selected each time for a duration of approximately .1 ms. Although the time required to complete a cycle is approximately 120 ms, no flicker is observed since the subgroups are selected after every 3.6 ms.

c) <u>Results</u>

The photograph of the 64 x 64 matrix TNLCD, addressed using IHAT are shown in Fig.4.20. The upper photograph in the figure illustrates the contrast variation in TNLCDs with the viewing angle as well as the intensity of light falling on it. The lower photograph in the same figure illustrates the brightness uniformity of the pixels in the display addressed with IHAT. Both the scanning sequences discussed above have resulted in a good pixel brightness uniformity. Typical addressing waveforms applied to the row and column of the matrix LCD as well as the waveforms across the ON and OFF pixels are shown in Fig.4.21. The rms voltage across the ON and OFF pixels were measured using HP3467A, a Logging multimeter capable of measuring true-rms voltage. Fig.4.22 gives the plot of rms voltage across the ON and OFF pixels vs. supply voltage. The theoretical curves of this plot are obtained by using eqns. (3.99) and (3.91). These curves are shown
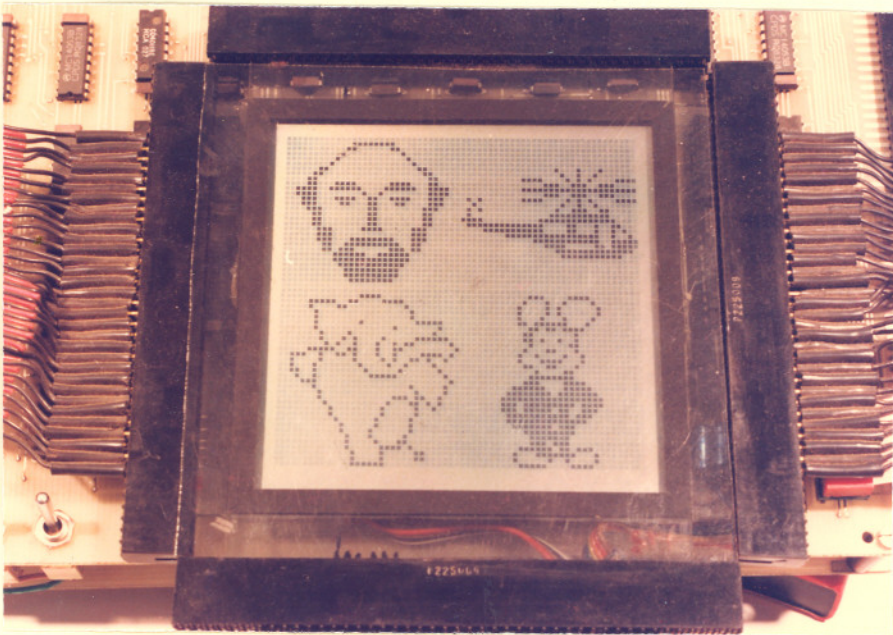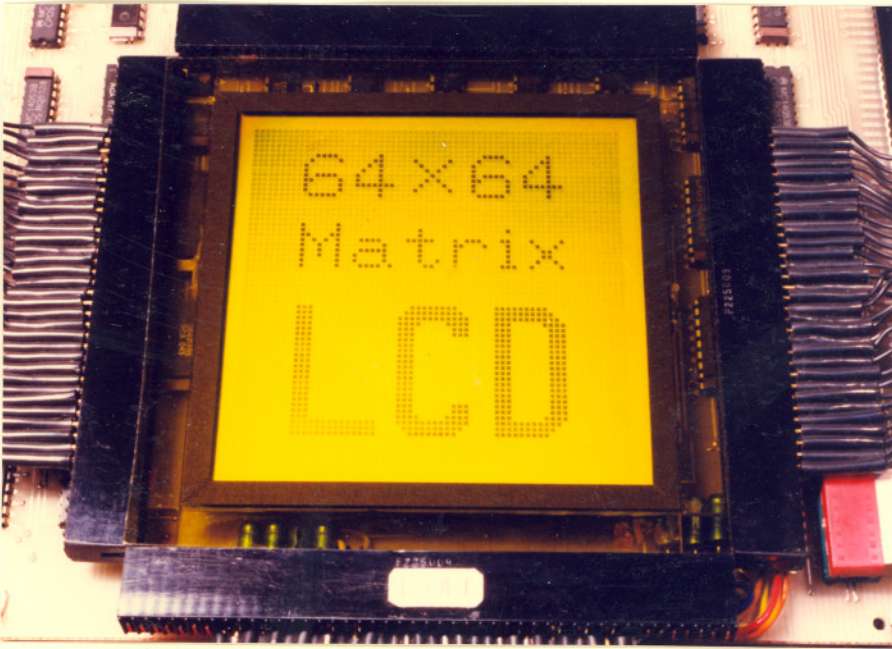
Fig. 4.20. Photographs of a display addressed with IHAT (N = 63 and ℓ = 7).

a) Typical row waveforms of IHAT .

b) Typical column waveform of IHAT .

Fig. 4.21.   Waveforms of IHAT when N = 63 and ℓ = 7 .
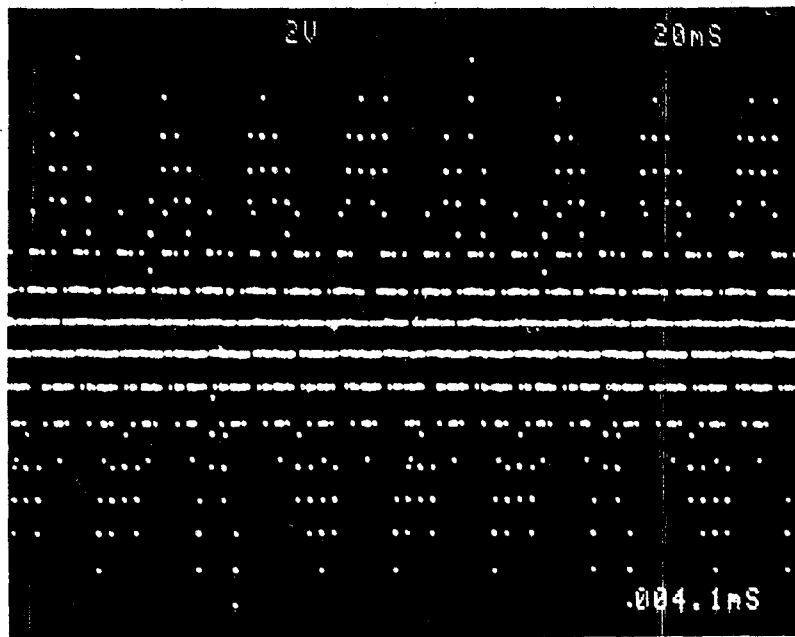
c) Typical waveform across an ON pixel in IHAT .
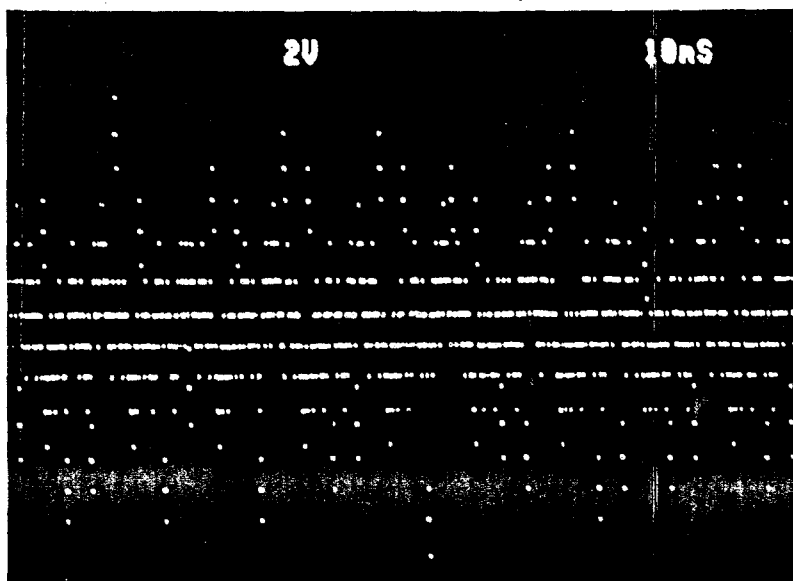
d) Typical waveform across an OFF pixel in IHAT .

Fig. 4.21.   Waveforms of IHAT when N = 63 and ℓ = 7 .

IHAT with N = 63, l=7
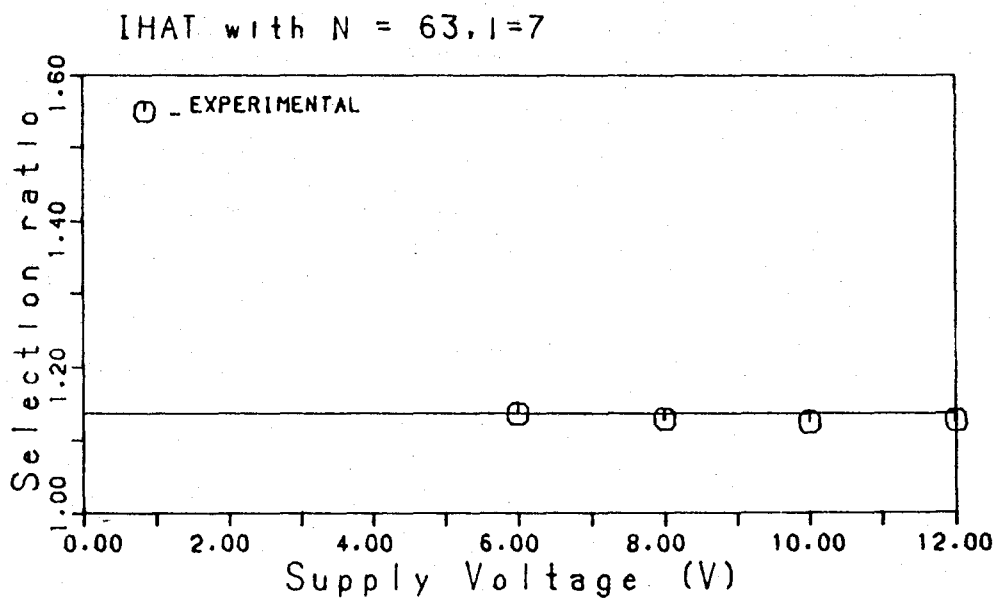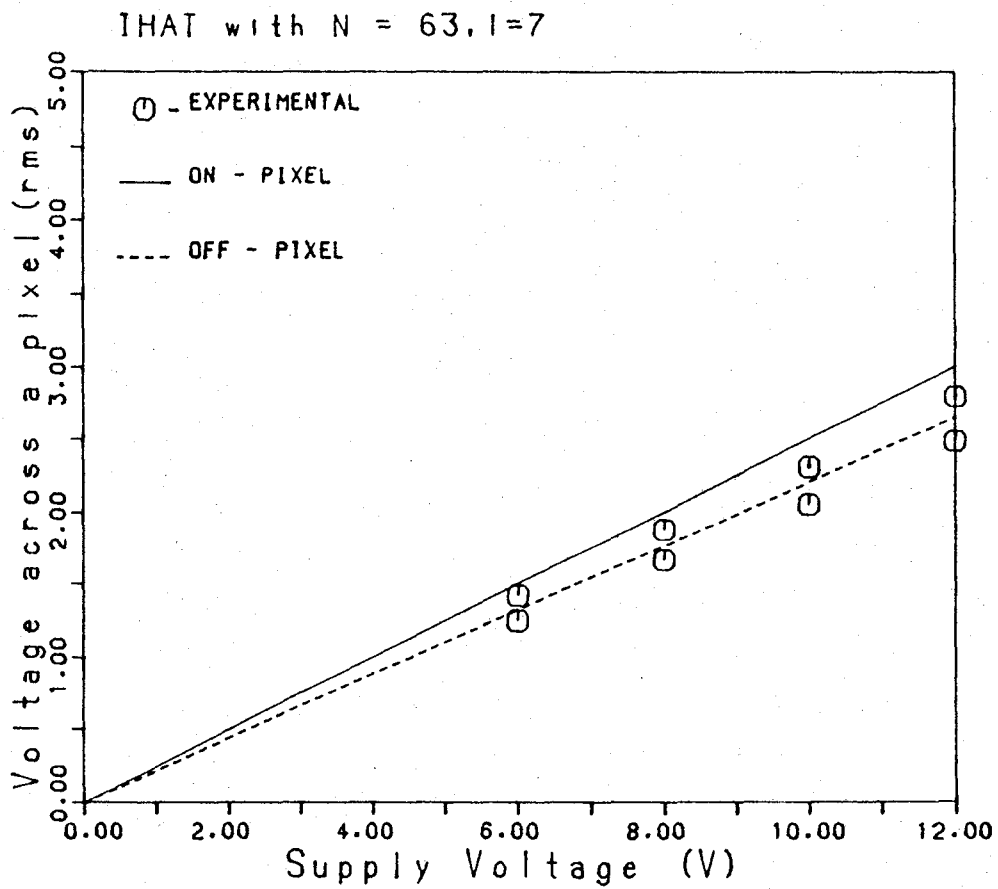
IHAT with N = 63, l=7

Fig. 4.22. Experimental results of IHAT, with N = 63 and l = 7 .

for comparison with the experimental results. The measured values of the rms voltage across the pixels are lower than the theoretical values. This may be attributed to the limited bandwidth of the measuring instrument. The value of the selection ratio obtained from the measurements agree with the theoretical value within ±1%, although the rms voltage across the ON and OFF pixels are lower than the theoretical values as shown in Fig.4.22.

4.2.4. IHAT-S4

The IHAT-S4 is demonstrated using a 64 x 64 matrix TNLCD.

a) _Display_

The specifications of the 64 x 64 matrix TNLCD are the same as that of the display used for the demonstration of IHAT. The value of l is chosen to be 7 so that the results of IHAT and IHAT-S4 can be compared. The value of N is again 63. The best possible value for N_{eq}, when $l = 7$ is (232N/215) as shown in Table 3.16. The selection ratio for N = 63 is 1.130, which is 99.5% of the maximum value possible (using IAPT or IHAT). However the supply voltage requirement of IHAT-S4 is 5.13 V_{th}, which is only 75.9% of that of IAPT (Table 3.18).

b) _Hardware_

The hardware realization of IHAT-S4 is the same as that of IHAT except for the following blocks:-

-    Column Signal Generator (CSG)

Apart from determining the number of errors as in IHAT, they are grouped as shown in Table 3.16. Fig.4.23.a gives the additional hardware to modify the CSG of IHAT for IHAT-S4 along with the truth table for the CSG.

- Column Drivers (CD)

The IHAT-S4 requires a 4-1 analog multiplexer as column driver while IHAT requires a 8-1 analog multiplexer.

- Voltage Level Generator (VLG)

The number of voltage levels required for the column drivers in IHAT-S4 is 4 as compared to 8 in the case of IHAT. The number of voltage levels in the row waveform is the same for both IHAT-S4 and IHAT. The ratio of the row to column voltage for optimum selection ratio is different for IHAT-S4 and is as given by eqns. (3.146) and (3.151). The VLG used for IHAT-S4 is given in Fig.4.23b.

The IHAT-S4 is implemented by duplicating the hardware used for IHAT (Fig.4.18). The VLG is implemented externally as shown in Fig.4.23b. The connections to the 8 inputs of the sixty-four CD 4051 (column drivers) as required for the simulation of IHAT-S4 using the PCB for IHAT is shown in Fig.4.23c. Thus, the same circuit can be used for both IHAT and IHAT-S4 by merely changing the VLG.

c) Results

Fig.4.24 gives a photograph of the 64 x 64 matrix TNLCD addressed with IHAT-S4. It was found that there is no appreciable change in the contrast ratio of the display compared to the display addressed with IHAT,

INPUT			OUTPUT	
X (n)	Y(n)	Z(n)	CS1	CS0
0	0	0	0	0
0	0	1	0	0
0	1	0	0	0
0	1	1	0	1
1	0	0	1	0
1	0	1	1	1
1	1	0	1	1
1	1	1	1	1
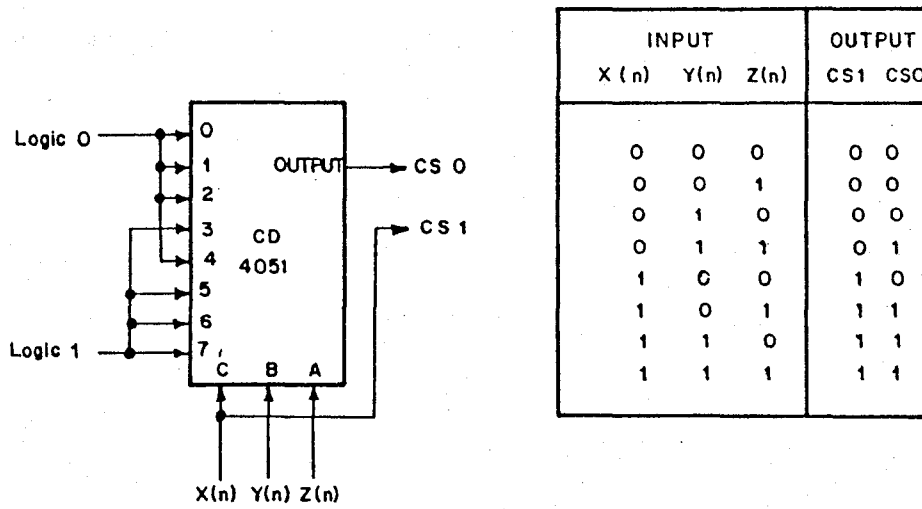
Fig. 4.23 a. Additional circuit when 4:1 multiplexers are used as column drivers.
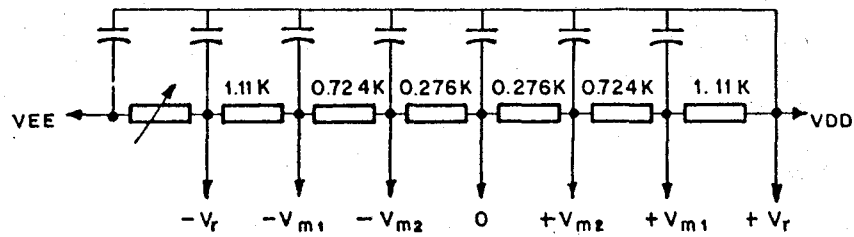
Fig. 4.23 b. Voltage Level Generator (VLG) for IHAT - S4.
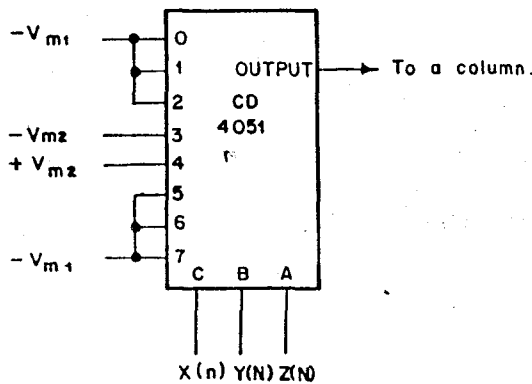
Fig. 4.23 c. Connection to the column drivers when IHAT - S4 is simulated with IHAT Hardware.
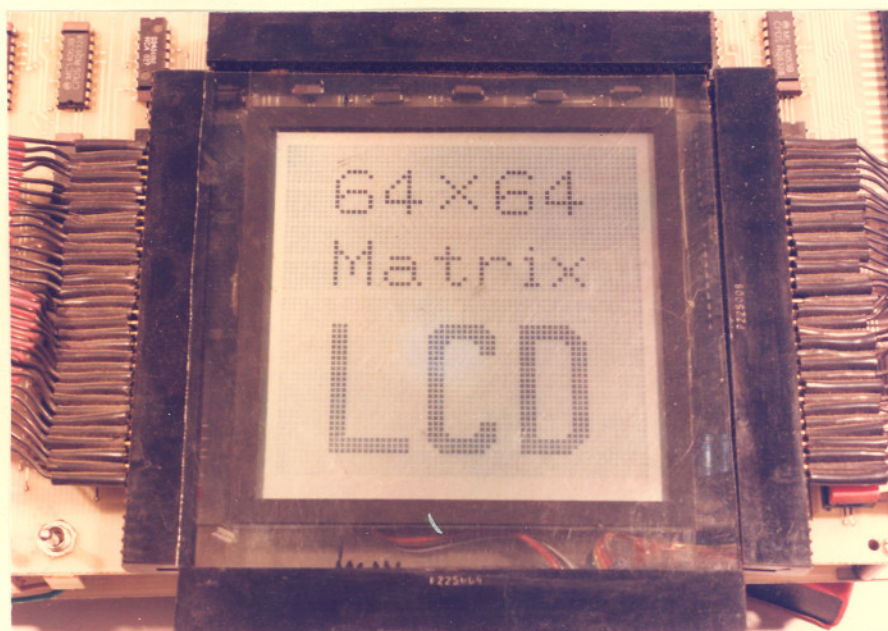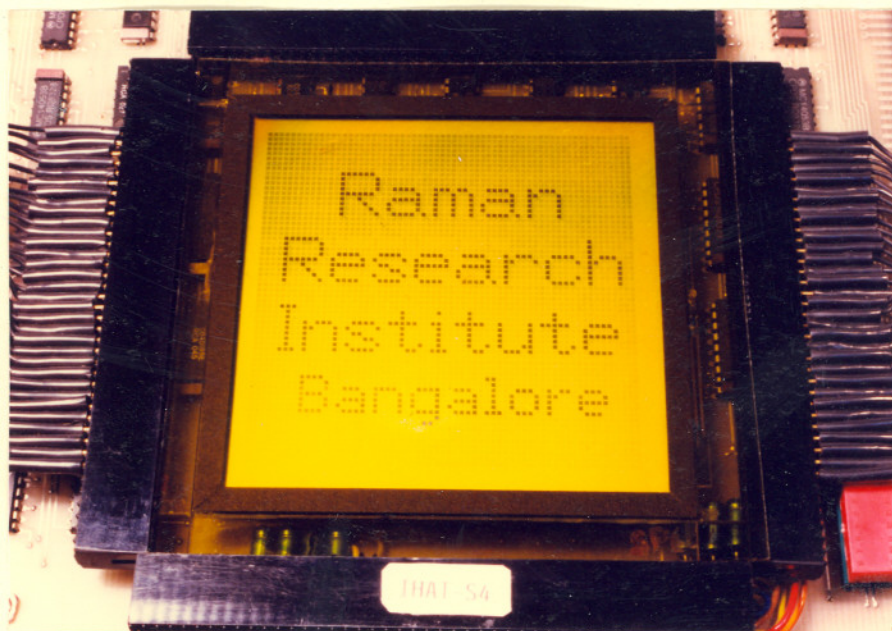
Fig. 4.24. Photographs of a display addressed with IHAT-S4
(N = 63 and l = 7).

this is in agreement with the analysis of section 3.4. Although the supply voltage of IHAT-S4 is slightly higher than that of IHAT, the IHAT-S4 retains the lower power supply voltage requirement as compared to IAPT (75.9% of IAPT). The V_{supply} of IHAT-S4 is 5.13 V_{th} (Table 3.18) as compared to 4.538 V_{th} (eqn. 3.99) of IHAT, i.e., 13% higher than that of IHAT. The variation of contrast in TNLCD with viewing angle and the intensity of light incident on it is shown in upper photograph of Fig.4.24. The brightness uniformity of pixels addressed with IHAT-S4 is illustrated in the lower photograph of the same figure. The brightness uniformity of the pixels in the display addressed with IHAT-S4 is good, as can be seen from the photograph at the bottom of Fig.4.24. Thus, nearly a 50% reduction in the hardware in IHAT-S4 by using 4:1 multiplexers (instead of 8:1 in the case of IHAT) does not significantly alter the performance of the display system as compared to IHAT. Typical addressing waveforms as well as the waveforms across the ON and OFF pixels of this display addressed with IHAT-S4 are shown in Fig.4.25. The rms voltage across the ON and OFF pixels were measured using HP 3467A logging multimeter. Fig.4.26 gives the plot of the V_{ON} (rms) and V_{OFF} (rms) for various values of the supply voltage. The theoretical curves of the same arrived at by using eqns. (3.153) and (3.161) are also presented for a comparison. The measured value of the rms voltage across the pixels is lower than the theoretical value as in the case of IHAT. This may be attributed to the limited bandwidth of the measuring instrument. The selection ratio obtained from the measurement agrees within ±1% of the theoretical value of 1.130, although the rms voltage across the ON and OFF pixels are lower than the theoretical values as shown in Fig.4.26.
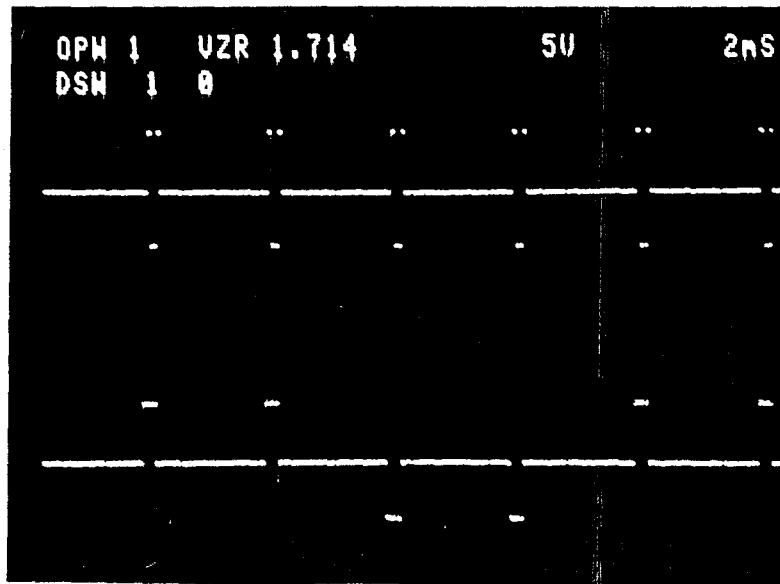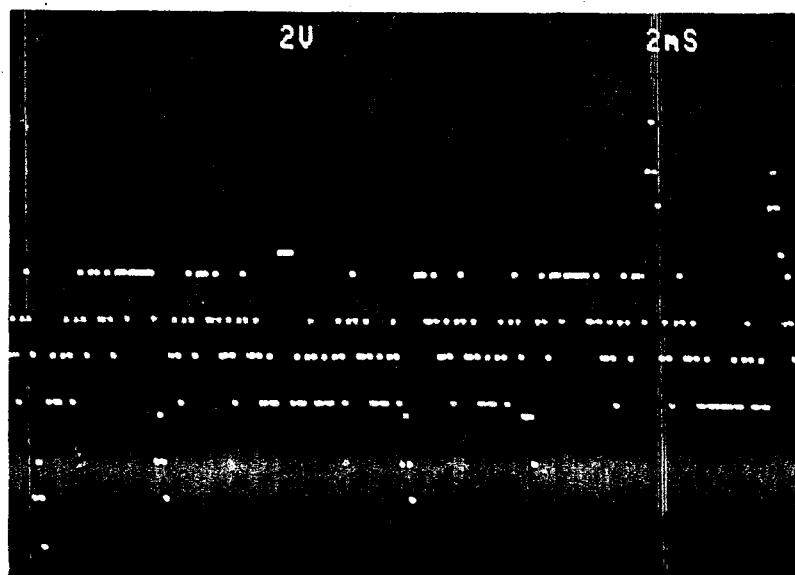
a) Typical row waveforms of IHAT - S4 .
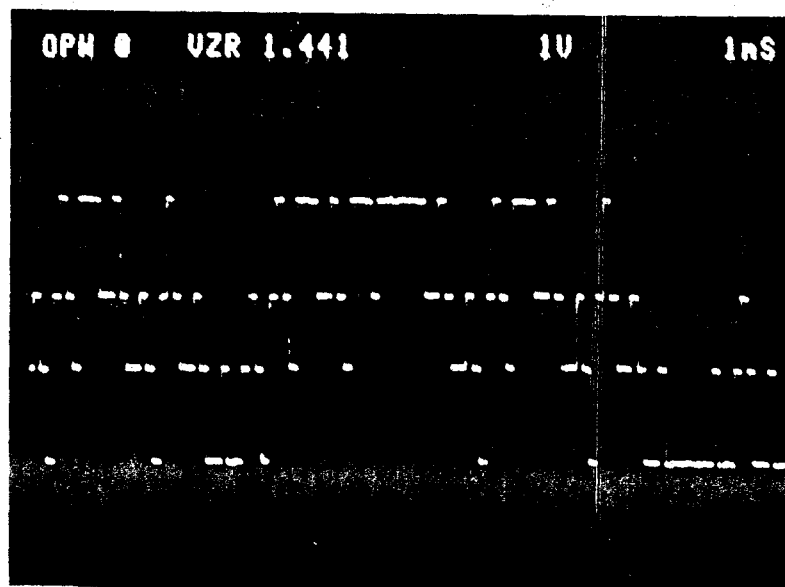
b) Typical column waveform of IHAT - S4 .

Fig. 4.25. Waveforms of IHAT-S4 when N = 63 and ℓ = 7 .
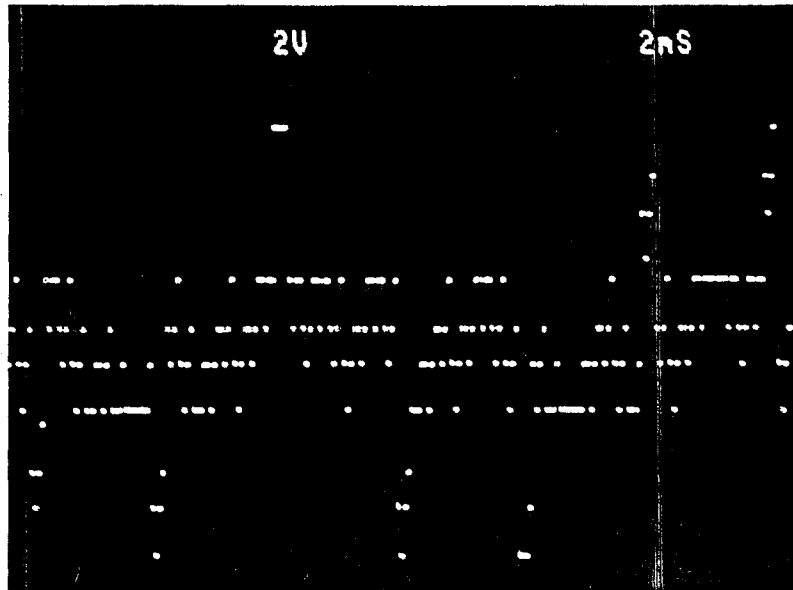
c) *Typical waveform across an ON pixel in IHAT-S4 .*

d) *Typical waveform across an OFF pixel in IHAT-S4 .*

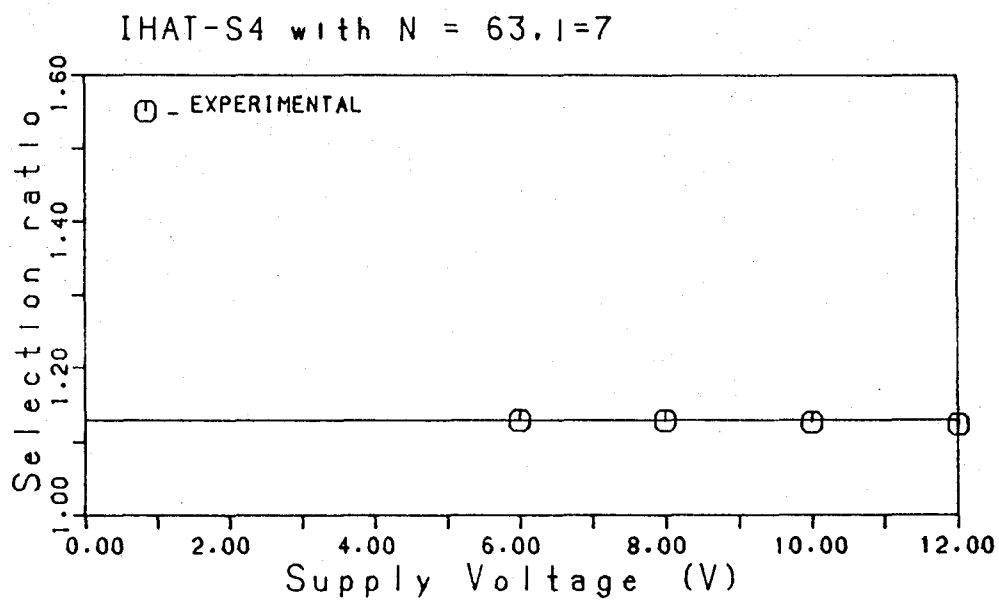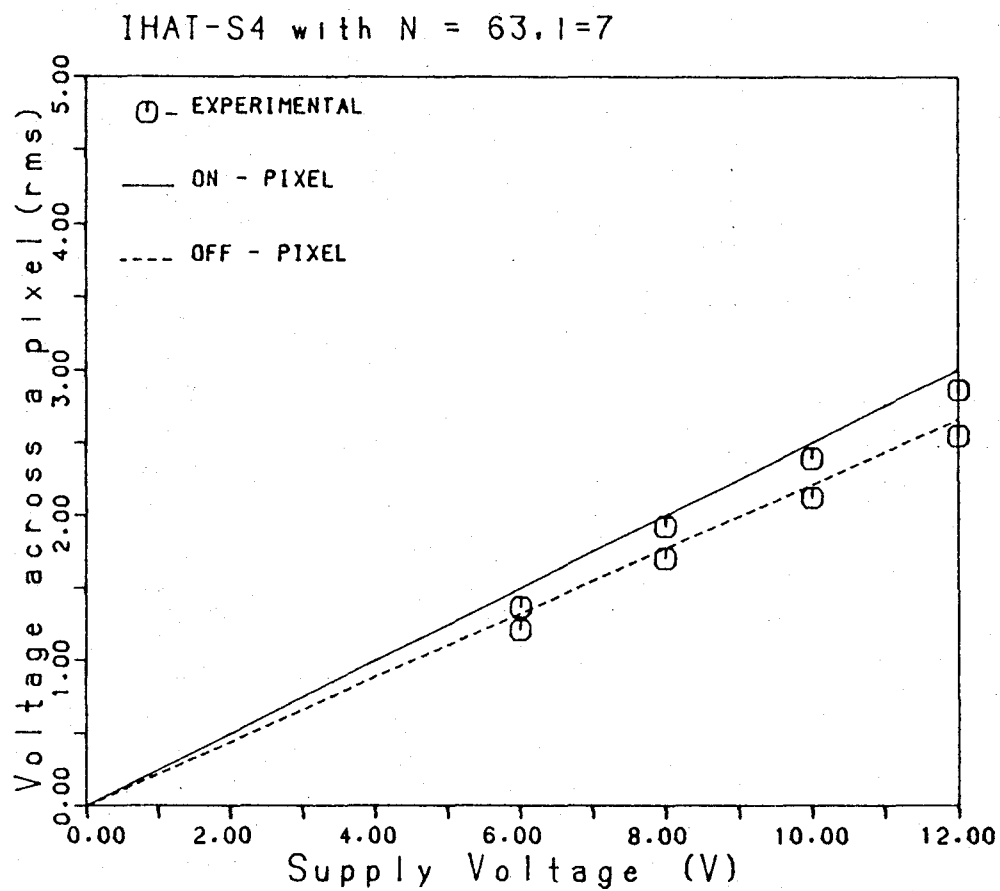*Fig. 4.25.* *Waveforms of IHAT-S4 when N = 63 and ℓ = 7 .*

IHAT-S4 with N = 63, I=7

IHAT-S4 with N = 63, I=7

Fig. 4.26. Experimental results of IHAT-S4, with N = 63 and l = 7.

4.2.5 RPAT-NC

The RPAT-NC is demonstrated by displaying multiple waveforms using a 64 x 64 matrix TNLCD.

a) Display

The physical specifications of the 64 x 64 matrix display are the same as that of the display used to demonstrate IHAT. The specifications of the P23 + N23 (50:50), a commercial NLC mixture (Chisso Corpn., Japan) used in the display are given below:-

- Threshold voltage (V_{th}) : 1.5 V
- Saturation voltage : 2.0 V
- Sharpness parameter : 13%
- Rise time : 75 ms
- Fall time : 60 ms.

The technique is demonstrated by displaying 4-waveforms (N_{eq} = 9 from eqn.3.169) and a single waveform along with legends (N_{eq} = 21.69 from eqn. 3.169). The selection ratios for these two cases are obtained using eqn. (3.167) and are 1.414 and 1.244 respectively. It is evident from the specifications of the NLC mixture that the value of the sharpness parameter is adequate for the present applications.

b) Hardware

A detailed block diagram of the Display system using RPAT-NC is shown in Fig.4.27. The Bit-Mapped Memory (BMM) is implemented using HN 462532, a 4K x 8-bit UV-EPROM. The pixel information is stored row-wise in the successive bytes of this memory. An EPROM is used here since the
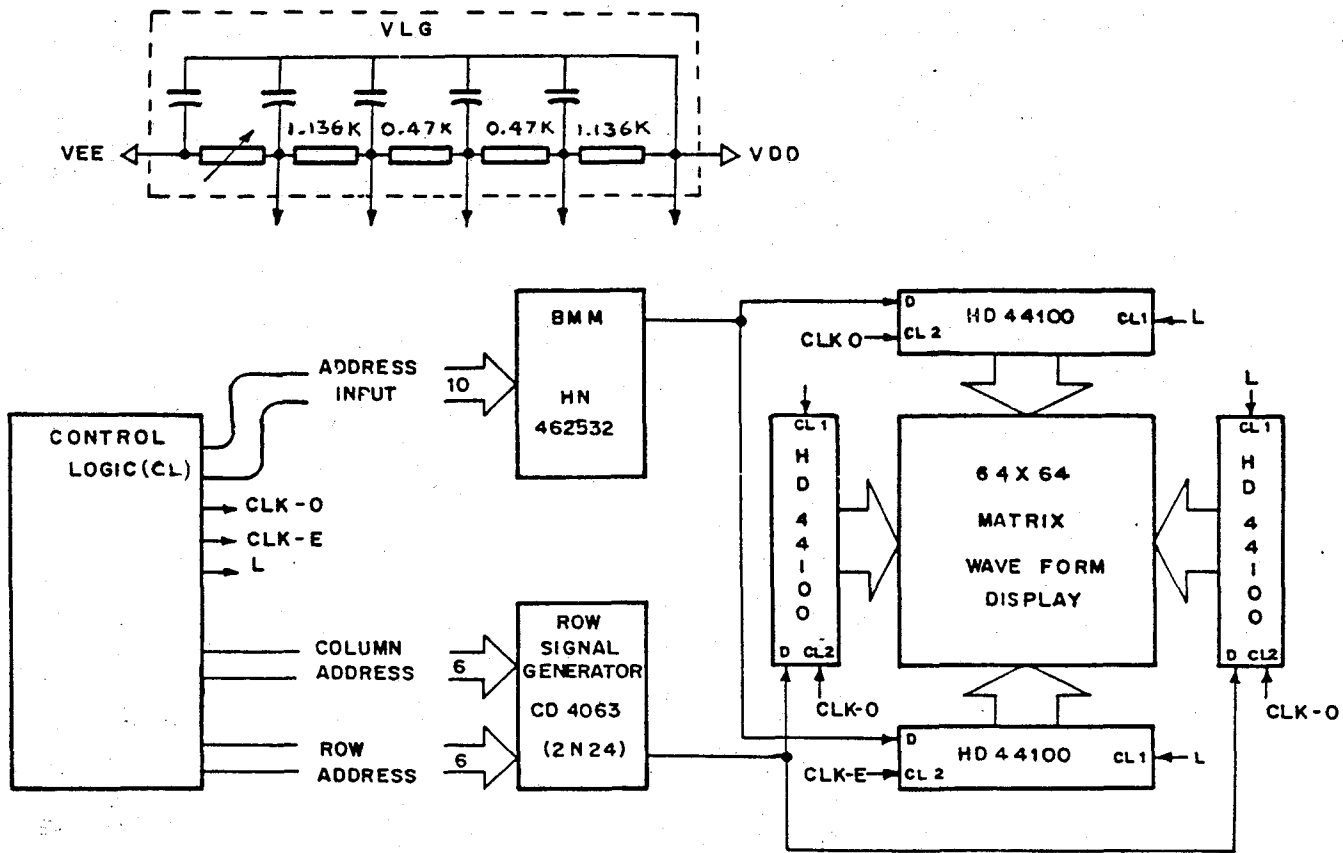
Fig. 4.27. Schematic of a display system using RPAT - NC.

display system is designed to demonstrate the usefulness of the RPAT for displaying the waveforms (restricted pattern) in an oscilloscope. However, the BMM should be implemented using RAM along with the front-end for acquiring the signals as discussed in section 4.1. The data in each byte of HN 462532 corresponds to 8 columns in a row. Hence, the first 3-bits of the address input are used for accessing the pixel information corresponding to a single row. The next 6-bits of the address input correspond to the 64-rows in the matrix display. The rest of the 3-bits in the address input are used to select one of the 8-frames stored in the EPROM. The data stored in the first 4-frames have four traces and the rest of the 4-frames have a single waveform along with legends.

The 8-bit parallel data from the HD 462532 are converted to serial form using CD 4014, an 8-stage synchronous shift register with parallel or Serial Input/Serial Output. The row and column drivers are implemented using HD 44100, an LCD driver with 40 channel outputs. The schematic diagram of the HD 44100 is shown in Fig.4.8.

The display system is designed for displaying 4-waveforms or a single waveform along with legends as shown in Fig.4.28. Although the V_{supply} is independent of the number of waveforms displayed as given by eqn. (3.175), the value of the ratio V_r/V_c depends on the value of W (number of waveforms displayed) as given by eqn. (3.163). The legends in the display are equivalent to 7- additional waveforms since additional 7-pixels are selected in each column as discussed in chapter 3. The optimum values for the ratio V_r/V_c are 2 and $8^{1/2}$ for displaying 4-waveforms and a single waveform with legends respectively as given by eqn. (3.163). The VLG shown in Fig.4.27 generates all the voltage levels required for displaying the wave-

forms without any dc across the pixels. A common VLG is possible here for displaying 4-waveforms and a single waveform with legends since the supply voltage required is the same for both in RPAT-NC. The appropriate voltage levels are connected to the display drivers, depending on the number of waveforms to be displayed by using CD 4053, a Triple 2-channel Multiplexer/Demultiplexer.

The display is refreshed at a rate of 25 Hz which is quite adequate to ensure an rms response and a flicker-free operation. The brightness uniformity of the pixels was found to be poor when a single waveform along with legends was displayed. However a good improvement in the brightness uniformity of the pixels was observed when the following modification was incorporated in the scanning circuit. The row address lines from the counter CD 4520 are scrambled so that the rows in the display are selected in the following sequence 1, 33, 17, 49, 2, 34, 18, 50, ... etc., instead of the natural sequence 1,2,3,4,5,6,7.... etc. The improvement in the brightness uniformity of the pixel is due to the following reason:-

-    The column voltage across the pixels (corresponding to the selected pixels in the column) are distributed more uniformly with the new sequence as compared to the natural sequence of row selection. Two CD 4063, 4-bit magnitude comparators are used to generate the row-select signal to the row drivers.

The Control Logic is implemented using CD 4047 (Low-Power Monostable/Astable Multivibrator), CD 4518 (Dual BCD up counter) and CD 4081 (Quad 2-Input AND Gates).

c) _Results_

The photographs of the 64 x 64 matrix TNLCD, addressed using RPAT-NC and the typical addressing waveforms (when W = 4) are shown in Figs. 4.28 and 4.29 respectively. The rms voltages across the pixels were measured using HP 3467A, a Logging multimeter capable of measuring true-rms voltages. Fig. 4.30 and Fig. 4.31 gives the rms voltages across the **ON** and **OFF** pixels. The theoretical curves shown are obtained by using eqns. (3.164) and (3.165). The selection ratio obtained from the measurements agree with the theoretical value within ± 1%.

4.2.6 **RPAT-PC**

The RPAT-PC is demonstrated by displaying multiple waveforms using a 64 x 64 matrix TNLCD.

a) _Display_

A display with the same specifications as that of the display addressed with RPAT-NC is used here for a comparison. The N_{eq} is obtained using eqn. (3.178) and the values are respectively 25 and 44.3 when 4-waveforms and a single waveform with legends are displayed. The selection ratios for these two cases are 1.225 and 1.163 respectively. It is evident from the specifications of the NLC mixture that the value of the sharpness parameter is adequate for the present application.

b) _Hardware_

The RPAT-PC differs from the RPAT-NC only in the phase of the column voltage applied to a selected pixel, with reference to the row-select
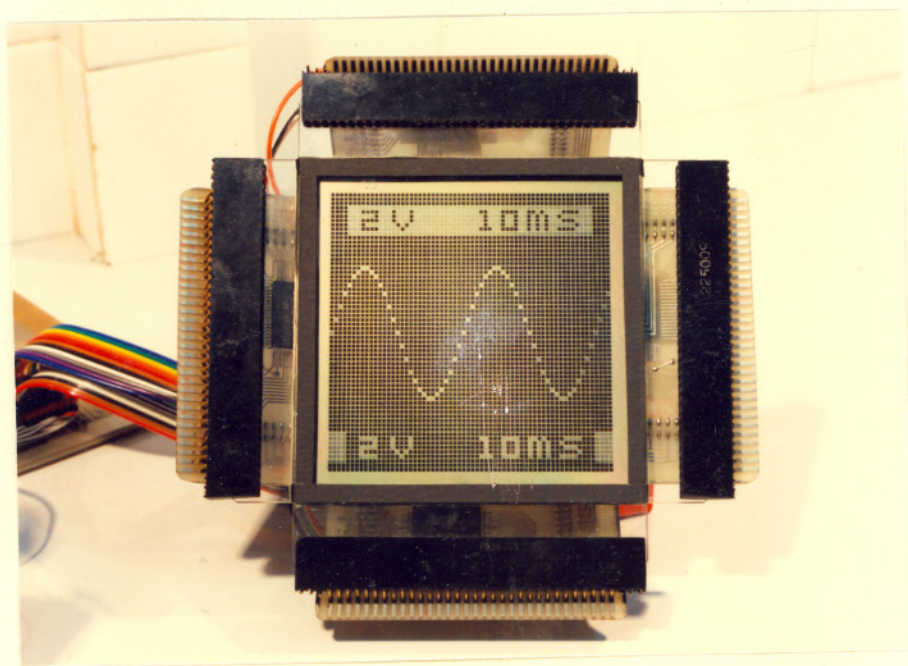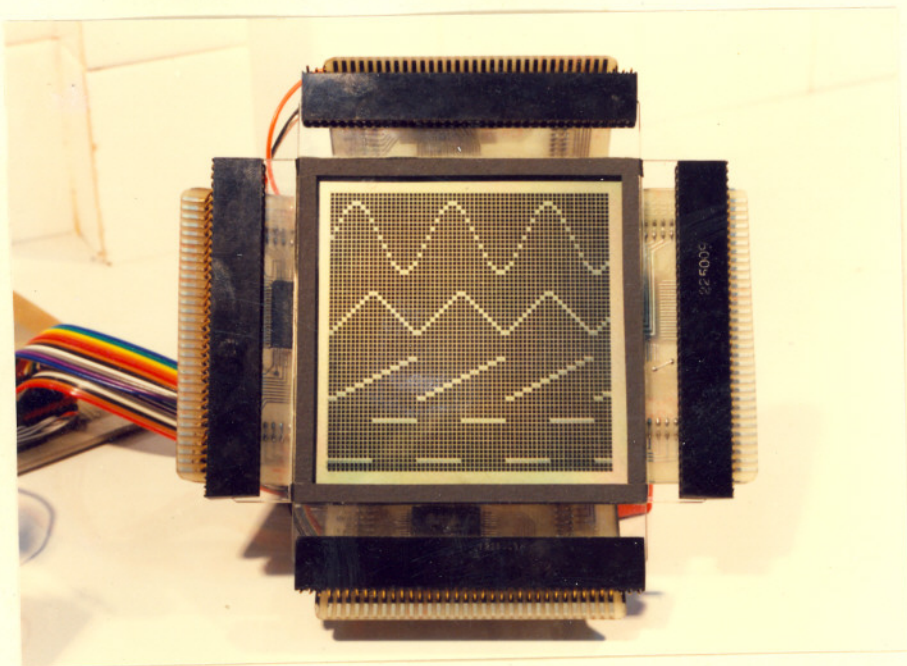
Fig. 4.28. Photographs of a display addressed with RPAT-NC.
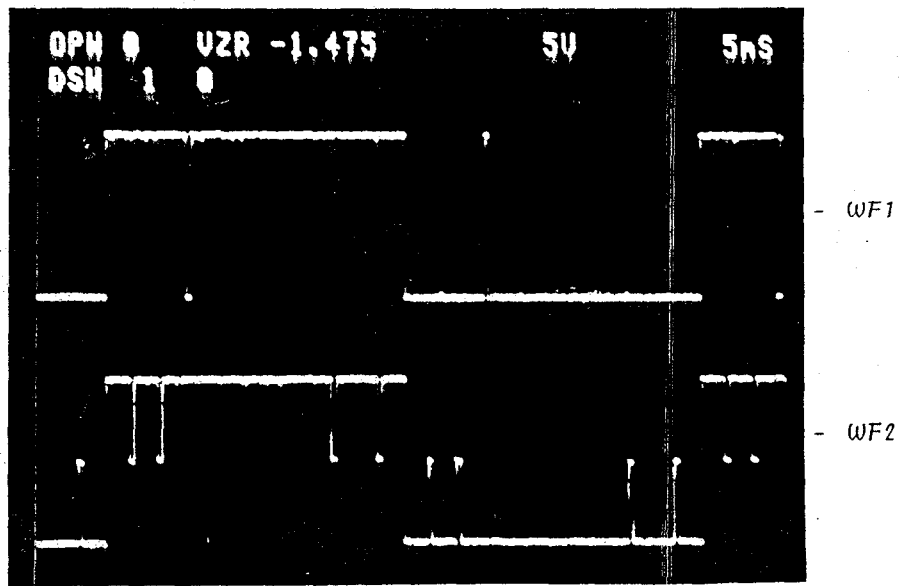
a) Typical addressing waveforms. WF1 - row and WF2 - column.
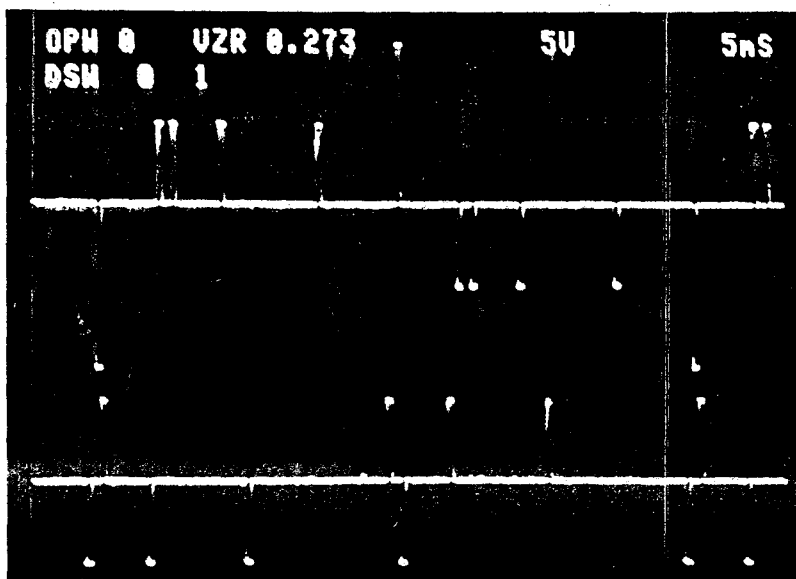
b) Typical waveforms across pixels. WF3 - ON and WF4 - OFF .
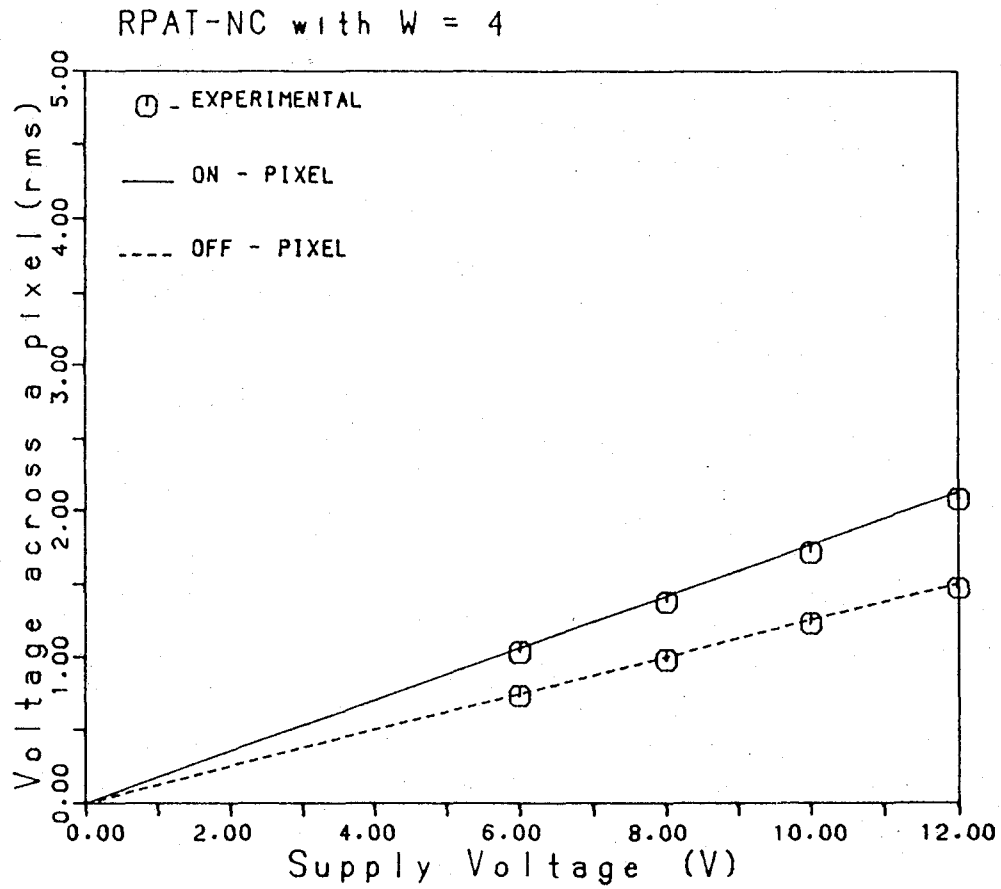
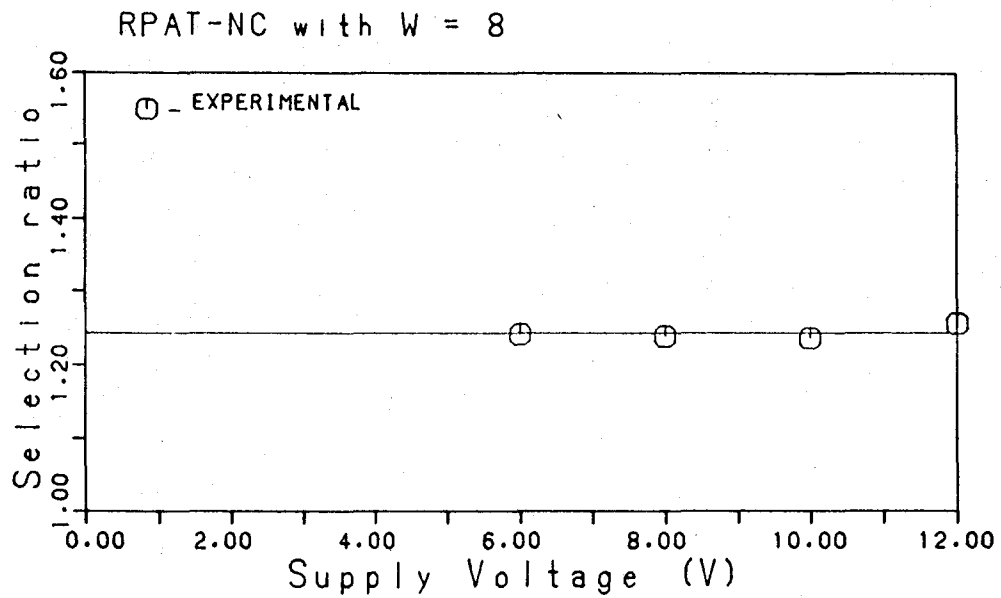Fig. 4.29. Waveforms of RPAT-NC when W = 4 .

RPAT-NC with W = 4
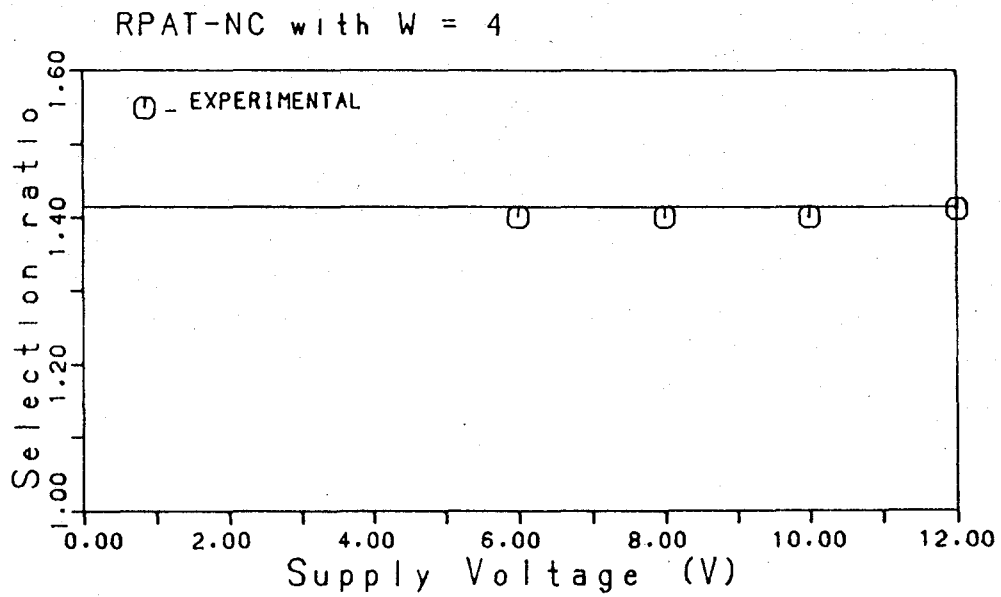
RPAT-NC with W = 4

Fig. 4.30. Experimental results of RPAT-NC with W = 4.

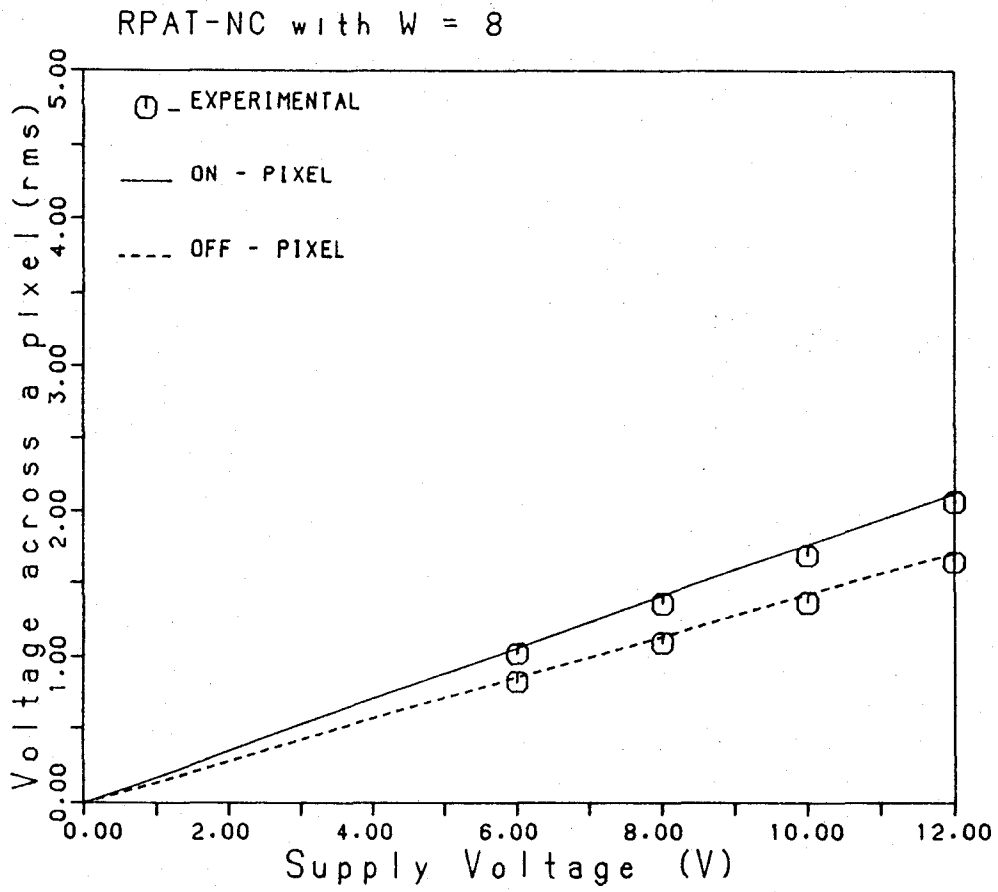RPAT-NC with W = 8

RPAT-NC with W = 8

Fig. 4.31. Experimental results of RPAT-NC with W = 8 .

voltage. Hence RPAT-PC is implemented by duplicating the hardware used for RPAT-NC except for the Voltage Level Generator (VLG). The two VLGs required for displaying the 4-wave forms and a single waveform with legends are shown in Fig.4.32. A CD 4053, Triple 2-Channel Multiplexer/Demultiplexer is used here for selecting the appropriate voltage level depending on the number of waveforms to be displayed.

The display is refreshed at 25 Hz which is quite adequate for ensuring an rms response and flicker free operation. The row scanning sequence used here is the same as that of the display addressed with RPAT-NC.

c) Results

The photographs of the 64 x 64 matrix TNLCD, addressed using RPAT-PC are shown in Fig.4.33. The photographs of the typical addressing waveforms when W = 4 are shown in Fig.4.34. The voltages across the pixels were measured using HP 3467A, a Logging multimeter capable of measuring true-rms voltage. Fig.4.35 and Fig.4.36 shows the plot of the rms voltages across the **ON** and **OFF** pixels Vs. supply voltage. The theoretical curves are obtained using eqns. (3.182) and (3.177) and are shown for a comparison with the experimental results. The values of the selection ratio obtained from the measurement agree with the theoretical values within ±1%. Photographs of the displays with similar specifications and addressed with RPAT-PC and RPAT-NC respectively are shown in Fig. 4.37 for a comparison.

In summary, the implementation of the addressing techniques have been discussed in this chapter. The experimental results obtained using these techniques agree well with those of the theoretical analysis given in Chapter 3. In the following chapter, a critical analysis of the techniques proposed in this thesis and their impact are discussed.
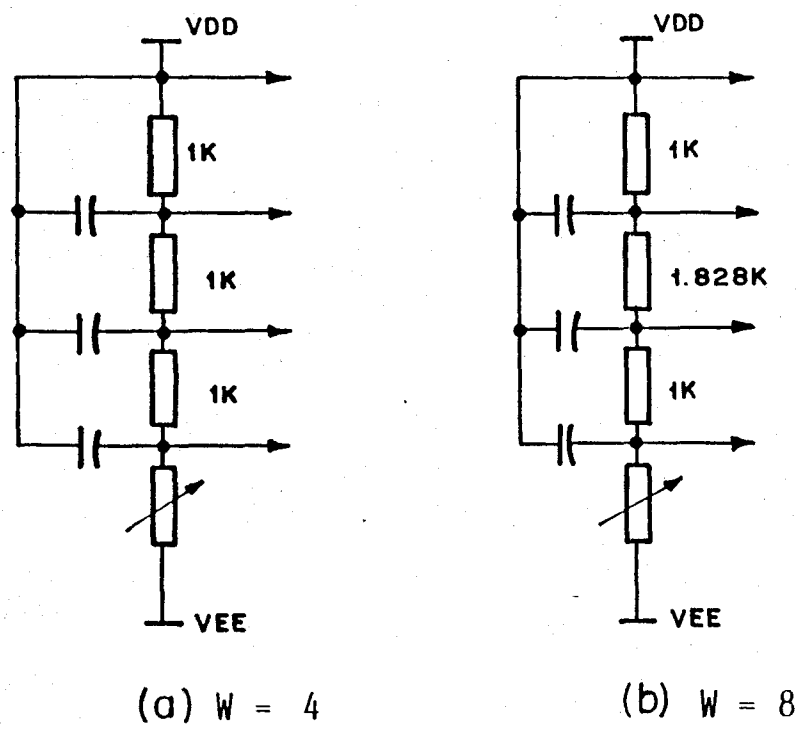
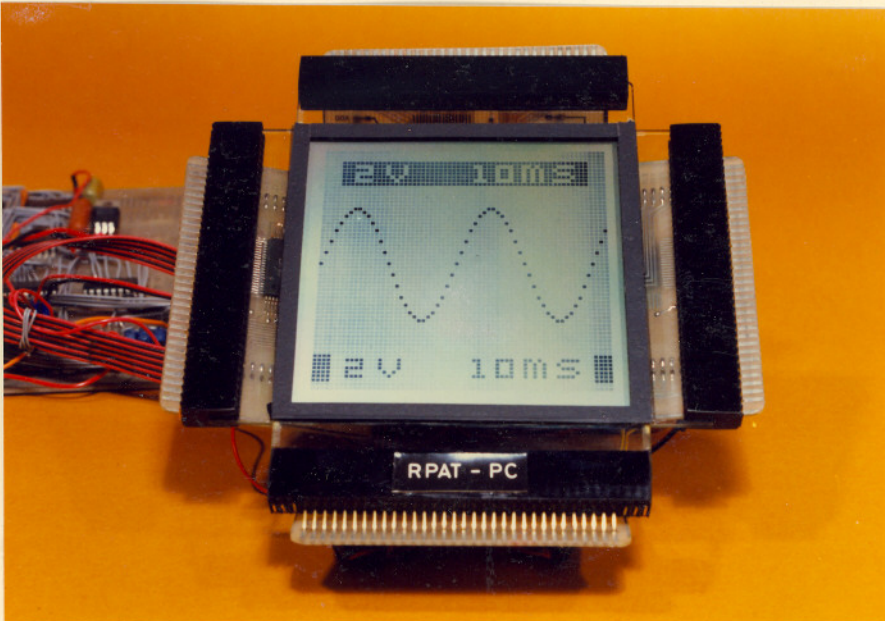(a) W = 4   (b) W = 8

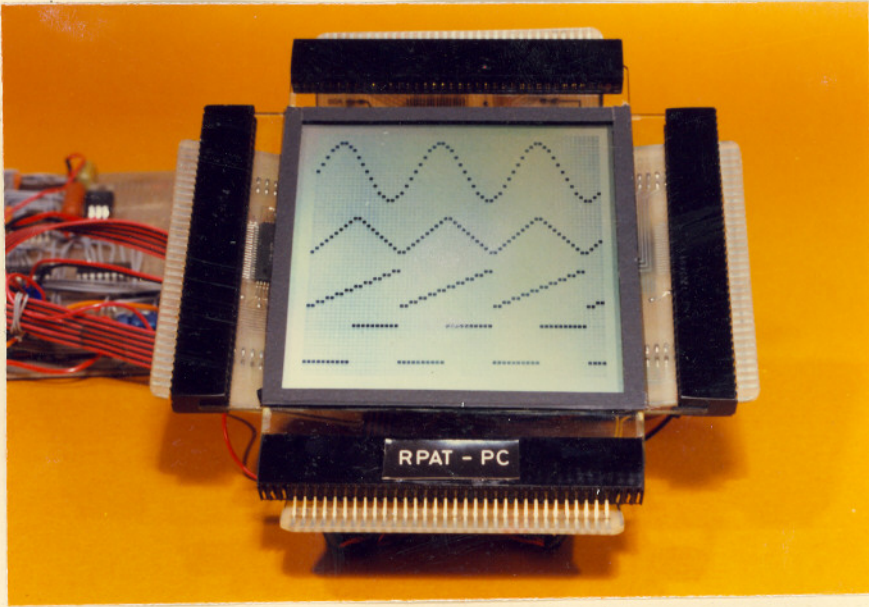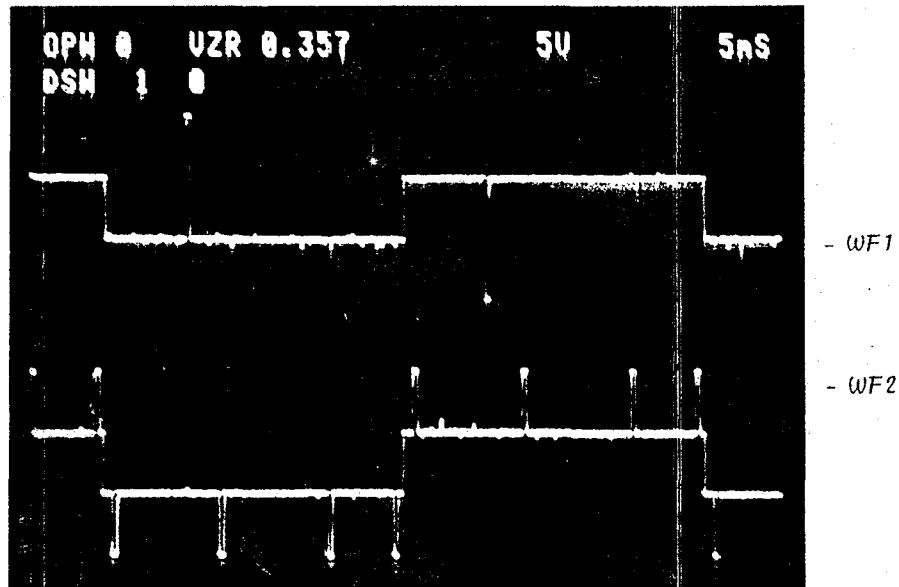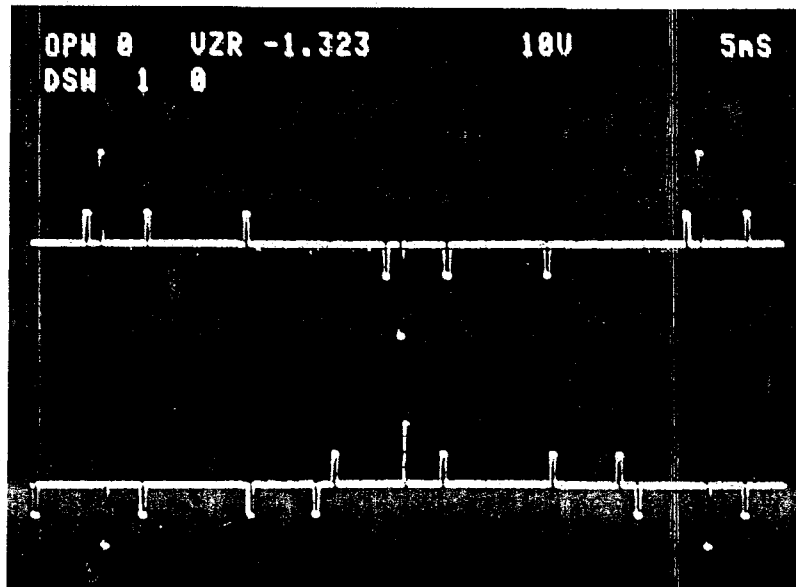*Fig. 4.32.*   *ULGs of RPAT - PC .*

Fig. 4.33. Photographs of a display addressed with RPAT-PC.

a) Typical addressing waveforms. WF1 - row and WF2 - column.

b) Typical waveforms across pixels. WF3 - ON and WF4 - OFF.

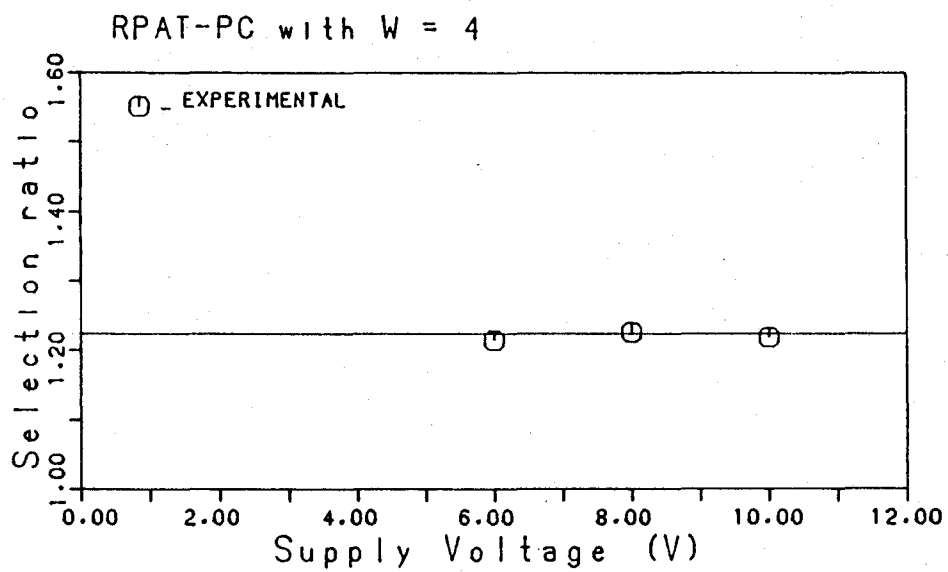*Fig. 4.34. Waveforms of RPAT-PC when W = 4 .*
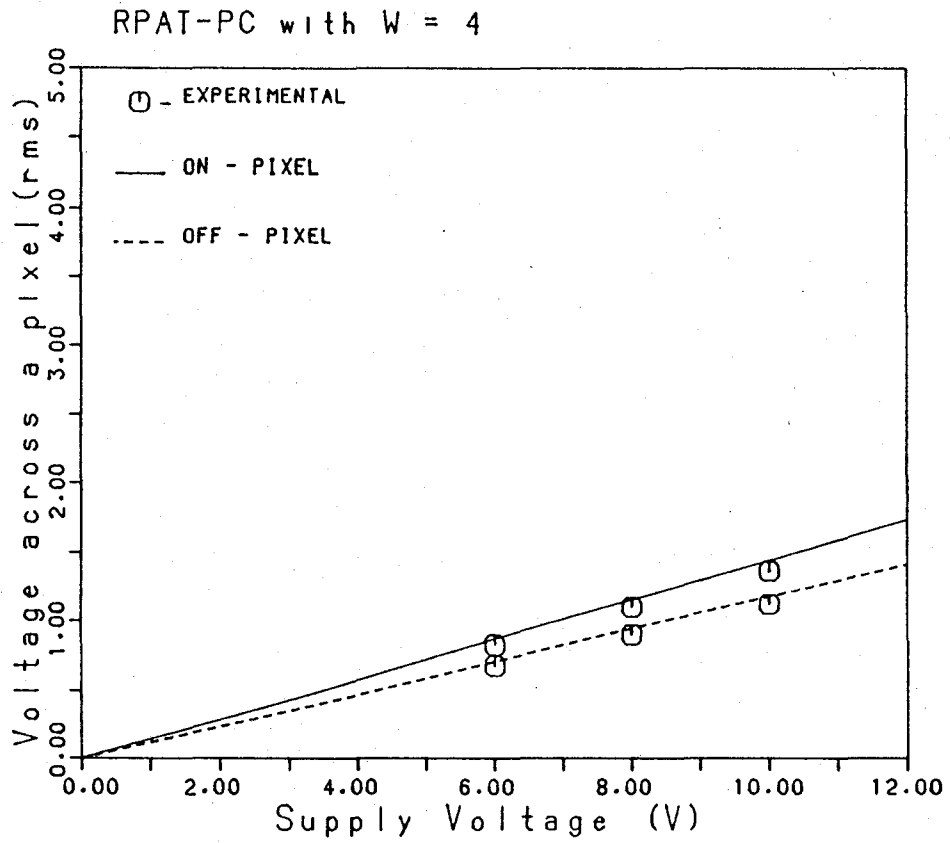
RPAT-PC with W = 4

RPAT-PC with W = 4

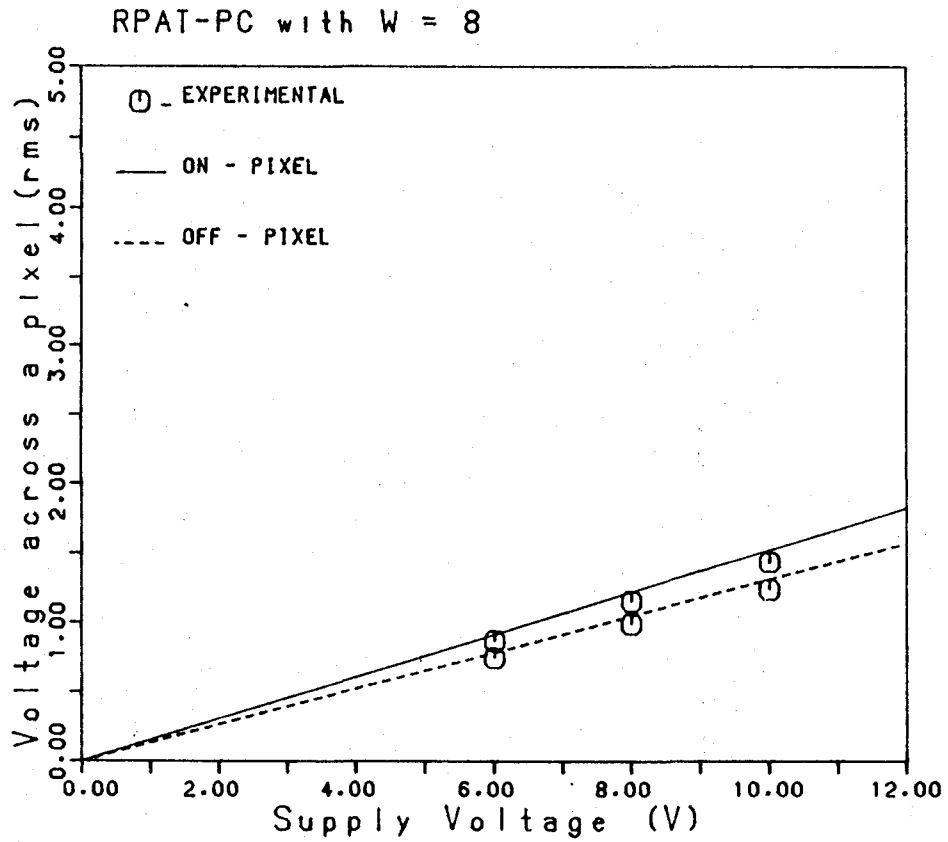Fig. 4.35. Experimental results of RPAT-PC with W = 4.
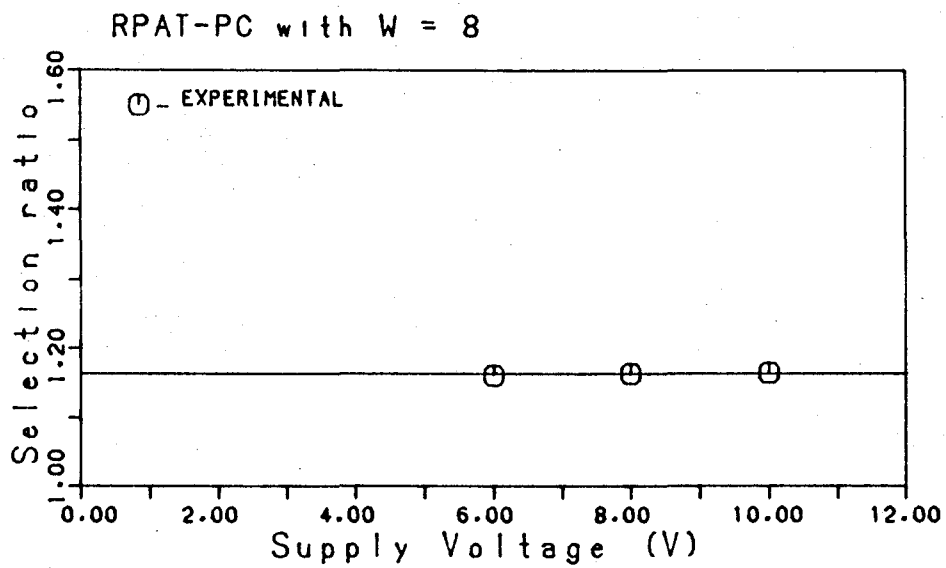
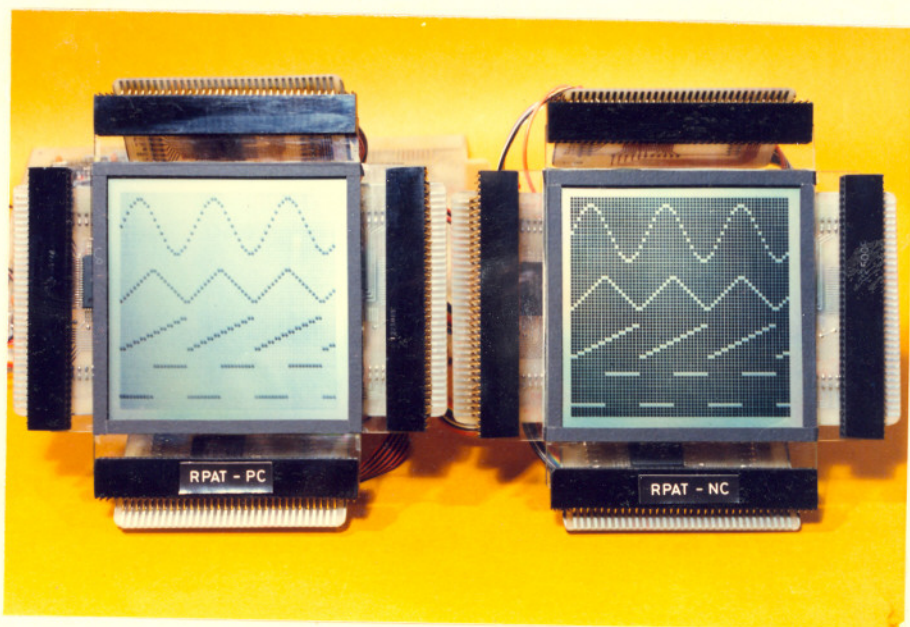Fig. 4.36. Experimental results of RPAT-PC with W = 8.

Fig. 4.37. Photograph of displays addressed with RPAT-PC and RPAT-NC for a comparison.