CHAPTER 6

SYSTEM TESTING

6.1 Introduction

The performance of the digital correlation receiver for the decametrewave radio telescope at Gauribidanur, whose detailed design has been discussed in the preceding chapters, was tested first in the laboratory and then on the field. The laboratory tests on the subsystems of the receiver were carried out, as described in Sec. 6.2 under Controlled Conditions and the performance was found to be satisfactory.

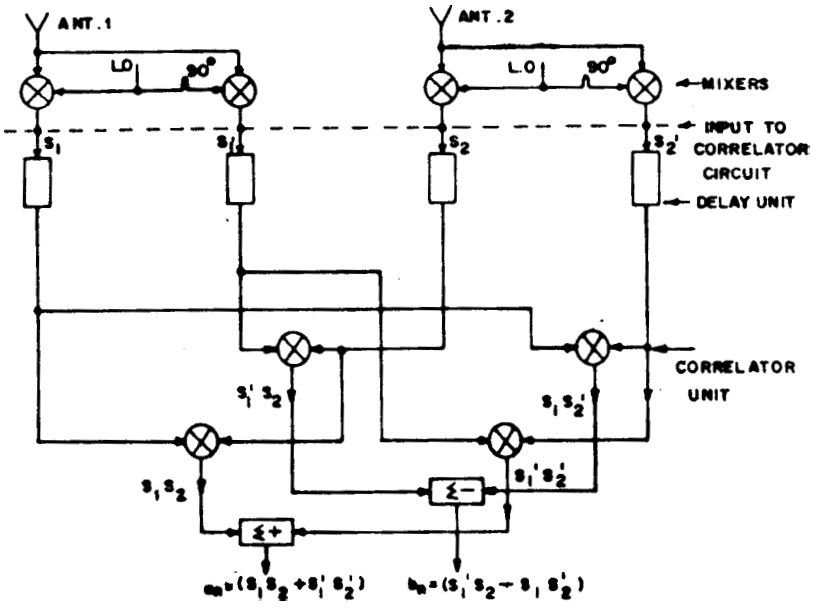
The field trial of the system was carried out by connecting the receiver system to the antenna system and obtaining tee system response for two strong radio sources, 3C144 and 3C218. The details of this test are discrssed in Sec. 6.3 below.

Both the laboratory tests and the field trials have shown that the system works satisfactorily as per the design.

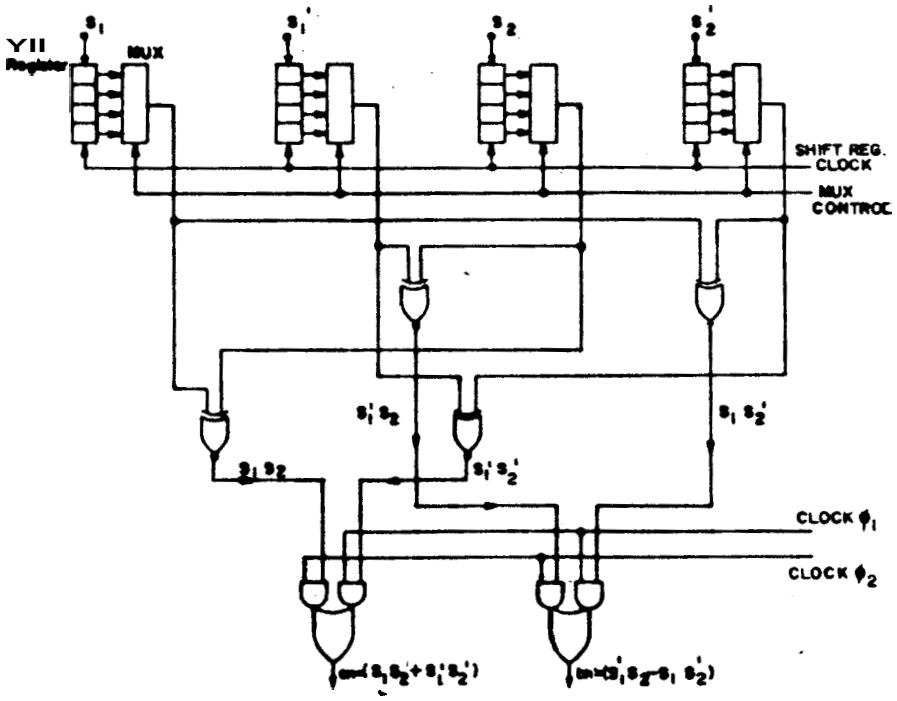
6.2 Laboratory tests

6.2.1 Tests on the Digital Correlator Circuit

As already discussed in Chapter 3, one-bit correlators and two adders (Ref. Fig. 6.1) are used



(A) SCHEMATIC OF CORRELATOR CIRCUIT.



F16.6.1 CORRELATOR CIRCUIT FOR DOUBLE SIDE-BAND SIGNALS.

for correleating double sideband signals directly without unfolding the signals. It may be recalled that the Cosine (a_n) and Sine (b_n) correlation coefficients are given by

$$\left.\begin{aligned} a_n &= S_1S_2 + S_1'S_2' \\ b_n &= S_2S_1' - S_1S_2' \end{aligned}\right\} \quad \text{Equation (7.4) Chap. 3}$$

The correlator circuit was first tested by giving all the possible combinations of the logic levels of the inputs S_1, S_2, S_1' and S_2' and monitoring the outputs a_n and b_n. As each of these four inputs can assume independently the logic levels 0 and 1, there are in all 16 possible combinations. This test indicated that the Correlator Circuit functioned as expected under static conditions.

To determine the effect of propagation delays in all the digital circuits in the four different signal paths, on the Correlation Coefficients, a_n and b_n, a noise source was used as shown in Fig. 6.2. The noise source was followed by a bandpass filter, BPF, of 600 KHz bandwidth at centre frequency of 4 MHz. BPF was followed by a zero-cross detector (ZCD) circuit to provide the one-bit signal of the noise input. Bandpass sampling was employed. The output of the

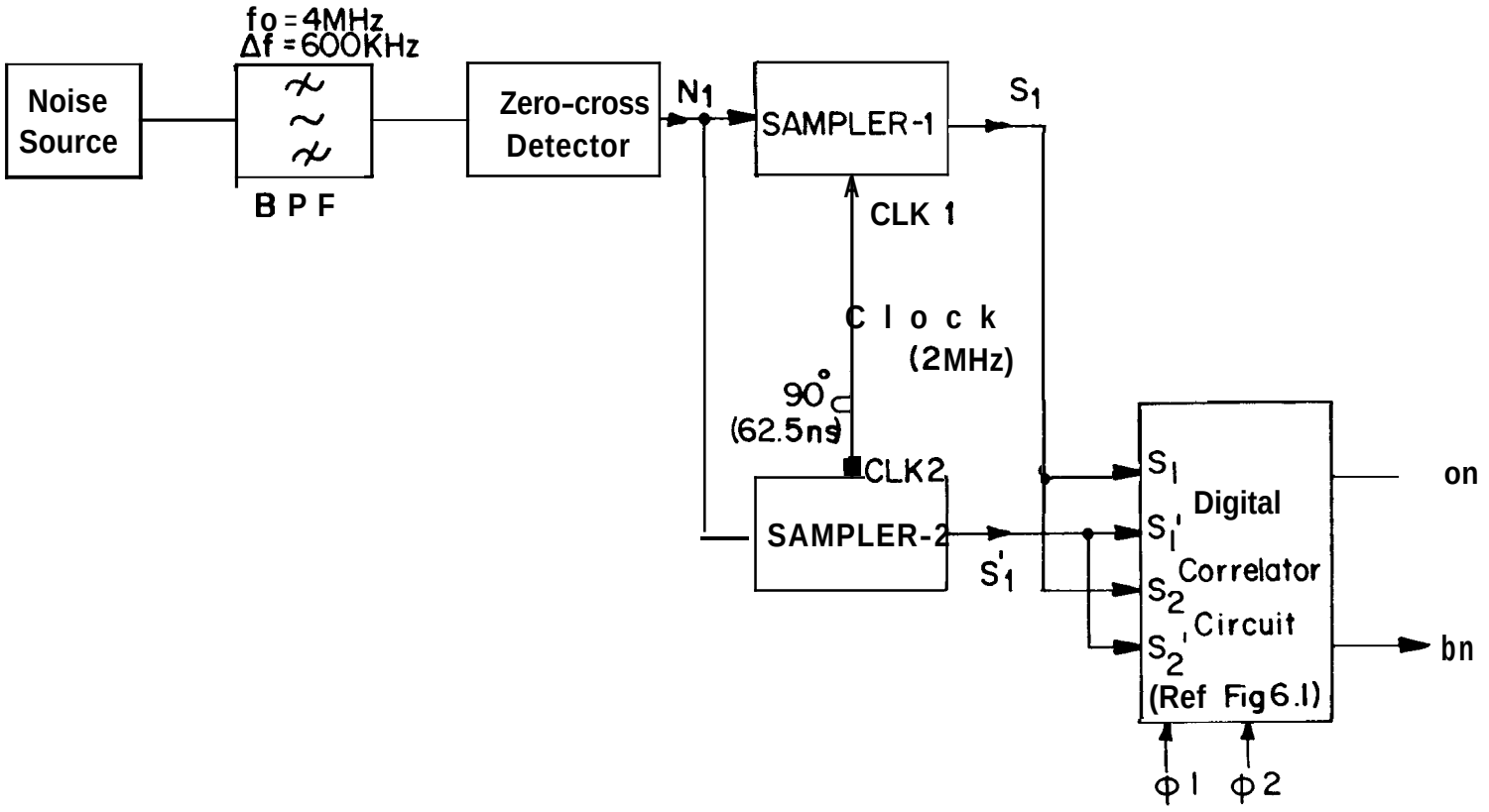


FIG 6.2. TEST SETUP FOR AUTO-CORRELATION.

ZCD, N_1, was sampled by a clock at 2 MHz to obtain the signal S_1. N_1 was also sampled by the clock shifted by 90^o, to obtain S_1' — the quadrature component of S_1. Further, S_1 and S_1' were fed to the digital correlator circuit also as S_2 and S_2' respectively. This makes the output the auto-correlation of the signals with zero time lag. The Cosine and Sine correlation coefficients were measured for these two elements. Normalised values of a_n and b_n were found to be unity and zero, respectively, which were their expected values. The results of this test therefore showed that the digital Correlator Circuit was functioning satisfactorily. That is, the variation in the propagation delays in the delay shift registers, four channel multiplexers, EXOR/EXNOR gates and the jitter in the clock signal in the delay shift registers, and the two phase clocks ϕ_1 and ϕ_2 do not produce any detectable loss in the correlation.

After testing the digital correlator circuit in the autocorrelation mode, the Correlator Circuit was tested with double sideband signals for its linearity. Fig. 6.3 shows the test set up used. Two independent noise sources N1 and N2 were connected to the two channels of the receiver through attenuators A1 and A2, which control the power output of these noise sources.

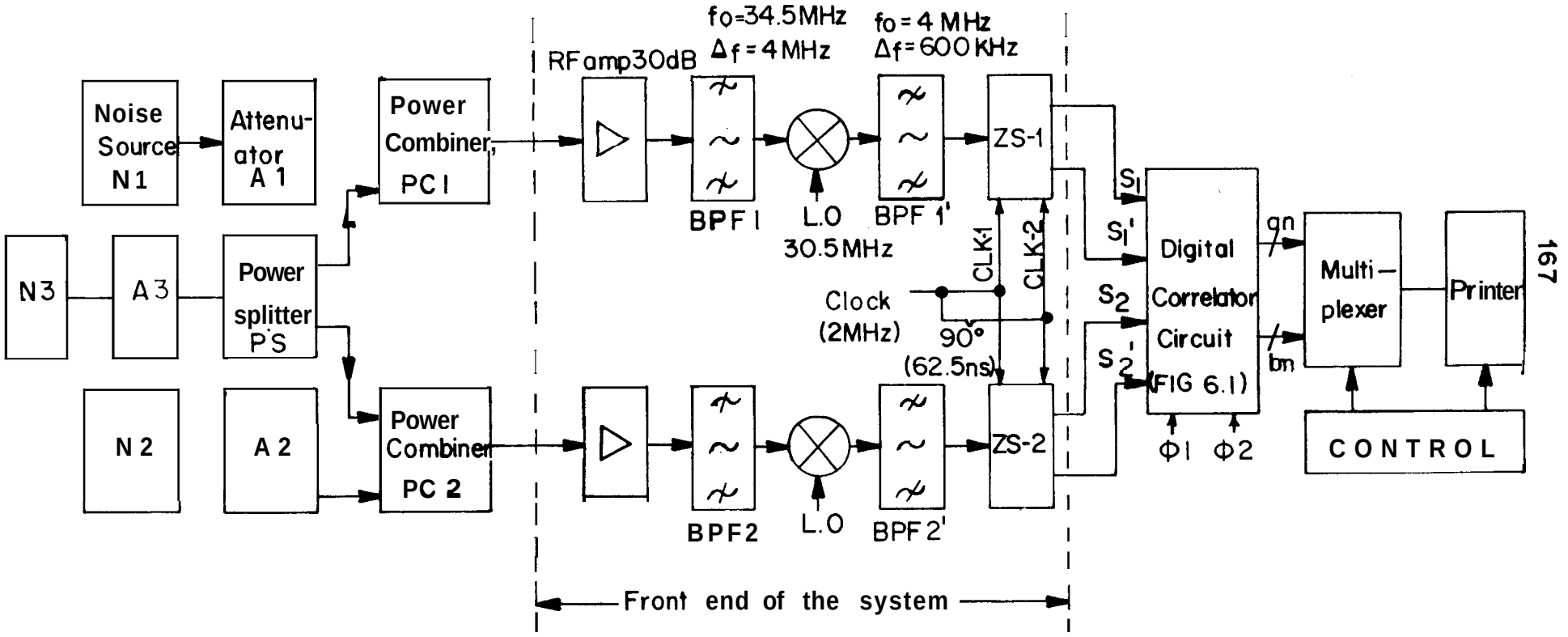


FIG 6.3 TEST SETUP FOR CROSS-CORRELATION-

A third noise source N3, which was used to simulate the signal, introduces equal powers simultaneously into the two channels of the digital correlator circuit via an attenuator, A3, and a power splitter, PS, and two power combiners, PC1 and PC2. A3 controls the signal power fed to the two channels of the receiver. The outputs of the power combiners pass through 30 dB-RF amplifiers followed by bandpass filters, BPF1 and BPF2 of 4 MHz bandwidth and a centre frequency of 34.5 MHz. Their outputs were mixed with the LO at 30.5 MHz giving an IF of 4 MHz. The IF outputs were passed through two more bandpass filters, BPF1' and BPF2' centred at 4 MHz with a bandwidth of 600 KHz, and their outputs were then converted to one-bit signals by passing through two zero-cross detectors. To enable bandpass sampling, the outputs of the zero-cross detectors were sampled by

(i) the clock, CLK-1, to give the signals S1 and S2 and also by

(ii) the clock, CLK-1, phase shifted through 90^{o}, to give S_1' and S_2'.

The outputs of both the channels, S_1, S_1' and S_2, S_2' were passed through delay shift registers and correlated using the digital correlator circuit, The correlator outputs were accumulated in counters for a predetermined time and the outputs of the counters were latched. The latched outputs from both the Cosine and

Sine correlators were outputted on a printer, as shown in the figure. Phase differences in the two channels were initially adjusted nearly to zero, so that only the Cosine correlation would be expected. In practice, since phase matching cannot be achieved over the entire band, both Cosine and Sine Correlation coefficients will have measurable values. The noise source, N3, was adjusted to give different signal levels for the correlator. It may be shown that the true correlation coefficient is given by

$$\rho_T = \frac{1}{\sqrt{\left(1 + \frac{1}{SNR_1}\right)\left(1 + \frac{1}{SNR_2}\right)}} \qquad (6.1)$$

where SNR_1 and SNR_2 are the signal-to-noise ratios of the two channels at the input of the digital correlator circuit,

The noise sources, N1 and N2 were adjusted to give an IF output of about 1.5 volts peak to peak, at which level the ZCD circuits function satisfactorily. Fig. 6.4 gave the variation of the Correlation Coefficient at the output of the digital Correlator Circuit, as a function of its true value, The standard deviation of the measured correlation coefficients from their true values was about 0.0255.

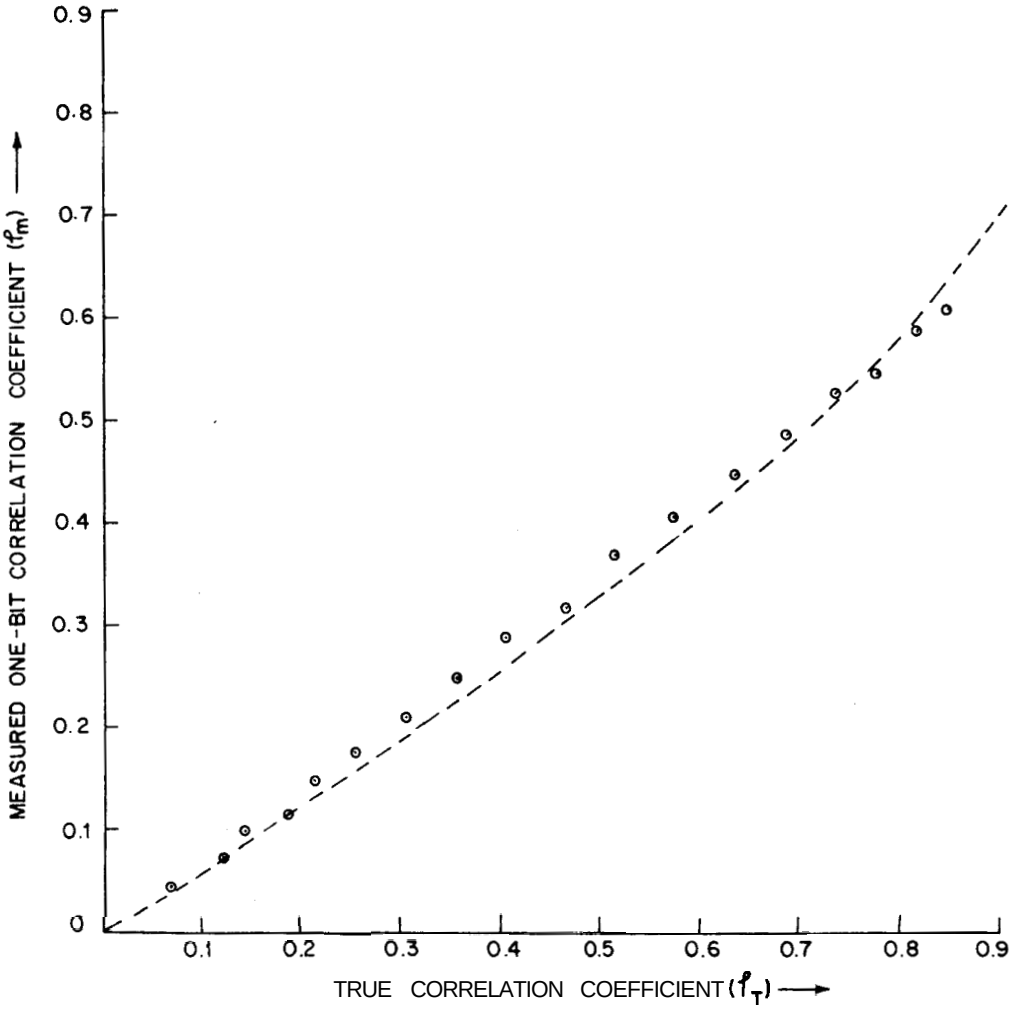


FIG. 6.4 PLOT OF OBSERVED COR. COEF. V/S TRUE COR. COEF.

The departure may be attributed mainly to the inaccurate calibration of the attenuators A1, A2 and A3 (Fig. 6.3) in determining the signal and noise powers to set different Correlation Coefficients in the test. The effect of phase characteristics in the front end system, threshold variation in ZCD's, jitter in samplers etc did also contribute to the departure of the measured correlation coefficients from their true values.

Another important measurement with the above test set up was to extend the test to zero signal power, When N3 output was set very small, the a_ns and b_ns gave the correlation of the two independent noise sources, N1 and N2. Both the a_ns and b_ns were within about one percent of zero correlation for an integration time of about 1/4 sec.

These tests establish that the circuit functions satisfactorily in giving the Cosine and Sine Correlation Coefficients of the two double sideband signals fed to the input channels of the receiver system.

6.2.2 Tests on the PT Processor

The FT processor was independently tested by feeding some known functions and comparing the transformed results of the system with the FFT results

obtained using a 13 digit calculator (HP 9821A)

Fig. 6.5 shows a Cosine function with a non-integral number of cycles chosen to give some significant points on the transformed function. The function to be fed was stored in the an-RAM (Fig. 4.1) in the following way. The phase correction cycle was used to implement the function

$$a_n = a'_n \text{ Cos } \Delta\psi_n + b'_n \text{ Sin } \Delta\psi_n \qquad \text{Eq.(4.2) Chap. 4}$$

$$b_n = b'_n \text{ Cos } \Delta\psi_n - a'_n \text{ Sin } \Delta\psi_n$$

The phase correction angle A was kept at zero by writing zeroes in all the locations of the $\Delta\psi$ -RAM. The function to be stored in the an-RAM was stored as the grading function in the GI-RAM. By putting a'_n as one and b'_n as zero, the grading function was stored in the an-RAM during the phase correction cycle. Similarly, the bn-RAM was written by choosing a'_n as zero and b'_n as one. For the present test, a'_n was made one by permanently connecting all the bits excepting the sign bit (MSB) to logic level '1'. Fig. 6.6 gives the test results of the FT processor compared with the FFT calculation with 13 digit accuracy. The curve 1 in the figure is from the FT processor, while curve 2 is the FFT result from the calculator. The mean error

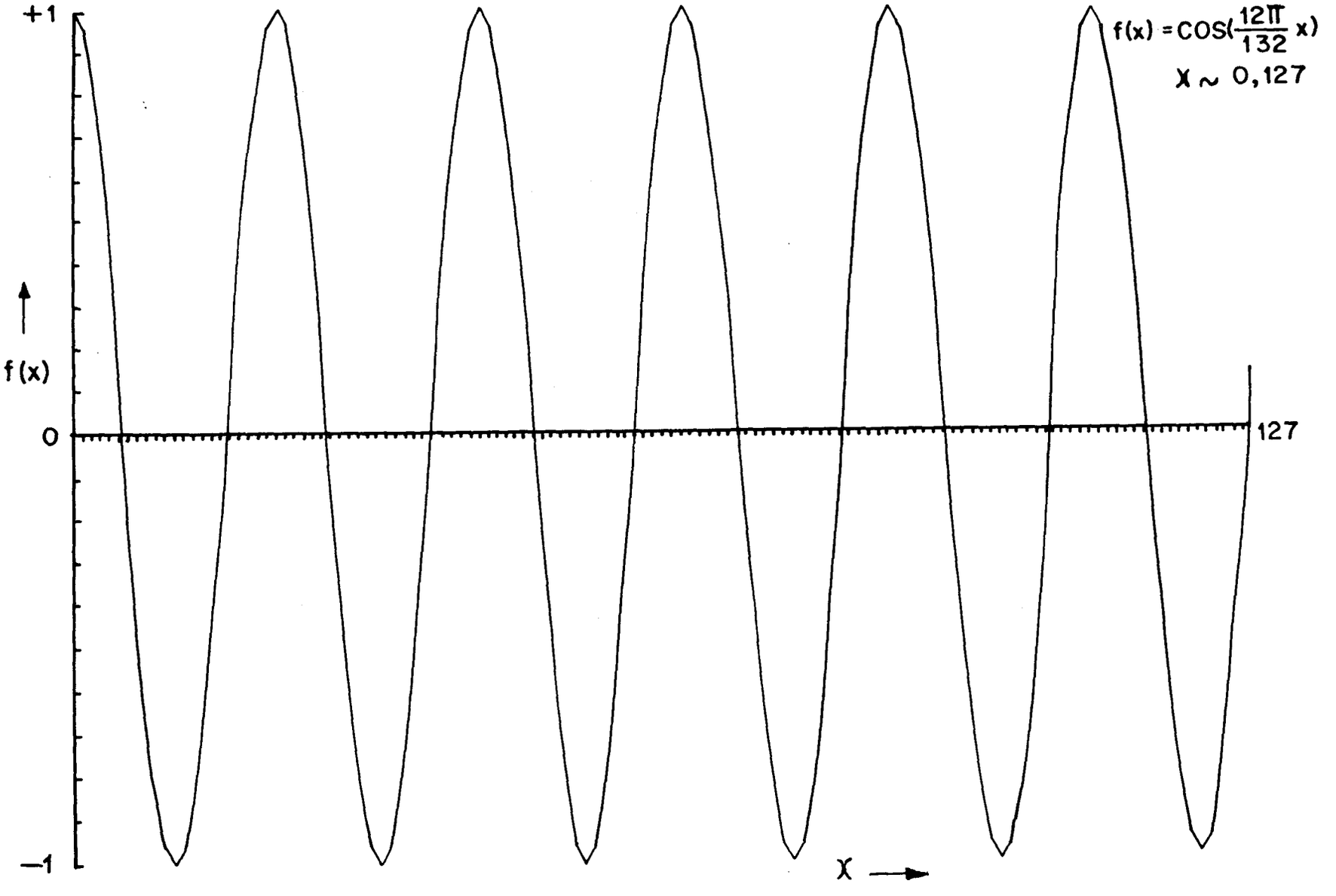


FIG. 6.5. COSINE FUNCTION FOR TESTING FT PROCESSOR

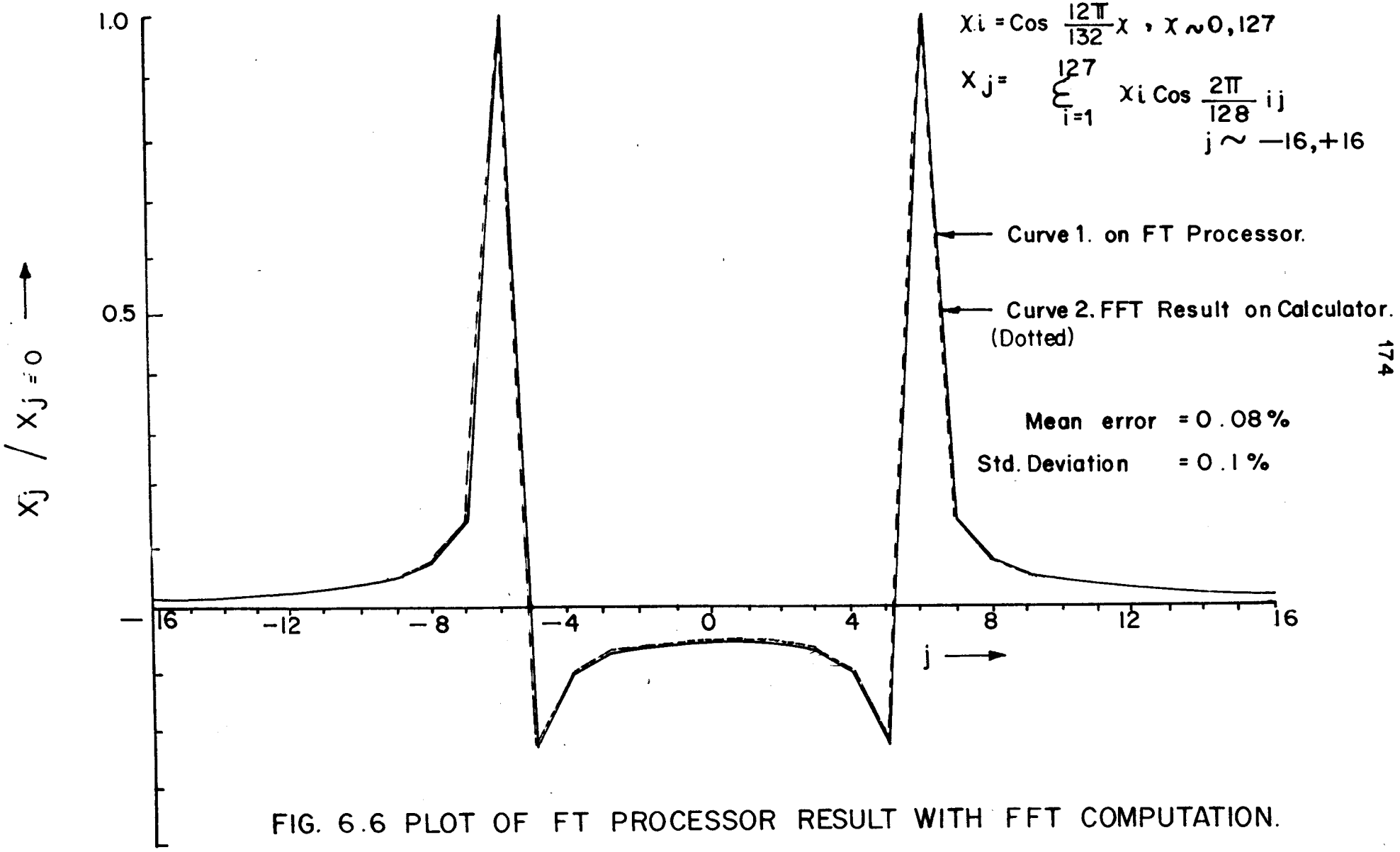


FIG. 6.6 PLOT OF FT PROCESSOR RESULT WITH FFT COMPUTATION.

and standard deviation between the two results were calculated and found to be 0.08% and 0.1% respectively. Prom this, it is seen that the truncation errors in the FT processor in representing the input number with only 8 bits, and the errors in truncation and rounding off after multiplication of two 8 bit numbers during processing to give only an 8 bit result are very small. The test was repeated several times to check the performance of the FT processor for its repeatability. Fig. 6.7A gives the display of the test result, while Fig. 6.7B gives the same repeated 128 times. Each column of points gives the level of the last significant bit of the 16 bit results corresponding to the 256 point display. There is no apparent error in computation in this repeatability test, confirming that the errors obtained are only from truncation and rounding off. Fig. 6.8 gives the grey level display of the output result, after converting and scaling the 16 bit 2'S complement output appropriately and truncating the result to give 4 bits for grey level display.

The above test was carried out by keeping the d.c. component, a_0, as zero. The test was repeated by keepinr a_0 as one, to check the proper functioning of the FT processor. The d.c. component, a_0, was directly entered from the input into the an-RAM as already discussed

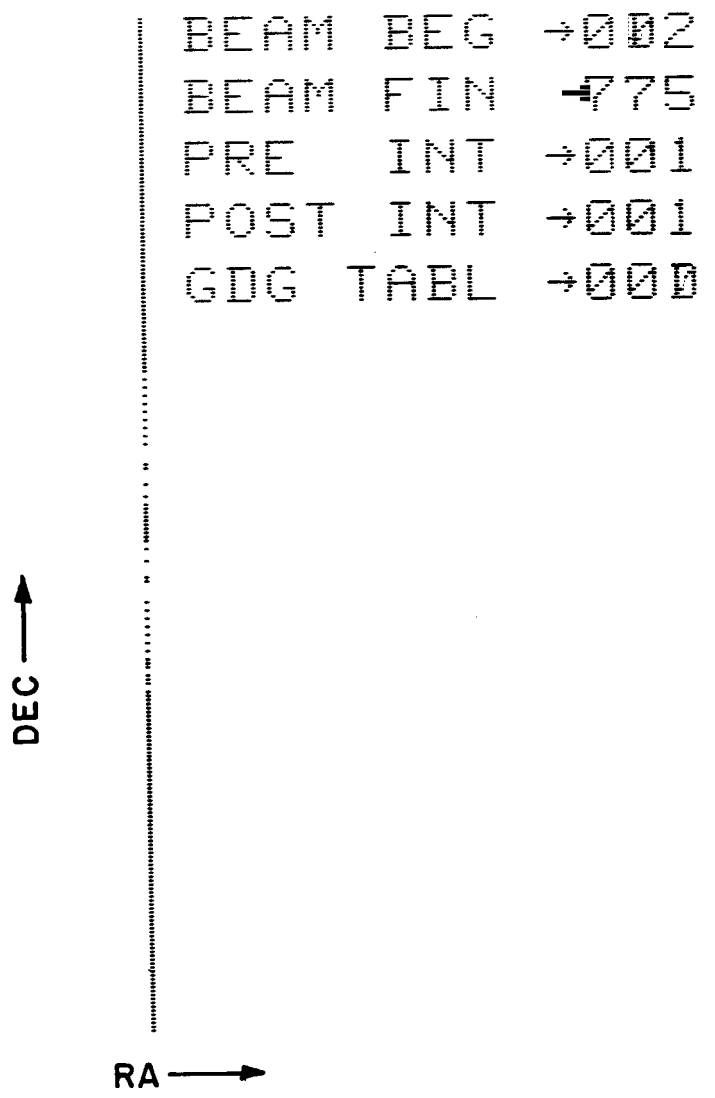


FIG. 6.7A GRAPHIC DISPLAY OF THE FT PROC. RESULT OF THE COSINE FUNCTION GIVEN IN FIG 6.5.

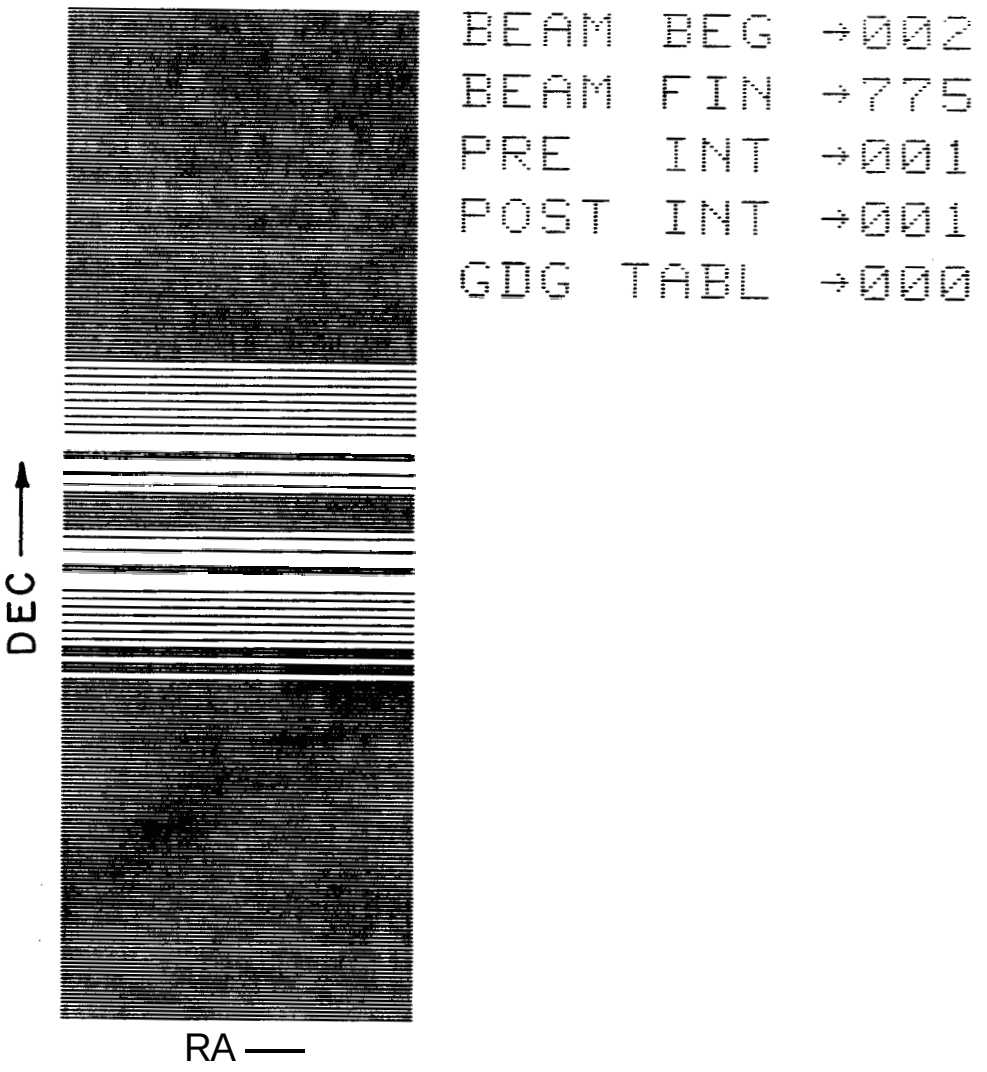


FIG 6.7B . GRAPHIC DISPLAY OF THE FT PROC. RESULT (LSB) REPEATED 128 TIMES OF THE COSINE FUNCTION GIVEN IN FIG 6.5.

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PRE INT →001
POST INT →001
GDG TABL →000

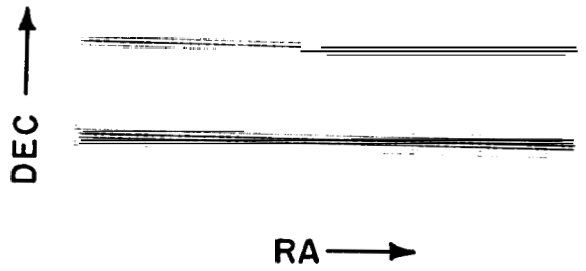

FIG 6.8 GREY LEVEL DISPLAY OF FT PROC. RESULT OF THE COSINE FUNCTION GIVEN IN FIG.6.5.

without going through the phase correction and weighting. This tested the functioning of the control circuitry of the FT processor in entering the d.c. component into the proper location in the an-RAM. The test results gave a mean error of 0.04% and a standard deviation of 0.1% again showing that the errors are insignificant. Fig. 6.9 shows a plot of the above test results.

The errors should be maximum when all the coefficients are maximum and hence a test was performed by keeping all the Cosine Coefficients maximum in the function,

$$f(\theta) = \sum_{n=1}^{N} a_n \cos n\theta \quad , \quad \theta = \frac{180}{256} \approx 0^{o}.7 \ldots (6.2)$$

A mean error of -0.7% and a standard deviation of 1.16% were obtained. Fig. 6.10 gives tne plot of the test results.

6.3 Field Trials

For carrying out the field trials of the Digital Correlator System, the N-S array was divided into 6 groups — 5 of 16 elements each and the sixth being of 10 elements only. The outputs of these groups wexe correlated with the single output of the E-W array. For this purpose, an eight input channel system was

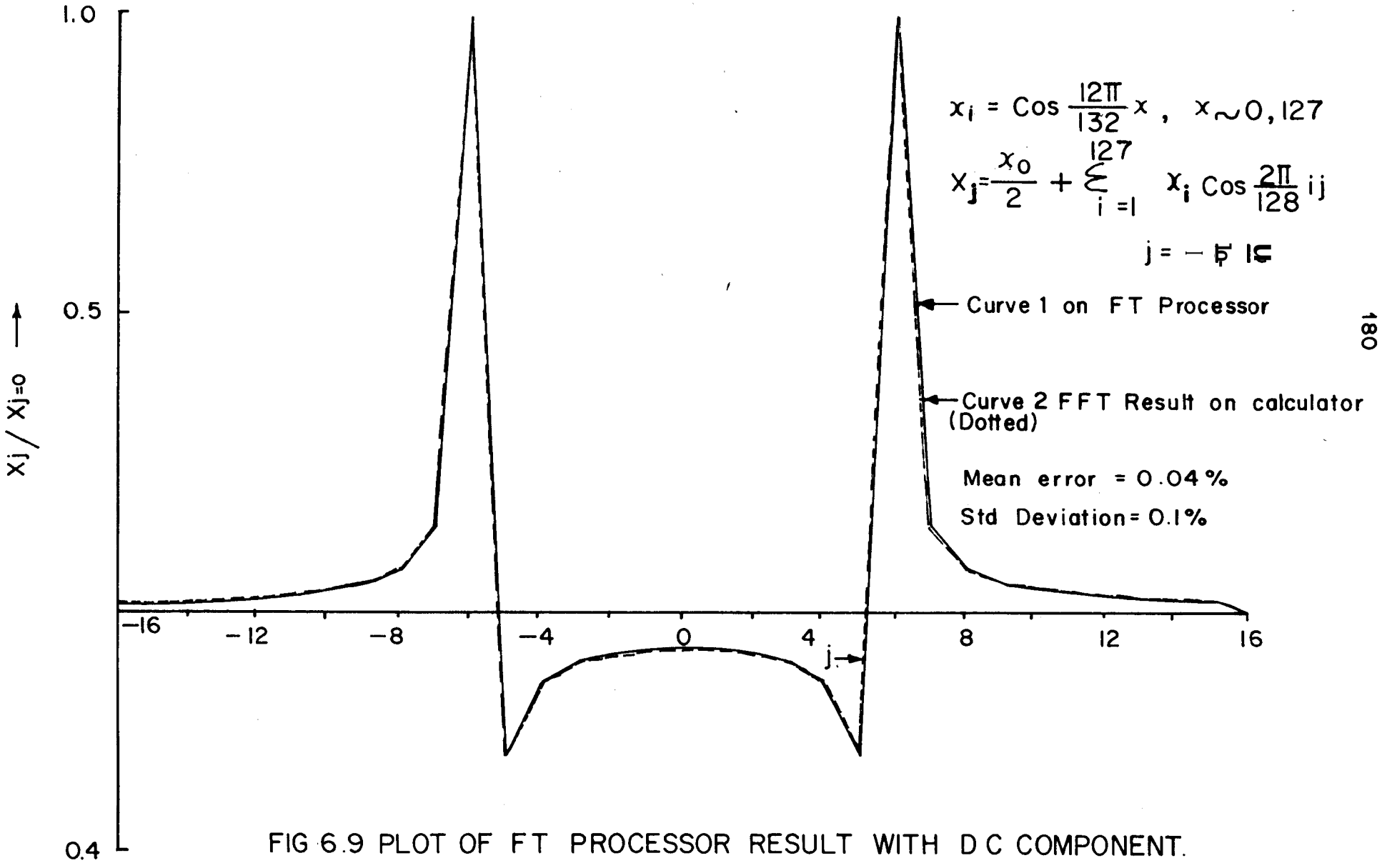

FIG 6.9 PLOT OF FT PROCESSOR RESULT WITH D C COMPONENT.

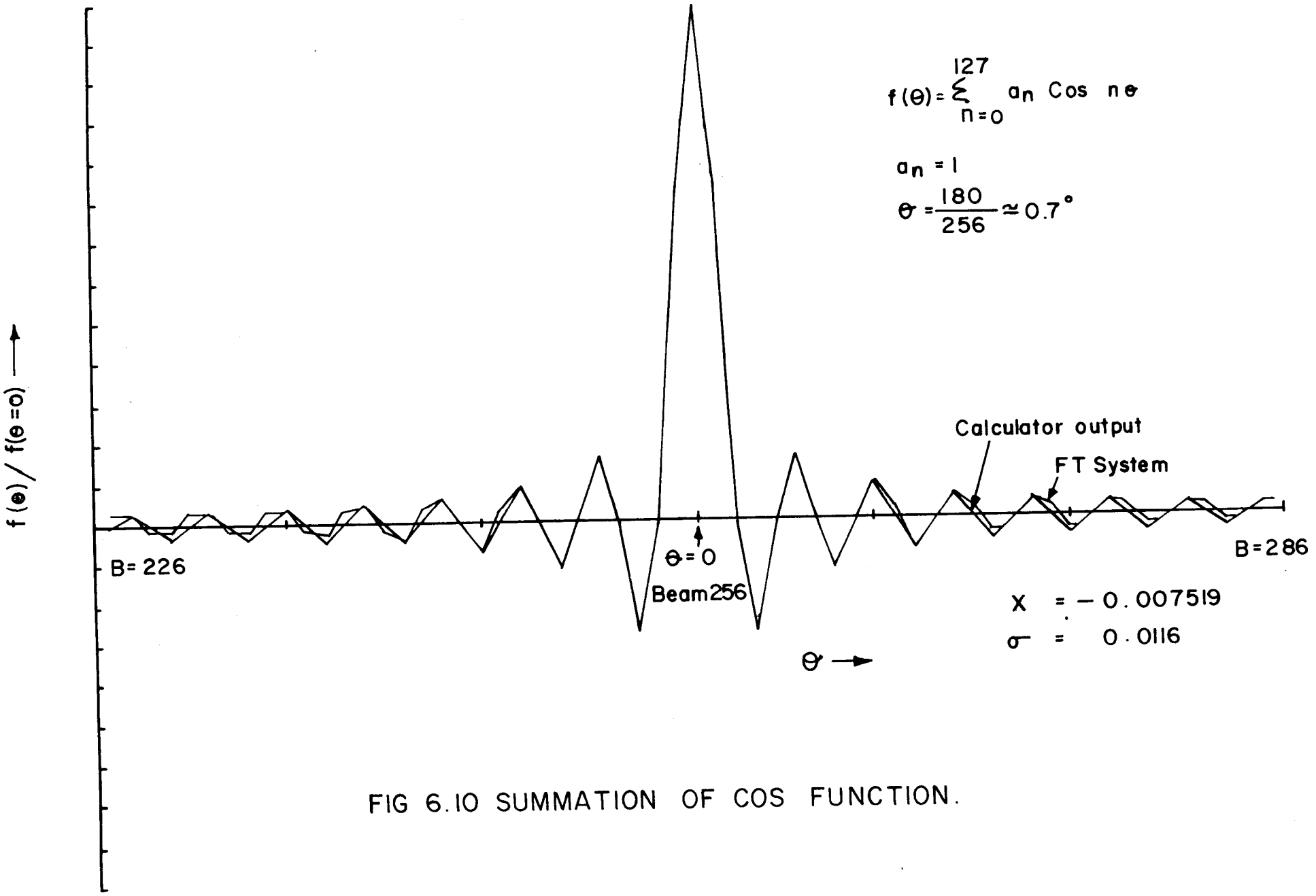

FIG 6.10 SUMMATION OF COS FUNCTION.

constructed. The signal S_{EW} (Fig. 6.11), from the E-W array was fed into the first channel and the outputs, S_{NS1}, S_{NS2}, S_{NS3}, S_{NS4}, S_{NS5} and S_{NS6} of the six groups of the N-S array were fed to channel numbers 2 to 7, respectively of the front end of the receiver. The signals, S_{NS1}, S_{NS2},..... S_{NS6} were also combined, employinp a corporate feed, and the single output, S_{NS7}, of the N-S array, thus obtained, was fed to channel No. 8 of the front end of the receiver.

The outputs of these 8 channels were connected to the inputs of the 8 channels of the Digital Correlator Circuit so as to yield the Cross Correlation Coefficients between S_{EW} and S_{NS1}, S_{EW} and S_{NS2}, ... S_{EW} and S_{NS}. Note that the output of the eighth channel of the Digital Correlator Circuit gives the autocorrelation Coefficient of the signal S_{EW}. This output checks the satisfactory operation of the digital system of the correlation receiver an3 was monitored throughout the field observation.

Before commissioning the system on the field, the test illustrated in Fig. 6.1 2 was carried out on the system in the laboratory. Since the same noise source is connected to all the eight channels, the outputs of the digital Correlator Circuit (after applying the Van-Vleck

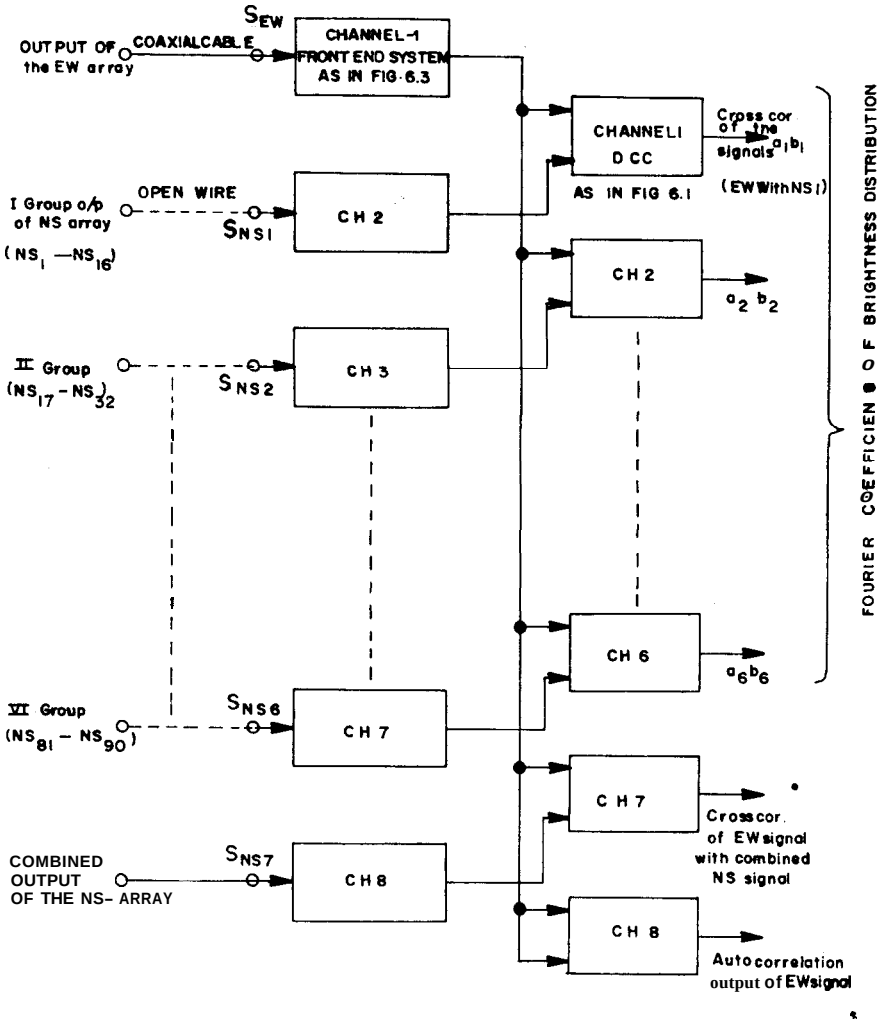

FIG 6.11 BLOCK SCHEMATIC OF 8 CHANNEL RECEIVER.

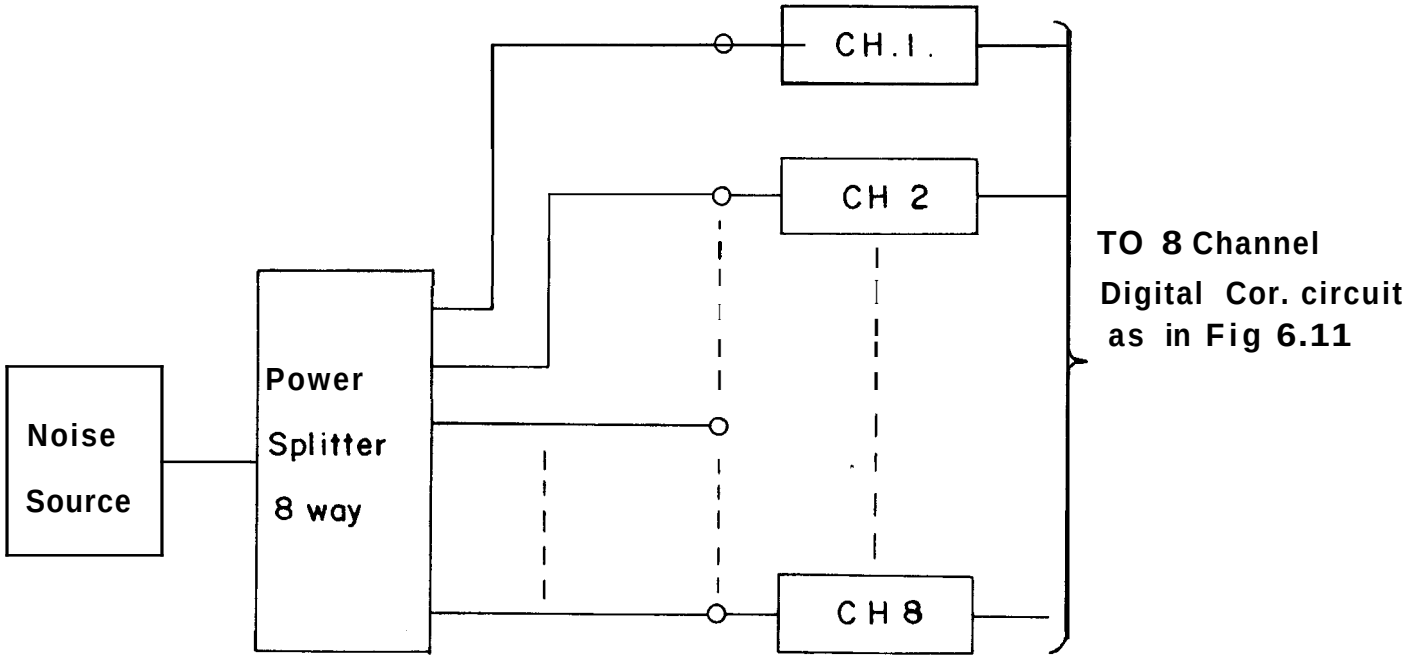

FIG 6.12 TEST SET UP FOR 8 CHANNEL RECEIVER

correction for one-bit signals) should give unity correlation coefficient. The results of this experiment showed a maximum loss in correlation of about 3%. This loss in correlation is due to the combined effect of the phase characteristics in the front end amplifiers, filters, mixers, threshold variation in ZCD, jitter in samplers etc.

The outputs from the six groups of the N-S array were connected by a 200 metre open wire transmission line (Ref, Fig. 6.11). The delay errors due to the differences between the lengths of the E-W cable and the N-S cables were compensated by setting the delay shift registers in the channels 2 to 7 of the digital correlation circuit. The field test was carried out by feeding a common signal from a noise source into the antenna ends of the transmission lines of both the N-S groups and the E-W array. The delay shift registers were set to give the maximum correlation in all the channels.

The noise levels in all the channels of the front end receiver were set by individual attenuators in each channel to give a noise level of about 1.5V peak to peak at the IF output, so that the ZCD's work satisfactorily. Observations were also made of some

strong point sources in the sky. The phase shifters in the E-W array and N-S array were set to point the beams at the declinations of the sources observed, A pre-integration time of about 1/4 sec was chosen to acquire the data corresponding to the Fourier Coefficients a_ns and b_ns of the brightness distribution. A post-integration factor of 80 gave a total integration time of about 20 seconds. The limited sampling of only six Fourier Coefficients of the brightness distribution was fed to the corresponding channels of the FT processor, keeping the other channels zero. The phase calibration of the six channels was done at the transit of one of the strong sources and the correction angles were stored in the corresponding locations of the $\Delta\psi$ -RAM. The FT processor output is the Fourier summation of the measured correlation coefficients, i.e, the brightness distribution in the N-S direction. The synthesized beam (normalized) is shown in curve 1 of Fig 6.13 obtained at transit of the source 3C144. Curve 2 in the figure gives the normalized beam pattern obtained on the source 3C218. Fig 6.14 shows the hard copy of the graphic display of source 3C144.

It may be pointed out that the system is designed to work with 90 G-3 channels. However, at the time of completion of this project, the hardware for only eight channels in the front end system was built. Since the

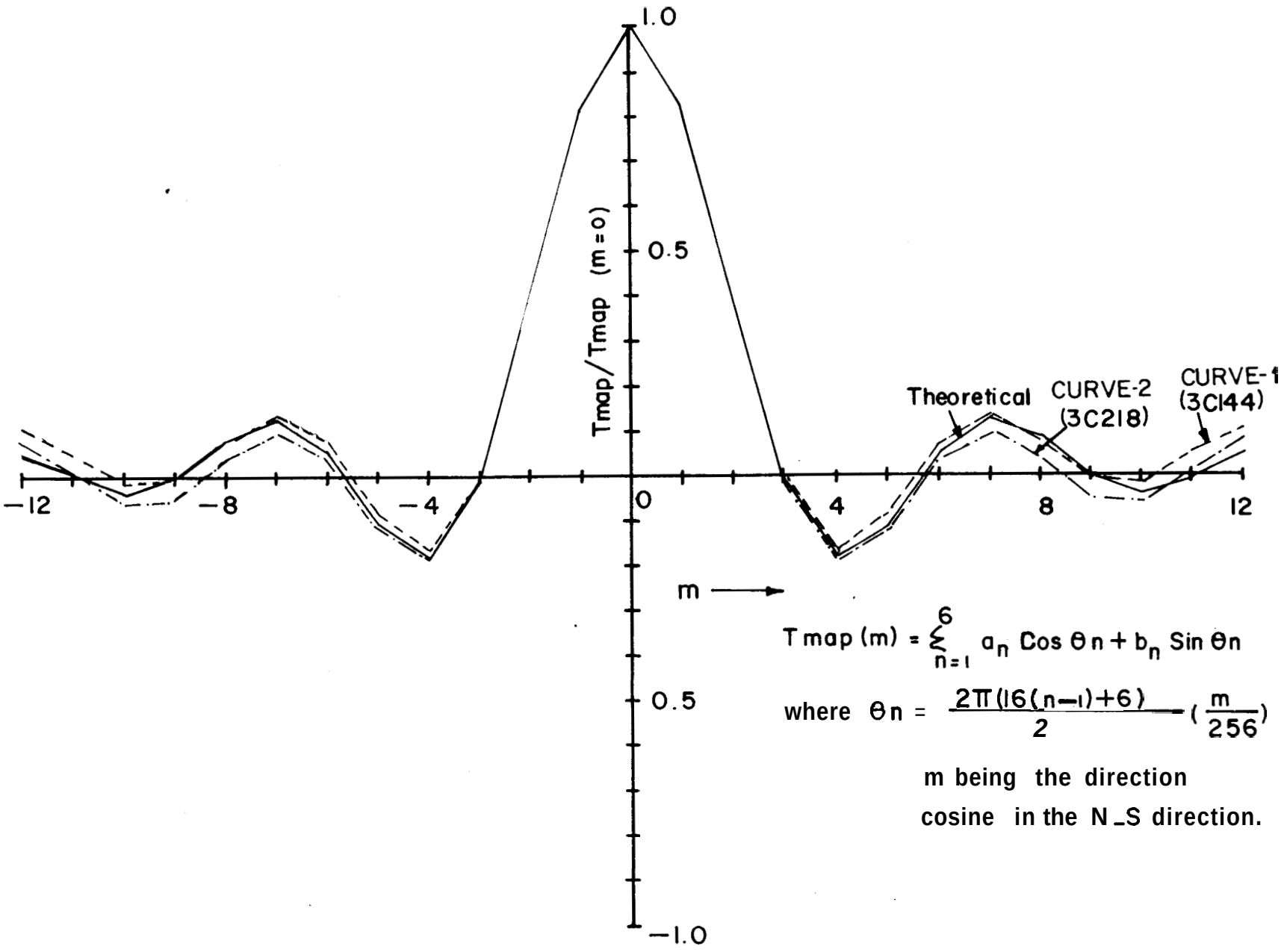

FIG 6.13 FIELD TRIALS TO SYNTHESISE BEAM PATTERN OF N-S ARRAY

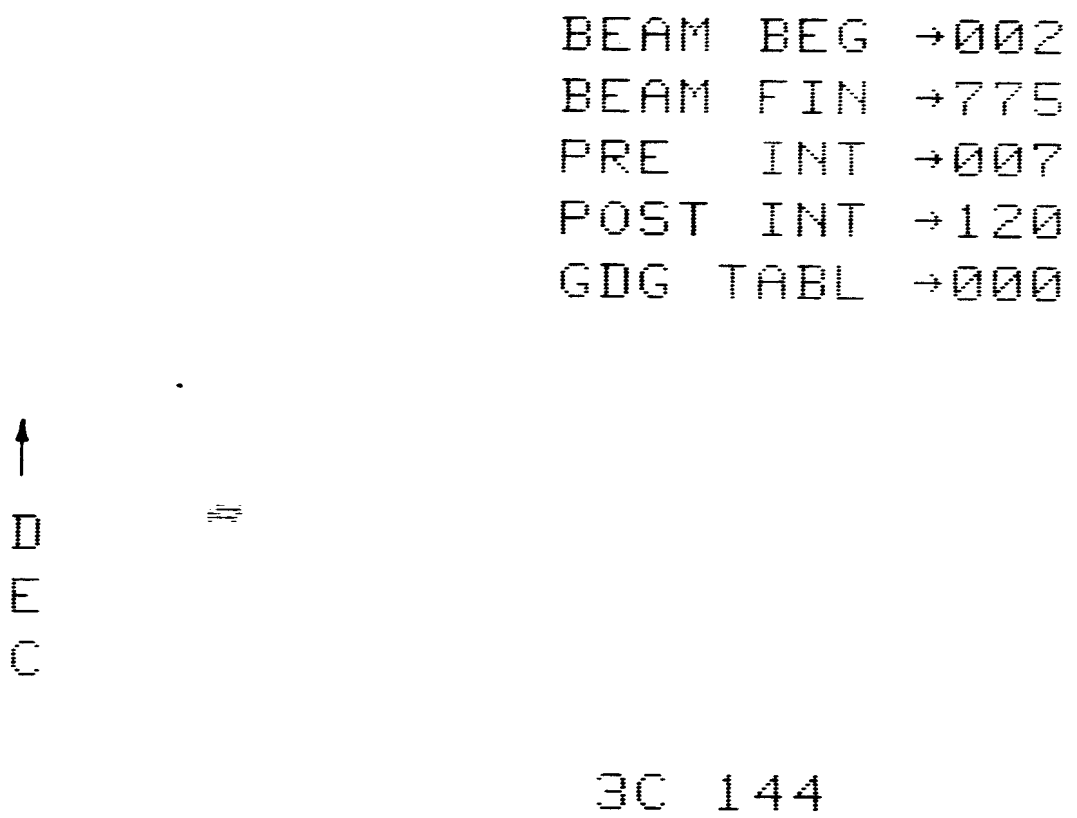

FIG 6.14 GRAPHIC DISPLAY OF THE SOURCE 3C 144

antenna elements in the N–S array are connected in a Christmas–tree arrangement, the outputs of groups of sixteen elements was taken. This resulted in 6 N–S group outputs for the above field trials. Hence, the tests were carried out on the digital correlation receiver with only 6 N-S channels. It is considered entirely reasonable to exnect that the total system will work satisfactorily based on the tests described of the 6 channel system. There are no cumulative errors in the system which could render a 90 channel system less accurate than the 6 channel system tested.

CHAPTER 7

CONCLUDING REMARKS

CHAPTER 7

CONCLUDING REMARKS

The design, construction and testing of a digital correlation receiver system for the low frequency telescope at Gauribidanur have been described in the earlier chapters. The signals from the multichannel correlator system are processed by Fourier transformation in real-time to obtain a brightness distribution map of the sky. The hardware to apply suitable phase corrections and to choose a grading function for the signals on an on-line basis has been discussed. A simple system is described which employs the digital one-bit circuits to correlate DSB signals and to obtain 2's complement conversion from the one-bit correlator-integrator, A microcomputer based peripheral controller was used to transfer the data from the FT processor to an incremental magnetic tape recorder and to display the processed signals on a TV monitor to provide a real-time brightness distribution map, The microcomputer was also used to initially set the delay for the various channels of the digital correlation receiver and to enter the phase correction data and the grading function in the appropriate memories.

In a one-bit correlator system, gain variations have practically no effect on the system performance. The phase calibration of the system is done by deriving the phase errors in each channel at the transit of a strong point sovrce and applying them as corrections while processing. This exercise has to be performed for various sources and at different times since ionospheric effects are predominant at the operating frequency of the telescope. The frequency of the calibration has to be decided based on a large sample of observations of the calibrating sources.

Scope for future work

There is a possibility of observing line radiation at the frequency of operation of the Gauribidanur telescope (Blake et al, 1980; Konovalenko et al, 1980). The present digital correlation receiver can be very effectively used as a line (auto-correlation) receiver by merely changing the front end circuitry to some extent. A 128 channel one-bit shift register can give time delayed samples of the input signal. The digital correlation receiver can be connected to obtain the autocorrelation coefficients. The on-line Fourier transformation then gives the power spectrum thus

enabling the observation of line spectra. The grading function facility can be used in this case to control the effective filter shape.

The microcomputer incorporated in the system is presently designed to operate as a peripheral controller and to perform some control operations of the receiver. At present, the grey level display of the brightness distribution map has a limited dynamic range in intensity, since the human eye can resolve at most 10 grey levels in a black and white TV monitor. A ruled surface display, on the other hand can have a much larger dynamic range. The microcomputer can be programmed to display the final data of the FT processor in the ruled surface format.