CHAPTER - 4

FOURIER TRANSFORM PROCESSOR

4.1 Introduction

We discuss in this chapter the Fourier Transform (FT) Processor subsystem of the Digital Receiver System. The FT processor computes, on an on-line basis, the sky brightness distribution employing digital techniques and by using the cosine and sine correlation coefficients as its input data. Appropriate phase corrections and the grading function are applied to the cosine and sine correlation coefficients which are obtained from the observed signals as explained in Chapter 3.

4.2 Principle of operation

The brightness distribution, $T_{map}(m)$, of the sky for a given direction of the beam in the meridian plane is given by (Appendix 3)

$$T_{map}(m) \propto \sum_{n=0}^{N} (a_n \text{ Cos } 2\Pi V_n m + b_n \text{ Sin } 2\Pi V_n m) \quad \text{.....(4.1)}$$

where a_n, b_n = the Cosine and Sine correlation coefficients,

m = Cos Z = the direction Cosine, Z being the zenith angle

V_n = the spatial frequency = 0.5 n cycles/radian

N = the total number of elements in the North-South array.

Let $2\Pi V_1 m$ be equal to angle θ, where V_1 is the

epatial frequency component given by the separations of any two adjacent elements of the N-S array. That is the angle, θ, the minimum incremental angle that has to be provided in the SIN and COS look-up tables.

As there are 90 each of Cosine and Sine Correlation coefficients in the spatial domain which has Hermitian Symmetry (Appendix-3), Fourier transformation will yield 180 independent directions called 'beams' in the angular domain. Since digital techniques are employed, processing for 256 beams instead of 180 beams does not involve much additional cost. In any case, it is desirable to oversample, and therefore 512 beams are formed in the meridian plane. While performing discrete Fourier Transformation (DFT), 38 points with zero values are appended to the ninety measured Correlation Coefficients and a 128 point DFT is performed.

4.3 System Design

The main features of the system design of the processor are:

1) pipeline technique of data processing;
2) on-line data acquisition and correction;
3) on-line implementation of grading function; and
4) selectable pre and post-integration time.

In the pipeline processing technique, the whole

processor system is divided into various blocks. The data flow from each block is sequential, while the processing goes on concurrently in different blocks. At no time does data acquisition or computation stop, and one has therefore to keep a careful watch on the valid data flow in any block at a particular instant of time. Data has to be latched at various blocks in order to yield error free operation. There is a severe constraint on logic design to keep the propagation delay within the cycle time of the processor. That is, the access time and the computation time of different hardware elements in each block has to be maintained within the basic cycle time of the processor.

The present digital correlation receiver is designed to be used in a variety of applications like making brightness distribution maps of sources at the frequency of operation of the telescope, scintillation studies of the ionosphere, solar observations, pulsar searches etc. These applications call for different integration times in the receiver, since the frequency spectra of interest for these applications are different. In the case of survey

work, where the brightnees distribution is to be computed, integration times should be as large as possible (limited by the beanwidth in the EW direction) so that weak sources can be detected. For scintillation work, the time constant of the receiver should be around 10 to 100 ms. In pulsar studies, the time constant should be as small as possible, preferably in the range of a few milliseconds. To cater for these different time constants, integration time control is provided at 2 levels, prior to and after the Fourier transforming process and are called pre-integration and post-integration respectively. This two level control gives economical system design for the required speed of operation. Pre-integration time is selectable from 2 mS to 256 mS in steps of powers of 2, while post-integration is a multiplying factor ranging from 1 to 256 times the preintegration setting. Thus integration times of 2 mS to about 1 minute can be obtained with the combination of the above controls.

In an on-line processing system, corrections, if any, have to be implemented on the measured correlation values before transformation. There are essentially two types of corrections - one is to compensate for gain instabilities in each channel and the other for relative phase errors in all the channels. Gain

corrections need not be incorporated in the one bit correlator system, since the signal is amplified sufficiently before going through the zero-cross detector. kelative phase errors between channels can be corrected by rotation of rectangular co-ordinates by the phase correction angle of each channel. Relative phase errors can be obtained from the known strong sources whose position in the sky are accurately known. These errors between the expected and the measured values can be noted and used in correcting the measured values. The error angles with a resolution of $\sim 1^{o}.4$ corresponding to each channel are stored separately in a RAM and can be accessed very fast. Let a_n' and b_n' be the measured cosine and Sine coefficients, while a_n and b_n are the exgected values. The phase error angle can be positive $(+\Delta\psi)$ or negative $(-\Delta\psi)$ depending upon whether the vector a_n' is anticlockwise $(0^{o} < \Delta\psi < 179^{o})$ or clockwise $(180^{o} < \Delta\psi < 359^{o})$. To rotate the vector in the rectangular coordinate system, one has to implement the following equations:

Case a: $+\Delta\psi (0^{o} < \Delta\psi < 179^{o})$

$$a_n = a_n' \text{ Cos } \Delta\psi_n + b_n' \text{ Sin } \Delta\psi_n$$

$$b_n = b_n' \text{ Cos } \Delta\psi_n - a_n' \text{ Sin } \Delta\psi_n \qquad \ldots \quad \ldots \quad (4.2)$$

Case b: $-\Delta\psi (180^{o} < \Delta\psi < 359^{o})$

$$a_n = a_n' \text{ Cos } \Delta\psi_n - b_n' \text{ Sin } \Delta\psi_n$$

$$b_n = b_n' \text{ Cos } \Delta\psi_n + a_n' \text{ Sin } \Delta\psi_n$$

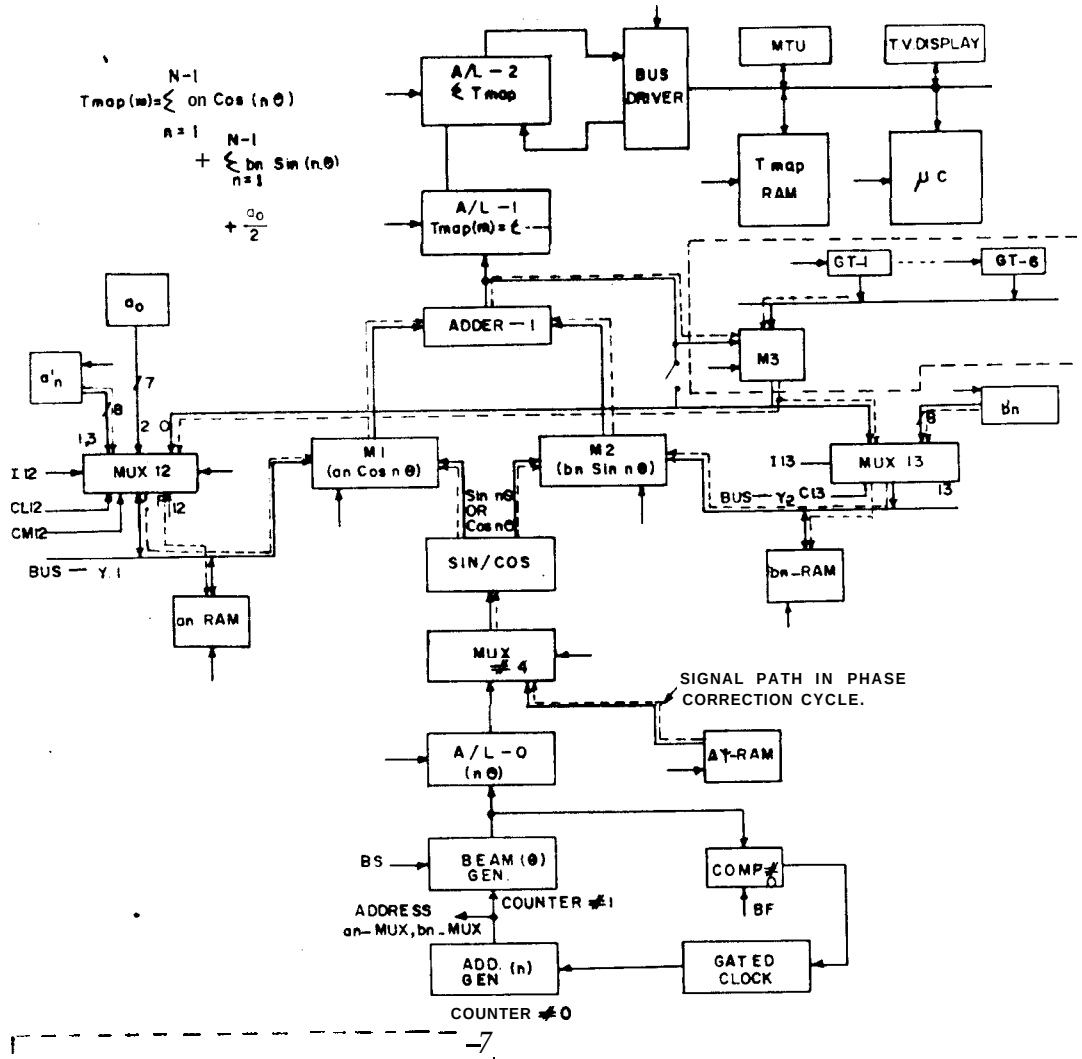
Appendix-4 gives the derivation of these expressions. The terms in these sets of equations are similar to those used in the normal FT operation (Equation 4.1). Hence, the hardware is efficiently utilised by two passes of the data, first going through the phase correction mode during data acquisition of the measured correlation coefficients, and then going through the FT operation. Control circuitry takes care of switching the appropriate arguments, the data and the sign for these terms.

Grading of the coefficients is also provided by weighting each coefficient before transformation. This affects the resolution and the side-lobe structure in the transformed domain and this has to be done after phase correction of the coefficients and before the normal operation of the transformation.

4.4 System description

Fig 4.1 gives the block schematic of the FT processor. The address Generator (counter-0) issues 7 bits of binary address to each of the two multiplexers the a_n - multiplexer and the b_n-multiplexer. The decoder in the control circuit sequentially multiplexes a_n' and b_n' simultaneously.

In the phase correction mode, the multiplexers, MUX-12 and MUX-13, enable a_n' and b_n' to one of the



CONTROL

1 TO GENERATE SIGN BITS IN PHASE CORRECTION & NORMAL OPERATION

2 TO WRITE an & bn AFTER CORRECTION

3 CONTROL SIGNALS FOR MULTIPLIERS.

4 CONTROL FOR POST INTEGRATION CIRCUITS.

FIG . 4.1

BLOCK DIAGRAM OF FOURIER TRANSFORM PROCESSOR

inputs of the multipliers M1 and M2 through the BUS Y1 and the BUS Y2 respectively. The multiplexer MUX-4, connects the A9 -RAM to the SIN and COS tables. Outputs from these tables are connected as second inputs to the multiplers, M1 and M2.

The sign bits for the positive and the negative angles are obtained from the MSBs of 'the data from the A+-RAM. The tables are switched such that in the first 128 clock pulses, b_n is obtained by computing $b_n' \cos \Delta\psi_n \mp a_n' \sin \Delta\psi_n$ and stored in the bn-RAM, through Multipliers, M1, M2 and Adder-1. Next, a_n is computed in the following 128 clock pulses as "$a_n' \cos \Delta\psi_n \pm b_n' \sin \Delta\psi_n$" and stored in the an-RAM, a_o is stored in the first location of the an-RAM. through the MUX-12 by properly gating the data into the an-RAM.

There are four fixed grading functions provided by four ROMs, GT-3 to GT-6, and two variable grading functions provided by the two RAMs, GT-1 and GT-2, which can be programmed from the console to store the grading function.

Multiplier, M3, is used for weighting the corrected coefficients by choosing the appropriate Grading table

selected from the Console. In fact, when not needed, the whole grading operation can be bypassed under control from the Console. Thus corrected and weighted correlation coefficients are acquired and placed in the a_n-RAM and the b_n-RAM for further processing.

In the normal mode, T_{map} can be computed for any number of beams under console control. The beam start thumbwheel switch situated on the console (BS) loads the starting angle, θ_s , into the Beam generator counter, counter-1, and goes through increments of one till the number set on the beam finish thumbwheel switch (BF) at the Console is reached. This counter is incremented after computing T_{map} for each beam by adding 128 terms, taking 128 clock pulses. The gated clock is stopped after computing for θ_F and waits for initiation of the next cycle till the end of the next integration period. This period, termed the pre-integration time, is selectable from 2 ms to 256 ms in steps of powers of two from the Console.

The Adder/Latch circuit, A/L-O, is used to generate n values for generating successive arguments in the normal mode. Here the present value $(n-1)\theta$ is added to θ from the Beam generator to get $n\theta$. MUX-4 enables $n\theta$ to be passed on to address the SIN

and COS tables in normal operation. Control circuitry for generating sign bits corresponding to SIN $n\theta$ and COS $n\theta$ are not shown in the block schematic . The 2's complement values for COS $n\theta$ and SIN $n\theta$ are used as arguments for the multipliers. These are fast multipliers taking $\leq$150 ns for multiplication and are capable of working in the pipeline mode, that is, new arguments can be taken in while the result of the previous terms is being taken out. The clock circuitry has to take care of the pipeline processing so that the initial terms are ignored, since the data flow has a definite time lag starting from the Address Generator. Adder-1 gives the sum of a_n Cos $n\theta$ and b_n Sin $n\theta$ corresponding to one coefficient at any time. The Adder/Latch Circuit, A/L-1, adds up all the 128 terms corresponding to each beam and stores the sum in a separate location in the final Tmap-RAM. The post-integration factor, a multiplication factor of upto 256 set by the Console control, is provided by the Adder/Latch Circuit, A/L-2, which adds the accumulated value to the present computed one, for each beam separately, and gives effectively the 'up-date' in the Tmap-RAM. At the end of the post-integration period, the data so accumulated corresponding to Beam-start to Beam-finish is dumped onto the

Magnetic tape unit, and also displayed on the video Monitor under microcomputer control to be discussed later. Fig 4.2 gives the schematic of the Control Console.

A section on the detailed circuit design is included in this chapter (Sec. 4.5) and also at the end of Chapter 5 (Sec. 5.3) to bring out clearly the basic contributions of the author in the design of the system. A detailed understanding of these sections may not, however, be necessary for a general appreciation of the overall system.

4.5 Detailed Circuit Design

4.5.1 Generation of clock signals

The basic clock required for the system is chosen as 2 MHz, as the maximum bandwidth of the signal to be processed is 1 MHz. A crystal controlled oscillator, shown in Fig 4.3, is the internal clock for the system. The system can also be driven from an external clock which may be of higher stability through the multiplexer, MUX-1 and the switch S1. The clock signal for the delay shift register (Fig 3.5), two-phase clocks in the correlator circuit (Fig 3.5), and the strobe and reset signals in the integrator circuit (Fig 3.6), are all

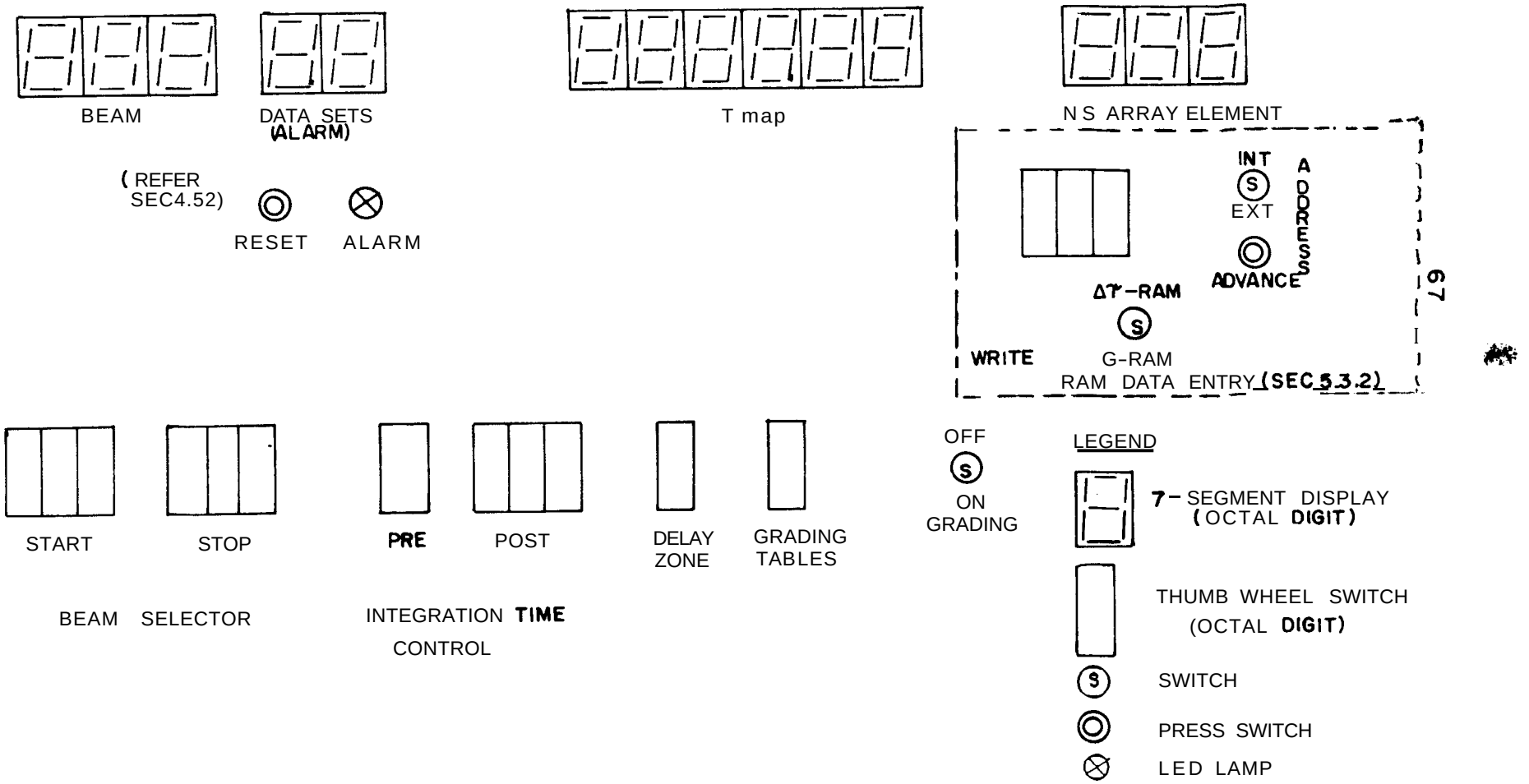


FIG 4.2 CONSOLE CONTROL.

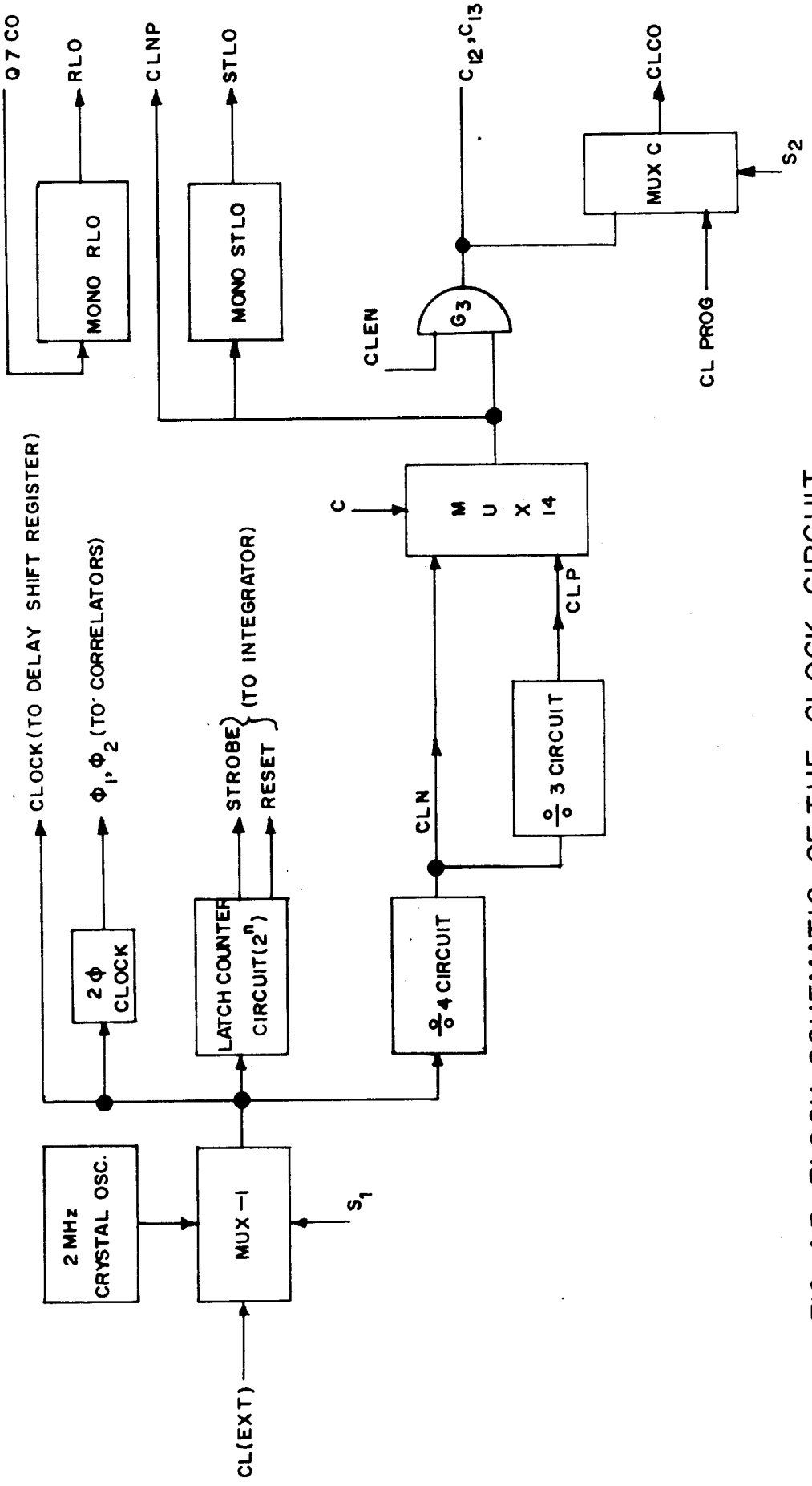


FIG 4.3 BLOCK SCHEMATIC OF THE CLOCK CIRCUIT.

derived from the 2 MHz clock as shown in the figure.

The FT processor is designed based on the pipeline processing technique in order to achieve faster data processing in real time. The design in this technique mainly concerns the division of the sequential processor into various blocks. The processing in each block is sequential, while the processing in different blocks are concurrent as already discussed in Sec 4.2, The number of blocks necessary for the complete processor is designed based on the function of the block, the propagation delays of the suitable devices to implement the function, the cost effectiveness and the power requirements in the logic design. Based on the worst case propagation delays in different blocks, the basic cycle time 2 μs for the processor is chosen. This is the most critical aspect of the whole design, as this controls the operational speed of the system thereby determining the throughput rate in the real-time processor. Another important aspect of the design is in choosing the devices, like LSI and other digital integrated circuits, which are compatible with pipeline processing. In addition to the above, cost effectiveness and power requirements are always considered in the choice of devices. All the LSI circuits are TTL

compatible circuits, while the logic circuits are based on CMOS circuits to save power. Buffer circuits are used wherever the LSI circuits are driven. The atability of the monoatable circuits used in various control circuits is not critical.

The 2 μs clock signal (CLN) is derived from the 2 MHz basic clock through two stages of divide-by-two circuits as shown in Fig 4.3. In the phase correction cycle, the multiplexed correlation coefficients from the correlators go through the phase rotation given by equations(4.2) and(4.3) and the coefficients are weighted by the function stored in the grading tables as already mentioned in Sec 4.2. Since the path for data flow is different in the process of correction and weighting, the system is divided into different blocks for the pipeline design in the correction cycle. A cycle time of 6μs was chosen based on the worst case propagation delay with a factor of safety of about 10 per cent. The phase correction clock, CLP, of 6 μs is derived from the clock, CLN, by a divide-by-three circuit as shown.

The internal clocks, CLN and CLP, are appropriately multiplexed as the signal CLCO to the address generator, COUNTER-0 (Fig 4.1) during the normal and the phase correction cycles respectively through multiplexer, MUX-14,

and clock enable gate, G3. External clock, CLPROG, can drive the address generator, COUNTER-O through the clock multiplexer, MUX-C. This is required to write data on $\Delta\psi$-RAM or G-RAM in the off-line mode. The choice of internal clock or external clock for address generation is controlled by a switch, S2, on the console.

4.5.2 Implementation of pre-integration time

Pre-integration time can be chosen as 2^n ms, n being selectable from 1 to 8 for different applications in radioastronomy as already indicated.

At the end of the pre-integration time, the counter values are latched, giving a data set of correlation coefficients a_i and b_n for further processing. The pre-integration time should always be chosen greater than the time required for the phase correction cycle and the time required for computing the brightness distribution for the selected beams. If this time is chosen to be less, the data sets of correlation coefficients will be missing in further processing. An observer will not be able to detect this in an on-line system. Because missing of the data sets leads to error in the RA (x-axis) of the two-dimensional plot of the T_{map}, the system is designed to sound an alarm

to the observer if such a situation arises. He can then either increase the pre-integration tine, or decrease the number of beams in processing, so as not to miss any data sets. In case he does not want to change either setting, processing will still be continued with the previoua settings, but with the observer's knowledge. A counter keeps count of the number of data sets missed, so that the x-axis of the brightness distribution map can be scaled accordingly later,

Fig 4.4 gives the circuit diagram of the controller for giving the pre-integration times. Fig 4.5 gives the timing diagram of the complete FT-processor. An Initialise switch on the console resets a flipflop, NORFF4, in normal operation. This enables gate, G1, to give the signal, LCP, whenever the latch counter pulse, LC, is issued at the end of every pre-integration period. The LCP signal sets up flipflops, ANFF1 and BNFF2, to enable the an-HAM, and the bn-RAM during the phase correction cycles. The signal, LCP, also sets up the clock flipflop, CLFF5, to give clock enable signal, CLEN, to enable the internal clock pulses for the address generator given in Sec 4.4.1. The signals, Q8C0 and Q9C0, from the address generator, COUNTER-0 (Fig 4.1), issued after 128 clock pulses and 256 clock pulses are used to reset ANFF1 and BNFF2 respectively.

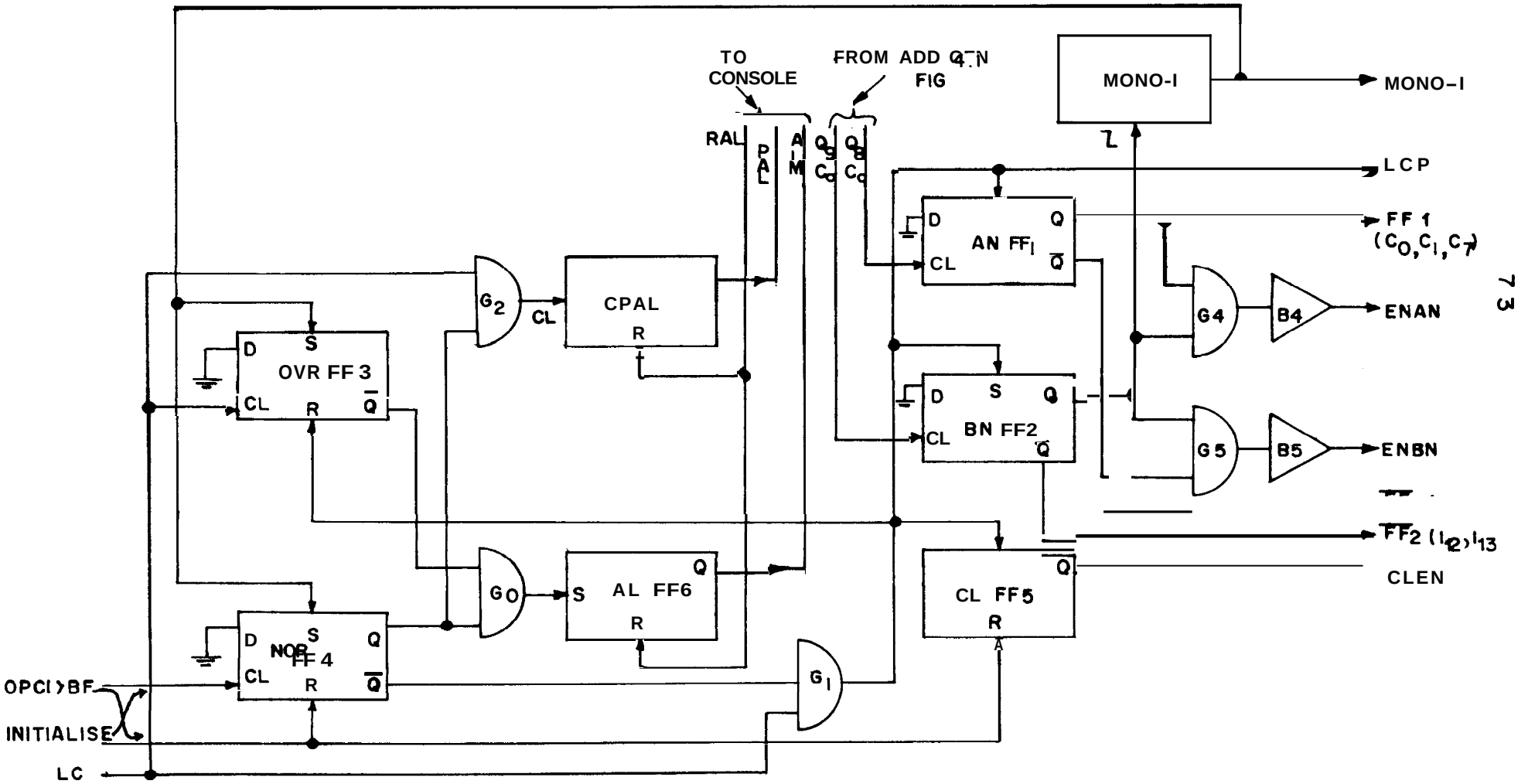


FIG. 4.4 PRE -INTEGRATION CONTROL CIRCUIT

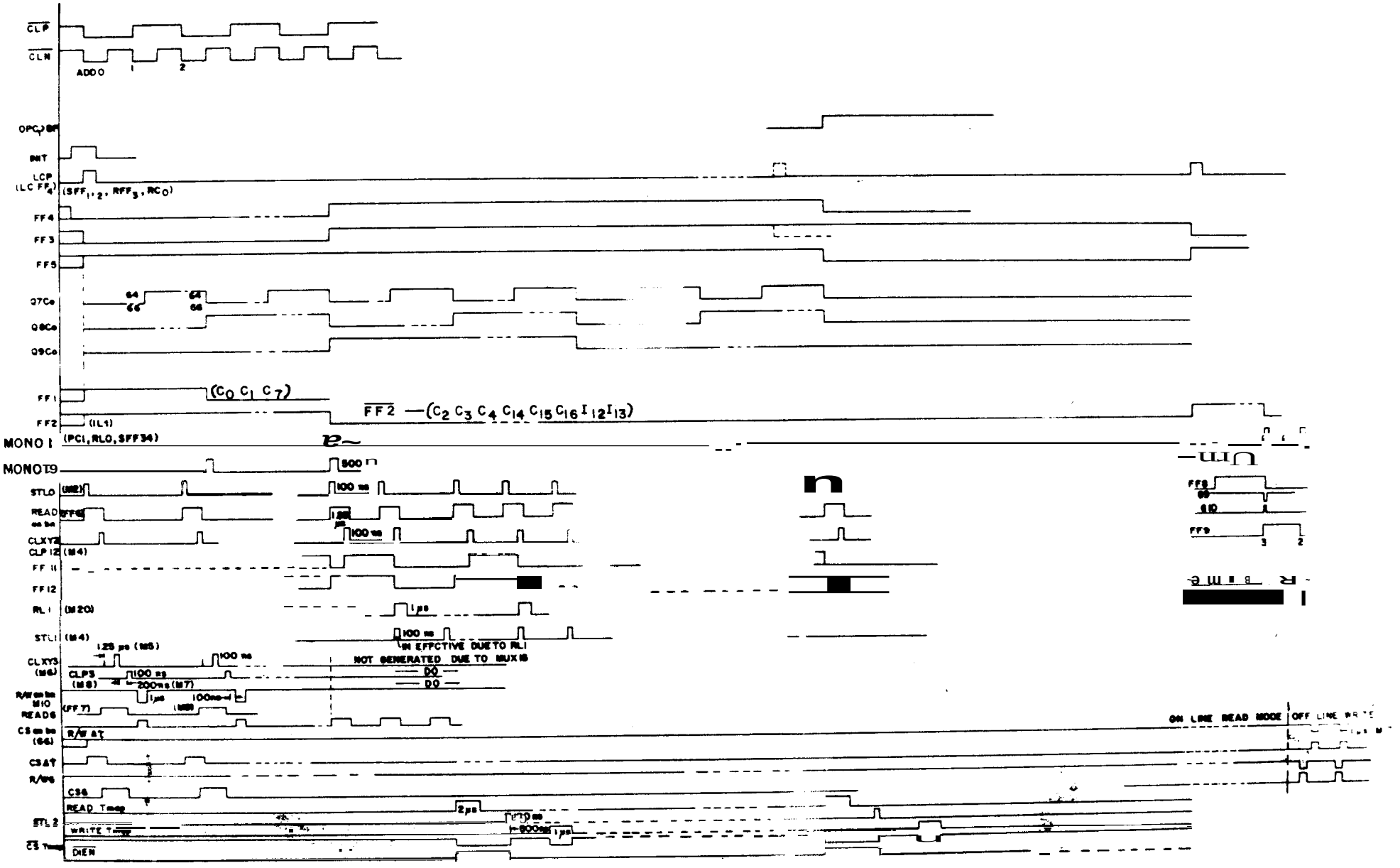


FIG. 4.5 TIMING DIAGRAM OF FOURIER TRANSFORM PROCESSING UNIT.

Gates, G4, along with buffer (BUF 4) gives the signal ENAN, to enable the an-RAM in the processor. Similarly, gate, G5, along with buffer (BUF 5) gives the signal ENBN, to enable bn-RAM. Signal, FF1, of ANFF1 and the signals FF2 and $\overline{FF2}$, from BNFF2 are taken out for controlling different multiplexers in the control circuit to be discussed later. The falling edge of BNFF2 is designed to set up MONO-1 to give the signal, MONO-1.

An over range flipflop, OVRFF3, and normal flipflop NORFF4, are used along with gates, Go, to indicate the alarm condition. LCP pulse from gate, G1, initially resets OVRFF3. Signal, MONO-1, sets up OVRFF3, which is reset only by following LCP pulse. NORFF4, which is reset by the initialise switch on the console is also set up by the signal, MONO-1, and is reset by the signal, OPC1 > BF, at the end of the normal FT operation. Gate, Go, gives the output for the AND logic function of the signals FF3 and FF4. Whenever the alarm condition exists (pre-integration time is set less than processor time) Go output sets up an alarm flipflop, ALFF6, to give the signal, ALMP, to switch on the alarm lamp in the console and also sounds a beeper.

Gate, G2, enables the latch counter pulses, LC, to be counted in the alarm condition and clocks the counter, CPAL. The output of the counter is displayed

on the console to give the count of missing data sets. Both the CPAL and ALFF6 can be reset by the signal RAL from the console.

4.5.3 Generation of argument 'n_θ'

The first block in the pipeline processing is the argument generator, which provides angle θ in the normal FT operation and angle $\Delta\psi$ in the phase correction cycle to the SIN-COS look-up table. An important design facility of this block is to provide the observer a choice of particular beams to be selected in the observation. Another design feature of this block is to provide the address for various RAMs and data multiplexers. The beam number selected for computation is taken out to address the Tmap-RAM. The range of beam numbers to be computed controls the display area on the video monitor.

The signal CLCO, (Fig 4.3) from the clock generator up-counts the counter-0, (Fig 4.6). Q1 to Q7 outputs of Counter-9, are taken as the address bits to control an-RAM and bn-RAM. This enables appropriate correlation coefficients to be fed to the multipliers during processing. These address bits are also taken to the group and channel decoder (Fig 3.6 (b)) , where the bits are suitably decoded to multiplex the correlation coefficients a_n and b_n from the front end of the receiver

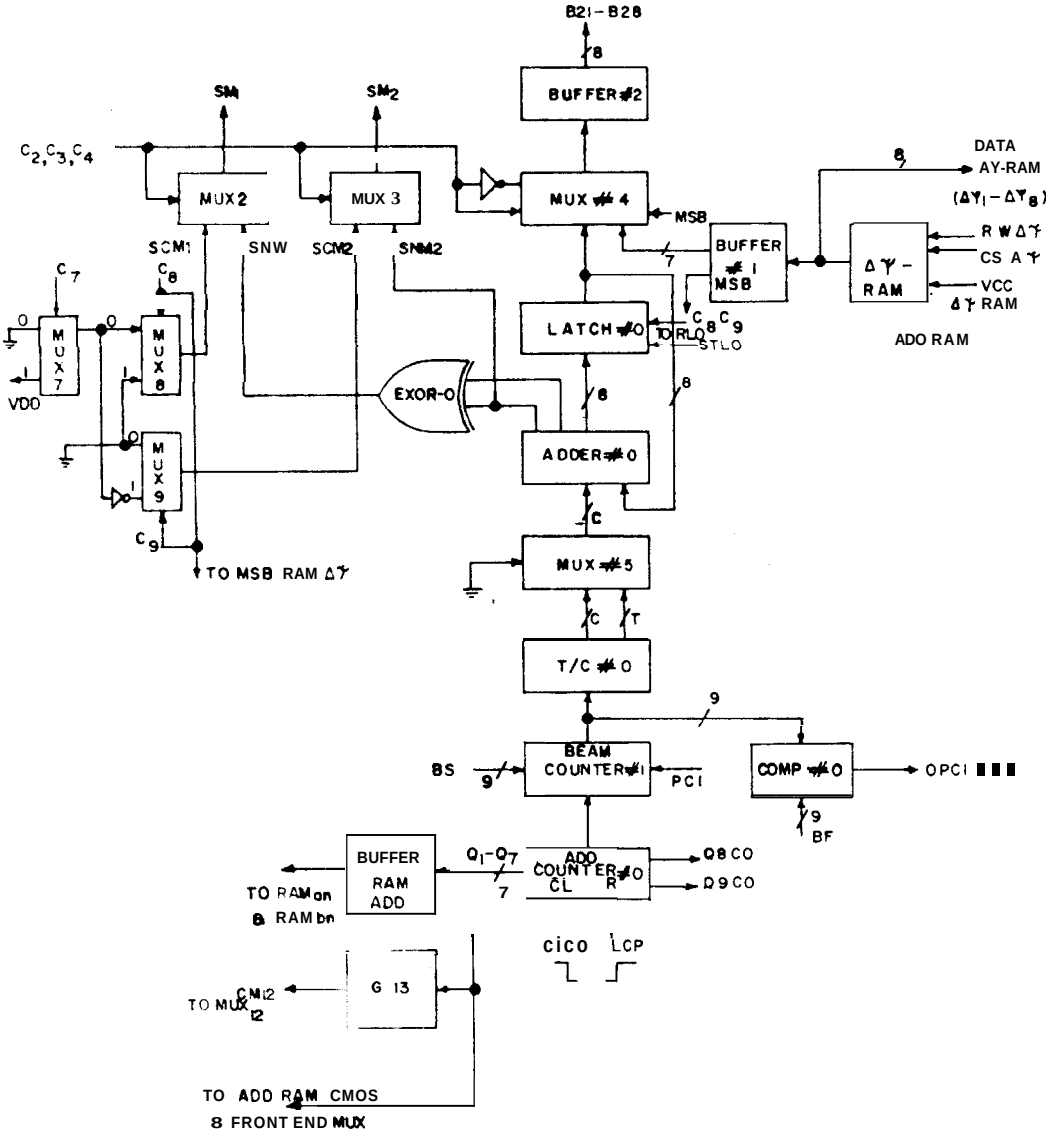


FIG. 4.6. SIGN BIT AND ARGUMENT GENERATION.

to the FT processor. The signal Q8CO and Q9CO from the Counter-0 is taken to the pre-integration time controller as discussed in Sec 4.4.2. Q8 output, Q8CO, from the address generator (COUNTER-0) clocks the beam counter, counter-1. This counter is preset with the number set on the Beam-Start thumbwheel switches (BS) on the console by the signal, PCI, (same as signal, MONO-1, in Fig 4.4).

COUNTER-1 gives the argument in equation(4.1) represented by θ in the computation of brightness distribution. This counter advances by one count for each beam till the number in the counter reaches a value set by the Beam-finish thumbwheel switch (BF) on the console. A 9-bit comparator, COMP-O, detects the condition when COUNTER-1 reaches BF value, and generates a signal, OPC1 > BF, which'resets flipflops, ~~ANFF1~~ NORFF4 and ~~BNFF2~~ CLFF5 (Fig ~~4.3~~ 4.4). Thus the computation for all the beans starting from BS to BF in increments of unit steps is carried out.

Beam numbers are counted from the horizon in the North going through the zenith to the other horizon in the south, and designated as beam numbers 0 to 511. Since the angle in the euqation (4.1) is reckoned from the zenith, the beam numbers given as output from the

COUNTER-1 is complemented to give the zenith angle. The true-complement circuit, T/C-0, gives both the true and the complement output of the COUNTER-1. A multiplexer, MUX-5, enables complement output to be taken to give the zenith angle in normal FT processing. Provision is kept to choose the true output of COUNTSR-1 in any other application of the system.

The output from the MUX-5 is taken through adder, ADDER-0, to give the zenith angles θ, 2θ, 3θ, ... $n\theta$ ...., 128θ, for the corresponding a_n's and b_n's. This is generated by first latching the ADDER-0 output at every address clock-pulse. Latch circuit, LATCH-0, gives the zenith angle, $n\theta$, at the nth clock-pulse of address generation for a particular beam. The output from the LATCH-0 goes directly to address the COS and SIN tables in the normal operation. The rising edge of the Q7 output from the COUNTER-0, Q7C0, triggers the MONO-RLO (Fig 4.3) to issue a 200 ns pulse, RLO, to reset LATCH-0 and starts computing for each beam. In addition, the LATCH-0 output is given to the other input of the ADDER-0. This facilitates the generation of $n\theta$ value at LATCH-0, when the strobe pulse, STLO, is issued. The rising edge of CLNP, pulse

(Fig 4.3) triggers the MONO-STLO, (Fig 4.5) to give a 100 ns pulse, STLO. The RLO and STLO pulses are thus properly phased to give the arguments for COS and SIN tables in the pipeline design.

The multiplexer, MUX-4 (Fig 4.6) allows the output from the $\Delta\psi$-RAM in the correction mode and the output from LATCH-0 output in the normal mode to address the COS and the SIN tables. BUFFER-1 is used to convert TTL signal levels of the $\Delta\psi$-RAM to CMOS levels. BUFFER-2 converts the CMOS level of the MUX-4 back to TTL level to address the COS and SIN tables.

4.5.4 Generation of Sin $n\theta$ and Cos $n\theta$

The multiplexers, MUX-0 and MUX-1 (Fig 4.7) connect the SIN/COS tables to the multipliers, M1 and M2 depending on the mode of operation. The signal FF1 (Fig 4.4) is connected as the control signals, C0 and C1, for MUX-0 and MUX-1. Multiplexers, MUX-10 and MUX-11 (Fig 4.7) control the true or 2's complement output depending on the sign bits, SM1 and SM2. The sign bit generation is discussed separately in a different section. The buffers, BUF-3 and BUF-4 convert TTL levels from the SIN/COS ROMs to CMOS levels, while BUF-5 and BUF-6 convert the signals back to TTL levels

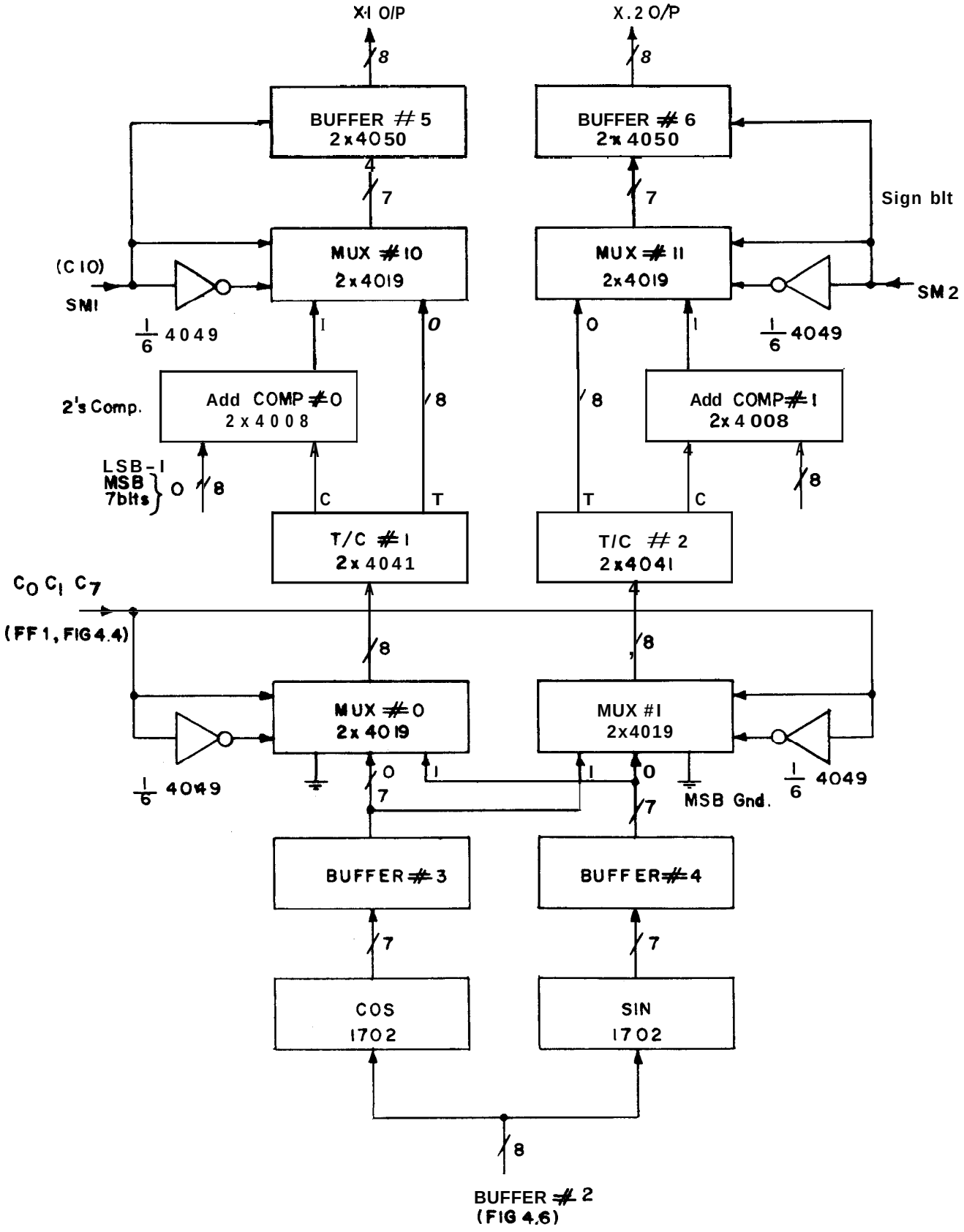


FIG. 4.7. GENERATION OF COS nθ & SIN nθ.

to drive the multipliers. The detailed circuit diagram for generating the 2's complement values is given in the figure.

Control circuits for the SIN/COS look-up tables are designed with minimal logic by enabling the ROMs throughout the operation. However, care has to be taken in the design to allow for the access time of these ROMs. In the present design, after setting up the address $\Delta\psi_n$ for these tables, multipliers, M1 and M2, are clocked after allowing the access time of the ROMs and propagation delays in all the intermediate circuitry discussed above. This timing was one of the important factors in the design of the cycle timing of each stage in the pipeline design.

4.5.5 Generation of Fourier terms

4.5.5.1 Phase correction mode of operation

In the phase correction mode of operation, the measured correlation coefficients a_n' and b_n', are given phasor rotation as already mentioned in Sec. 4.4 This is done in two passes. In the first pass, the sine correlation coefficient, b_n, is obtained during the first 128 clock pulses by implementing the equation (4.2) for b_n.

In the second pass, the Cosine correlation coeffi-

cient, a_n, is obtained during the next 128 clock pulses of the phase correction mode by implementing the equation (4.2) for a_n.

The equation for correcting a_n is similar to normal FT operation given in equation (4.1). Hence the sequence of the ebove two passes, first for b_n and then for a_n, enables the control circuitry to change from phase correction mode to normal mode without any delay.

An important design feature of the processor is to implement the on-line phase correction with the hardware designed for normal FT operation. Phase correction and normal FT operation are time multiplexed utilising the same hardware. The control signals are suitably generated to control the various circuits, so that the signals are properly routed. The signal path in the phase correction node is as shown in Fig 4.1. In this node, the multiplexers, MUX-12 and MUX-13 enable a_n^1 and b_n' to appear on the bus, Y1 and Y2, of the multipliers, M1 and M2, respectively. The other operands for the multipliers are Cos $\Delta\psi_n$ or Sin $\Delta\psi_n$ depending on correcting a_n or b_n. The two products from M1 and M2 are added at ALDER-1, and wei-hted by the multiplier, M3. The output from M3 is multiplexed through MUX-12 and MUX-13 to an-RAM AND bn-RAM res-

pectively. As already mentioned in the first pass, b_n' is corrected and stored in bn-RAM, and then in the second pass, a_n' is corrected and storea in an-RAM. During the first 128 clock pulses the bn-RAM is enabled by the signal ENBN through gate, G5 (Fig 4.4) and in next 128 clock pulses an-RAM is enabled by the signal ENAN through gate, G4 (Fig 4.4).

The zero spacing component, a_o, sometimes called the d.c. component is weighted by half and added with the other correlation coefficients, a_n and b_n in the Fourier summation given by the equation(4.1) .The coefficient a_o has to be stored directly into the an-RAM without any correction being applied, while a_n' and b_n' need phase correction. MUX-12 (Fig 4.8) is a 4 channel multiplexer enabling a_n' in the channels 1 and 3, d.c. component, a_o ,in the channel 2, and Multiplier, M3, output in the channel 0. MSB of the channel control bit, CM12, of the MUX-12, is taken from a NOR gate which detects zero address count, while CLP clock pulses (Fig 4.3) are given as the LSB channel control bit,.CL12. Multiplexer, MUX-14, enables CLP clock to pass on through gate, G3, in the phase correction cycle. This control enables a_o to be stored directly in the zeroth

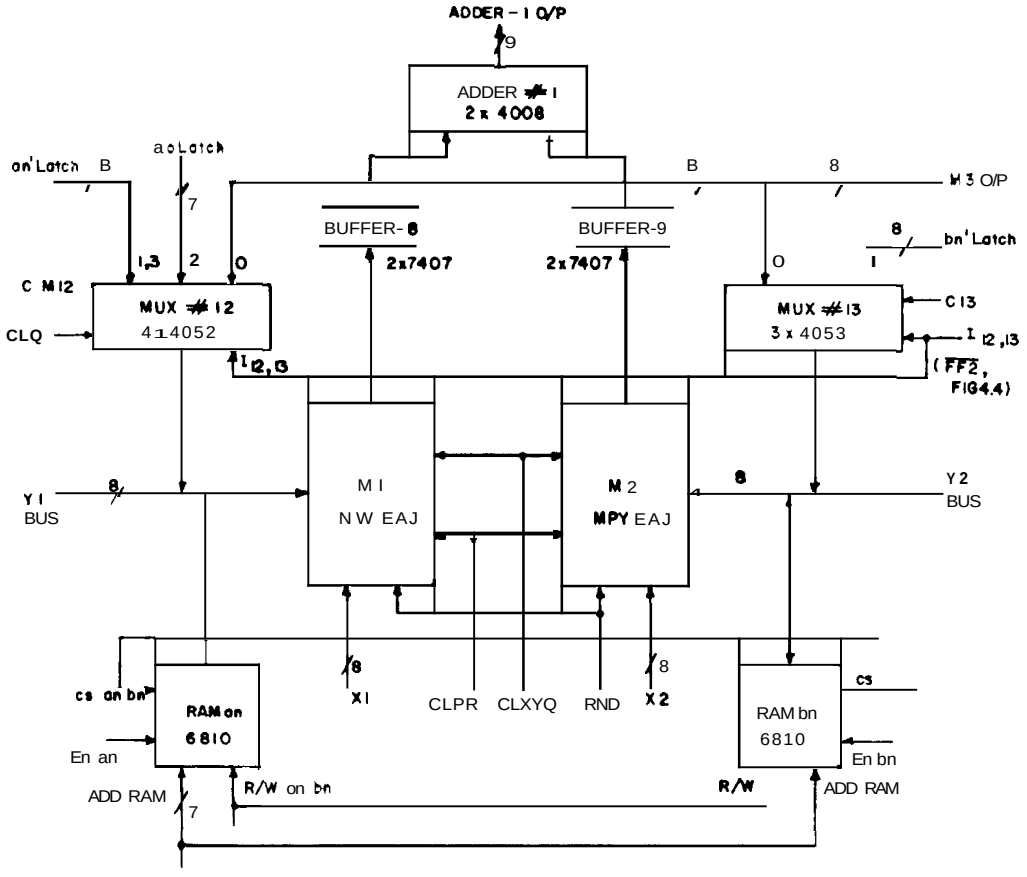


FIG. 4.0 GENERATION OF (on Con nθ + bn Sln nθ)

location and a_n' to be phase corrected and stored in first location onwards in the an-RAM. MUX-13 is only a two channel multiplexer, since either the b_n' or M3 output has to be enabled to the bus Y2, of the multiplier, M2. CLP clock pulses are connected here also as the control bit, 013, of the MUX-13.

MUX-12 and MUX-13, are enabled only in the correction mode and so are connected to the signal, $\overline{FF2}$ (Fig 4.4), through the inhibit pins I12 and I13 (Fig 4.8) of the multiplexers. With a 50 per cent duty cycle of the CLP clock pulses, the correction mode works in the following way:

1) The signals, CM 12 and CL12, initially connects a_n to bus Y1 and the signal, 013, connects b_n' to bus Y2 for 3 µs during the high level of CLP clock pulse. It is very important that at this time, other inputs connected to Y1 and Y2 bus are inhibited. The an-RAM and bn-RAM are inhibited during the read operation of the $\Delta\psi$-RAM in the correction mode.

2) The 200 ns clock pulses, CLXY12, of the multipliers, M1 and M2, come after 1.75 µs (Fig 4.9B) after setting the address from the address generator and hence data is settled after the $\Delta\psi$-RAM read pulse. MONO-3 (Fig 4.9A) gives the delay of 1.75 µs and MONO-4 gives a 200 ns pulse which is taken as CLXY12. The clock pulses for the multipliers are unchanged

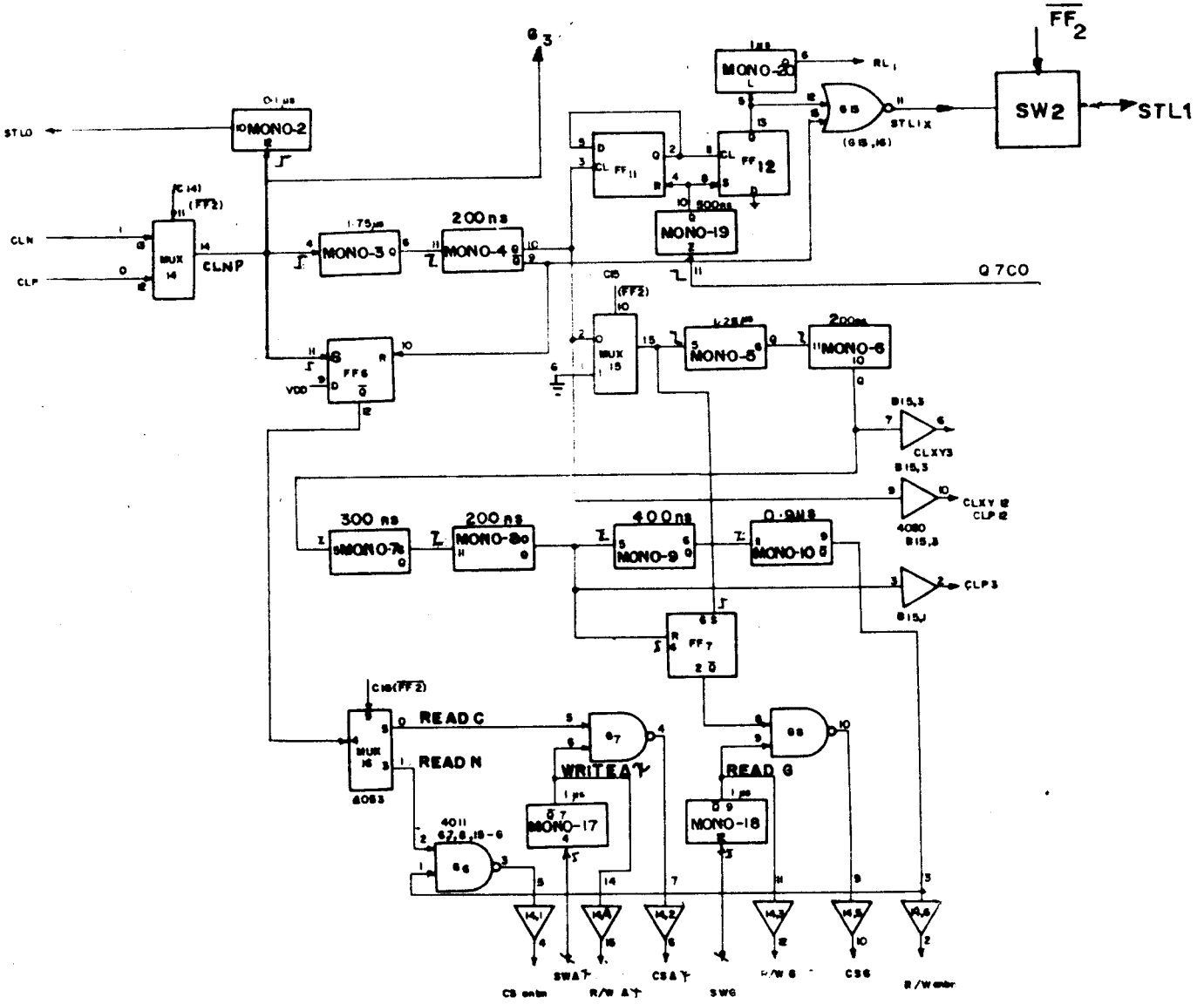


FIG. 4.9A GENERATING CONTROL SIGNALS (A-RAM, G-RAM & ADDER/LATCH CIRCUITS).

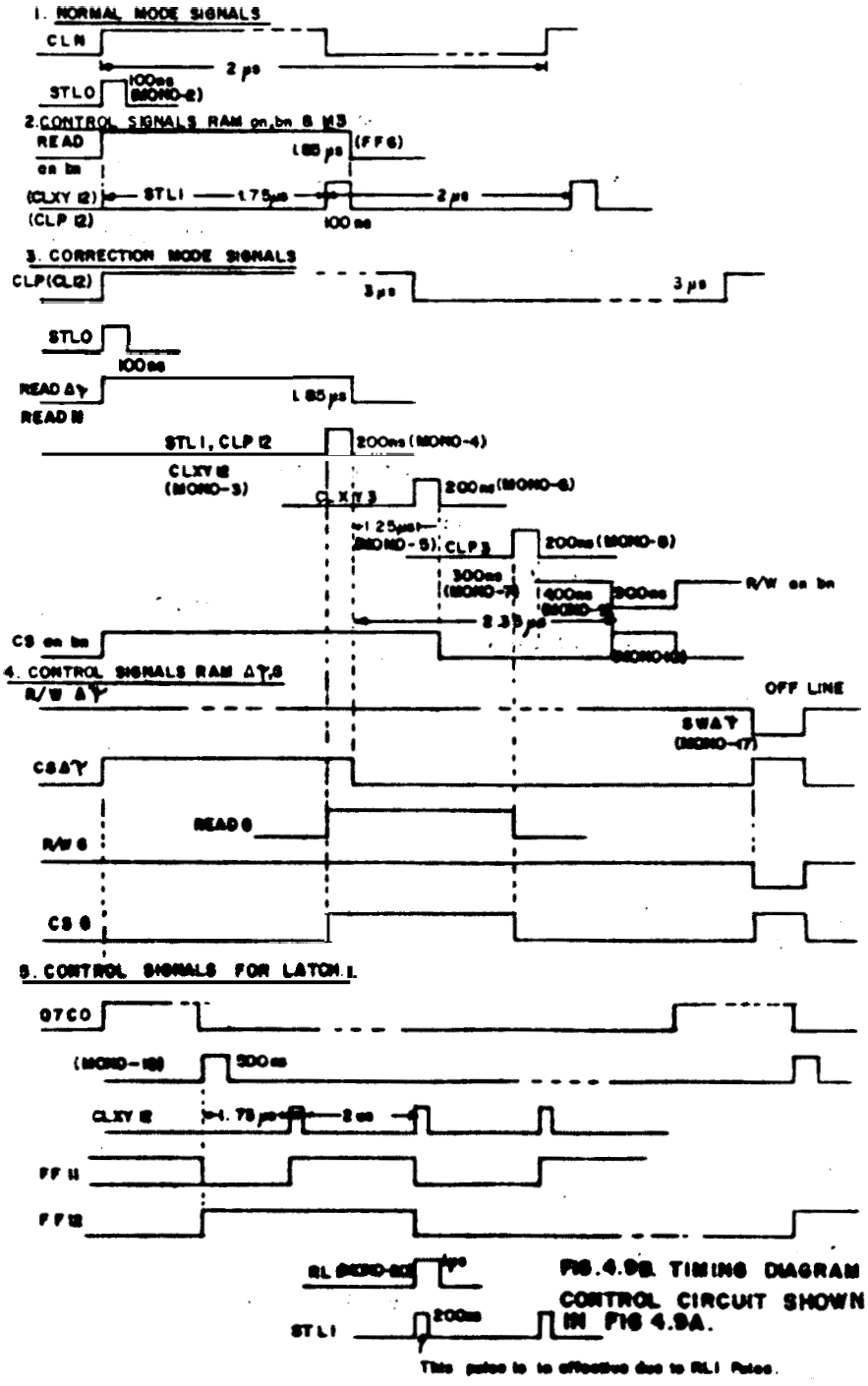


FIG.4.9B TIMING DIAGRAM OF CONTROL CIRCUIT SHOWN IN FIG 4.9A.

in the normal mode of operation and also, when the an-RAM and bn-RAM are enabled. This design facility utilises the same control circuitry in both the modes of operation.

3) Write pulses, R/W an bn (Fig 4.9B) for the an-RAN come 2.35 μs later than the CLXY12 pulse, so as to allow multiplication time for M3 and propagation delay in the intermediate circuitry including that of MUX-12.

4.5.5.2 Normal mode of operation

The signal flow paths for generating a_n Cos $n\theta$ and b_n Sin $n\theta$ are shown in Fig 4.1 . In this mode, MUX-12 and MUX-13 are inhibited by the signals I12 and I13, which are at high level. The output from the an-RAM is connected to M1 through bus Y1 and similarly the output from the bn-RAM is connected to M2 through bus Y2. The other inputs for the multipliers are designed to be same in both modes of of operation, the argument, $n\theta$, is latched at A/L-O in the normal mode of operation providing a separate stage in the pipeline process design. Sign bit generation for the arguments in this mode is separately discussed.

Since the hardware for the signal flow is designed to be the same in both the modes of operation, the control

circuitry for generating the clock pulses for multipliers and read/write pulses for the an-RAM and bn-RAM are suitably designed as discussed later in Sec 4.5.5.7.

4.5.5.3 Sign bit generation in phase correction mode

Sign bit in correction phase is generatea according to the table 1 given in Fig 4.10. Sign bits, SCMI and SCM2, for the two multipliers are given for the two cases of $+\Delta\psi$ or $-\Delta\psi$. These two cases are distinguished in the hardware by storing 0 in the case of $+\Delta\psi$ and 1 in the case of $-\Delta\psi$ in the most significant bit of the $\Delta\psi$-RAM. Multiplexers, MUX-8 and MUX-9 (Fig 4.6) control the two cases. The MSB of the $\Delta\psi$-RAM is taken as the control signal C8 and C9 for these two multiplexers. Consider first the case of $+\Delta\psi$. SCM1 and SCM2 have to be set as 1, 0 in the first pass, and 0, 0 in the second pass as given in the Table - 1 (Fig 4.10). This is achieved by setting the data inputs and control inputs of the multiplexers MUX-7, MUX-8 and MUX-9 as shown in Fig 4.6. The signal FF1 (Fig 4.4) is connected as the control signal, C7, for the multiplexer, MUX-7. This multiplexer sets the sign bits in the two passes. In the first pass, the control signal, C7, is high. This enables the second

TABLE I Sign bit in phase Correction Mode.

Sign bit for Multiplier	Case 1: $+\Delta\Upsilon$ ($0° < \Delta\Upsilon < 179°$) MSB of $\Delta\Psi$-RAM = 0		Case 2: $-\Delta\Upsilon$ ($180° < \Delta\Upsilon < 359°$) MSB of $\Delta\Psi$-RAM = 1	
SCM1	bn I pass −(1)	anII pass +(0)	bn I pass +(0)	anII pass +(0)
SCM2	+(0)	+(0)	+(0)	−(1)

TABLE II Sign bit in normal mode.

ADDER 0		SIGN BIT FOR MULTIPLIERS	
9 bit	8 bit	SN M1	SN M2
0	0	0	0
0	1	1	0
1	0	1	1
1	1	0	1

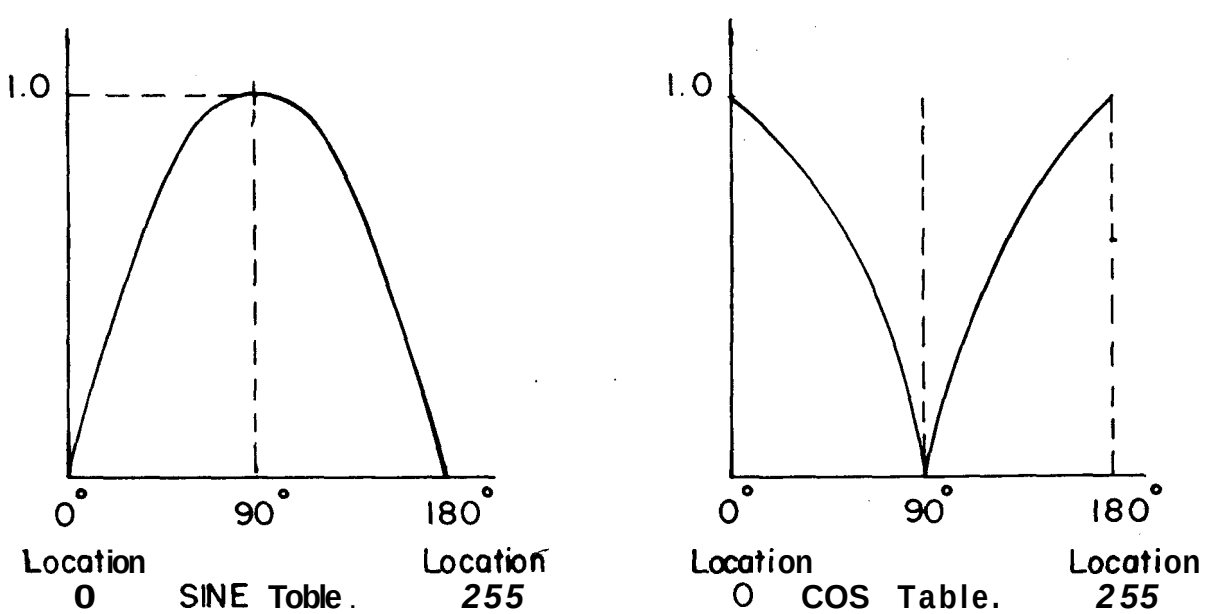


FIG 4.10 SIGN BIT GENERATION.

input, which is permanently connected high to set the output of MUX-7 as high. The output of MUX-7 is connected to the first output of MUX-8. For the case of $+\Delta\psi$, the control signal, C8 and C9 are low, enabling the first inputs of MUX-8 and MUX-9. Thus SCM1 goes high in the first pass and low in the second pass, as the first input of MUX-7 is grounded. The first input of MUX-9 is connected to ground, and hence SCM2 is low in both the first and the second pass.

In the second case of $-\Delta\psi$, C8 and C9 are high, enabling the second inputs of MUX-8 and MUX-9. SCMl is low in both the passes, as the second input is returned to ground. SCM2 is low in the first pass and high in the second pass as the output of MUX-7 is inverted and given as the second input of MUX-9, thereby generating 0, 0 in the first pass and 0, 1 in the second pass as the sign bits. Thus with simple multiplexers, a definite pattern of sign bits are generated in the phase correction mode as required.

4.5.5.4 Sign bit generation in normal mode

The SIN/COS tables are stored in 256 byte ROMs. Values corresponding to the range 0° to 180° are stored in these 256 locations with eaual intervals of angles, thereby giving a resolution for the look-up table of

$\approx 0.7^{\circ}$ approximately. Positive values are stored in the tables for all the 180° as shown in Fig 4.10. The sign bit is generated in normal operation depending upon the quadrant in which the $n\theta$ value of the argument falls. **ADDER-0** gives a 9 bit output (Fig 4.6) for the angle, $n\theta$, to cover all the 360° in 512 values. The most significant two bits of ADDER-0 output is used to give the quadrant of the angle, $n\theta$. Table-2 in Fig 4.10 gives the sign bit for different quadrants.

The sign bit for the M2, SNM2, is given directly from the **MSB** of the ADDER-0 output. The sign bit for M1, SNM1, is obtained by taking the most significant two bits through an exclusive-or gate, EXOR-0, as shown in Fig 4.6.

Although 256 byte long **EPROMs** were the only choice for look-up tables at the time when the system was planned, present day EPROMs with higher memory capability do not give any simpler control hardware.

4.5.5.5 Storage of DC component

Fig 4.11 gives the schematic for entering the dc component a_0 into the an-RAM as already mentioned. In the second pass of phase correction mode, when the address is **zero**, the first CLXY12 pulse enters a_1 (first spatial frequency component) from latch a_n' through the BUS-Y1.

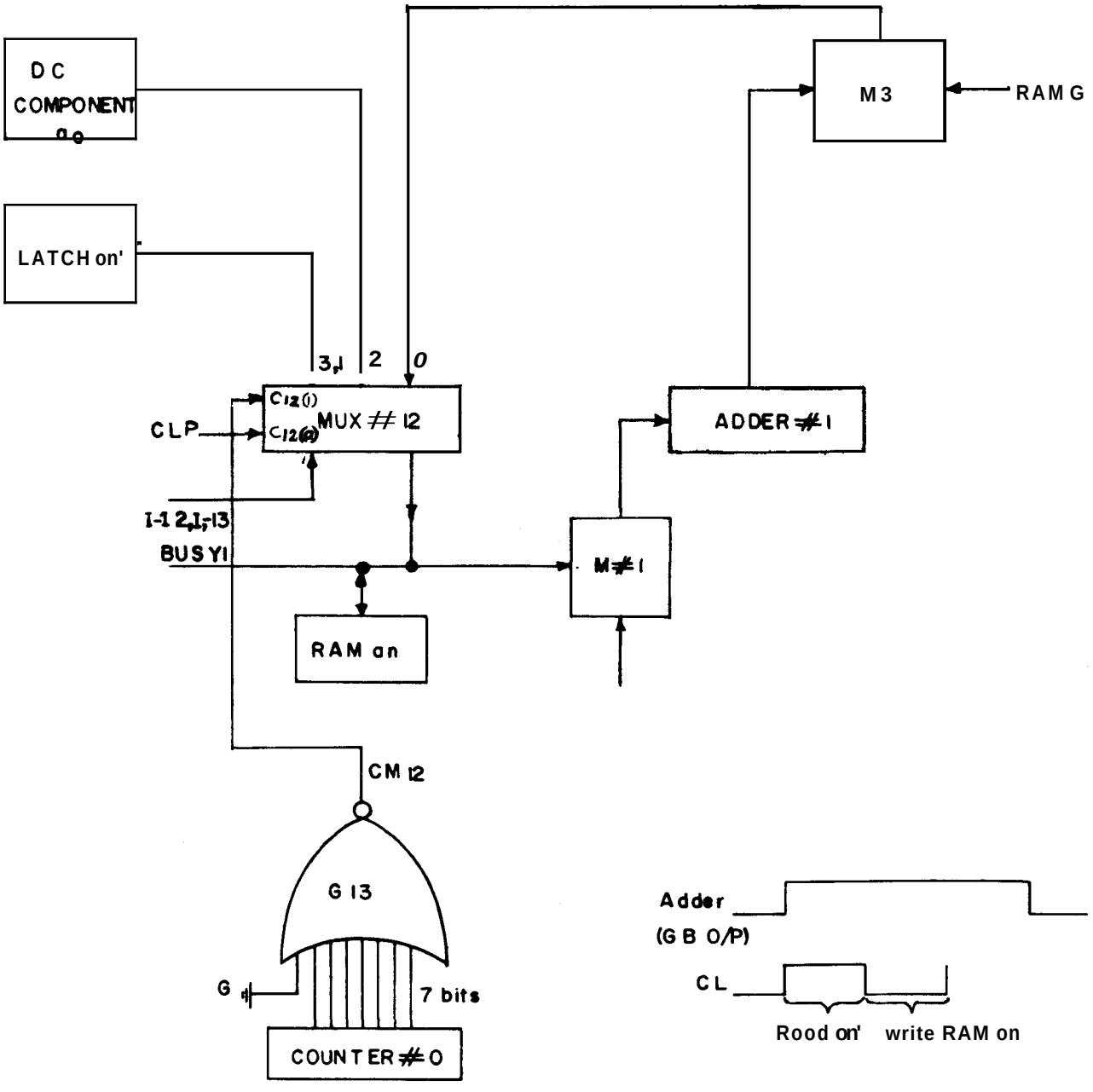


FIG.4.11. DC 'COMPONENT STORAGE.

This is because the address control for MUX-12 is 3 as CM12 is high for the address count 0 and CL12 (CLP) is also high (Fig 4.9B) for 3 μs in the first address cycle. The phase correction angle is given by the Δψ - RAM and the propagation delay is less than 1.75 μs to reach the multiplier input. Hence the first location in the A+-RAM corresponds to the phase correction angle corresponding to the first element. At the same time, the output clock pulses at the multipliers M1 and M2, CLP12, take the product of invalid data to M3. The output of M3 is however not taken in, since CL12 has changed to low after 3 μs and the control addrees for MUX12 is now 2 for the remaining 3 us in the first address cycle, thereby allowing a_o to reach BUS-Y1. Before the end of the first address cycle, the control signal R/W an bn, (Fig 4.9B) writes a_o into the 0th location of the an-RAM. In the first pass of the phase correction mode with the above design of the control circuitry, the bn-RAM is enabled and some invalid data enters into the first location of the bn-RAM, which is not correct. A zero can be entered into first location of the bn-RAM by having a zero placed in the first location of the grading function. This will ensure 0 at the M3 output in the first address cycle of the phase

correction mode.

4.5.5.6 Implementation of the grading function

The phase corrected correlation coefficients, a_n and b_n, are weighted by a grading function if required. There is a choice of 6 grading functions, four of which are stored permanently in ROMs and two grading functions are stored in RAMs.

Fig 4.12 gives the circuit for implementing the grading function. The output of ADDER-1 (Fig 4.1) is connected as one input of the multiplier, M3, through BUF-9, which converts signals from CMOS levels to TTL levels. The other input of M3 is connected to grading data bus, BUS-G. Two RAMs (6810), G1 and G2 are memories where the grading function is temporarily stored. Two ROMs (Intel 1702) provide four grading tables, G3 to, G6. Addresses for both the RAMs and ROMs are connected to the output of the address generator, COUNTER-0 (Fig 4.1). Selection of the particular function is provided by the thumbwheel switches, on the console. The MSB 8 bits of the output of the multiplier, M3 are converted to CMOS level by BUF-10, which goes to MUX-12 for writing in the an-RAM and the bn-RAM as already discussed in earlier sections.

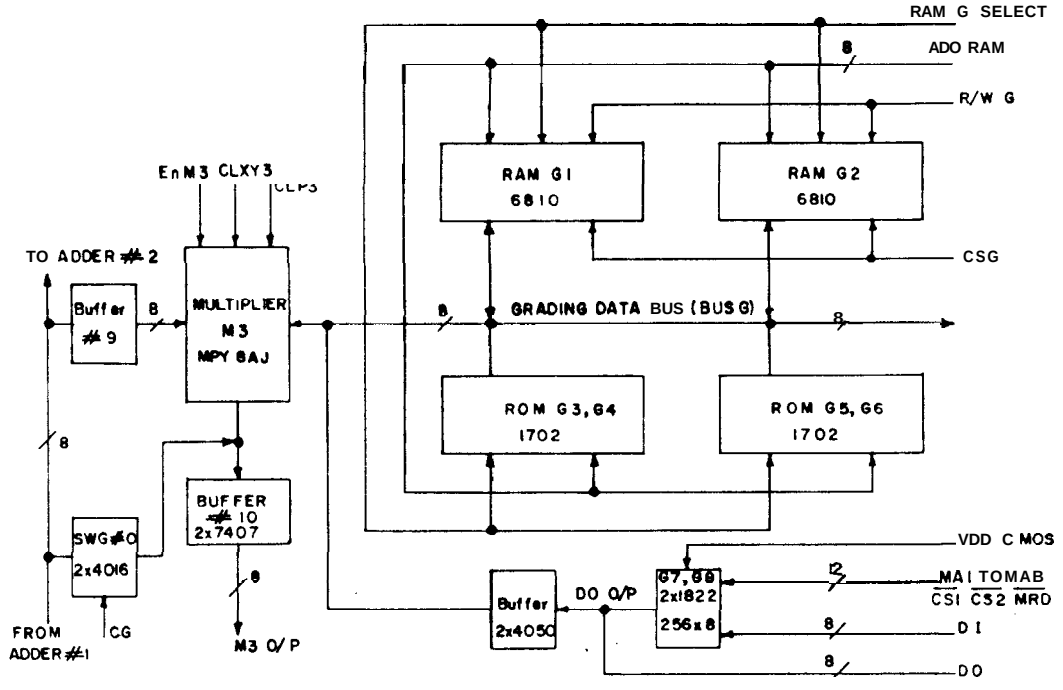


FIG. 4.12 . GRADING FUNCTION IMPLEMENTATION.

Two CMOS RAMs (RCA 1822) provide two more grading functions, G7 and G8, which are connected with the back-up power supply. This feature avoids data entry repeatedly into these memories in case of power failures.

The grading function can be bypassed by the signal, CG, which connects ADDER-1 output to BUF-10 input directly. Simultaneously, M3 is disabled by the signal, ENM3. Both these signals are generated under console control.

A 200 ns long input clock signal, CLXY3, of the multiplier, M3, is provided by MONO-6 (Fig 4.9A), after a delay of 1.25 μs from the output clock signal CLP12, of the multipliers, M1 and M2. This takes care of the propagation delay of BUF-9 and ADDER-1 circuits. The output clock signal, CLP 3, of multiplier M3, is given after 300 ns from the signal, CLXY3, to allow for the multiplication time in M3. MONO-7 gives the necessary delay of 300 ns, while MONO-8 gives a 200 ns long CLP3 pulse. The signal, R/Wanbn, of 900 ns length is generated after a delay of 400 ns to allow for delays in BUF-10 and MUX-12. MONO-9 gives the delay of 400 ns, while MONO-10 gives 900 ns long R/Wanbn. All these timings are considered in the pipeline process design.

4.5.5.7 Control signals for Read Write Memories

Control signals for the an-RAM and the bn-RAM

Write pulses are produced only in the correction mode, since MUX-15 (Fig 4.9A) allows output of the MONO-4 to be applied to MONO-5. R/Wanbn is taken from the output of MONO-10 as already mentioned in an earlier section. The Flip-Flop, FF6, gives read pulses, which are set by the low to high transitions of the CLNP pulses and are reset by the output of MONO-4. READ pulses are demultiplexed by MUX-16 as READ C pulses in the phase correction mode and READ N pulses in the normal mode of operation. Chip select signal, CS anbn is given by the logical OR function of READ N and R/W anbn signals. Only READ N pulses are gated to CSanbn by gate, G6, the other input being R/W anbn from MONO-10. This is connected to chip select pin of an-RAM and bn-RAM. The signals ENAN (Fig 4.4) ENBN are given to other chip select pins of an-RAM and bn-RAM respectively.

Control Signals for the $\Delta\psi$ -RAM

MONO-17 (Fig 4.9A) is used for generating the R/W $\Delta\psi$ signal in the OFF line mode. R/W $\Delta\psi$ is taken from the $\overline{Q}$ output of MONO-17 and is normally in the high state thereby enabling read operation of the RAM.

The chip select signal, CS is obtained by logical OR function of the READ C pulse and the R/W $\Delta\psi$ pulse. Gate, G7, provides this OR function either by connecting the MONO-17 output or the FF6 output through MUX-16.

Control Signals for the G-RAM

The $\overline{Q}$ output of MONO-18 provides a R/W G signal, which ia normally high enabling read operation of the RAM. The signal CSG is obtained by the logical OR function of the Read G pulse (obtained from FF7 during the grading cycle operation) and the R/W G pulse. Gate, G8, provides this operation. Fig 4.9B gives timing diagram of all the control signals for the RAMs.

4.5.5.8 Design of pipeline control system

Worst case propagation delays were worked out for the circuit designed, based on the data sheets of the circuits. The figure given in the bracket shows the design value chosen in the system. The propagation delays (Ref Fig 4.1) are as given below:

1. From Adder/Latch, A/L-0, to multipliers M1 and M2 input is 1650 ns (1.75 μs is chosen).

2. From multiplier M1 output to Adder/Latch, A/L-1, input is 1950 na (CLN chosen as 2 μs),

3. From multiplier M1 output to multiplier M3

input is 1060 ns (CLXY13 is chosen as 1.25 μs after CLP12).

4. M3 output to BUS-Y1 is 10 ns (400 ns is chosen, A large factor of safety here does not worsen the speed of processing).

For working out the pipeline processing system, one has to account for invalid data since the data is flowing continuously. The status of the data signal flow with respect to the control signals at the multipliers, M1 and M2, is tabulated where the unprimed terms refer to multiplier M1, and primed terms refer to multiplier M2.

No. of CLXY12 pulses in normal mode	M1 Input	M1 Output	M2 Input	M2 Output	Adder/ Latch, A/L-1, Output
1st	x_0-y_0	invalid	$x_0'-y_0'$	invalid	invalid
2nd	x_1-y_1	x_0-y_0	$x_1'-y_1'$	$x_0'-y_0$	invalid
3rd	x_2-y_2	x_1-y_1	$x_2'-y_2'$	$x_1'-y_1'$	$x_0y_0+ x_0'y_0'$
4th	x_3-y_3	x_2-y_2	$x_3'-y_3'$	$x_2'-y_2'$	$x_1y_1+ x_1'y_1'$

The strobe pulse for A/L-1 is derived from the CLXY12 pulse (Fig 4.9B). From the above table, it is seen that the third CLXY12 pulse should be the effective strobe pulse for A/L-1 when proper output is available. This

is accomplised by Flip Flops, FF11 and FF12 and mono-stables, MONO-19 and MONO-20 (Fig 4.9A). The timing diagram is given in Fig 4.9B. MONO-19 generates a 500 ns pulse at the falling edge of the Q7C0 pulse. FF11 provides a toggle circuit which is reset by the MONO-19 pulse and toggled by the CLXY12 pulse. FF12 is set by the MONO-19 pulse and reset by the high to low transition of the FF11 pulse. The high to low level transition of FF12 triggers MONO-20 in generating a 1 μs reset pulse for A/L-1 (RL1). Now the CLXY12 pulses are ANDED with the $\overline{FF12}$ signal to produce a strobe pulse, STL1X, for A/L-1 from the second CLXY12 onwards. However the first STL1X is ineffective because of simultaneous production of the RL1 and STL1X pulses. Hence the STL1X pulses are allowed only in the normal mode by the SW2 switch as signal STL1. This ensures retention of data at the A/L-1 output in case the phase correction cycle starts immediately. In this worst case, when the pre-integration period just starts after computation, the STL1 pulses in phase correction mode can destroy the previous added value, since the A/L-1 output is taken after some time.

4.5.5.9 POST-Integration Scheme and Tmap-RAM

Fig 4.13 gives the schematic for providing the post-integration tine, which is selectable from the console as mentioned earlier. Fig 4.14 gives the schematic of the Tmap-RAM. Tmap-RAM is a 512 by 16 bit

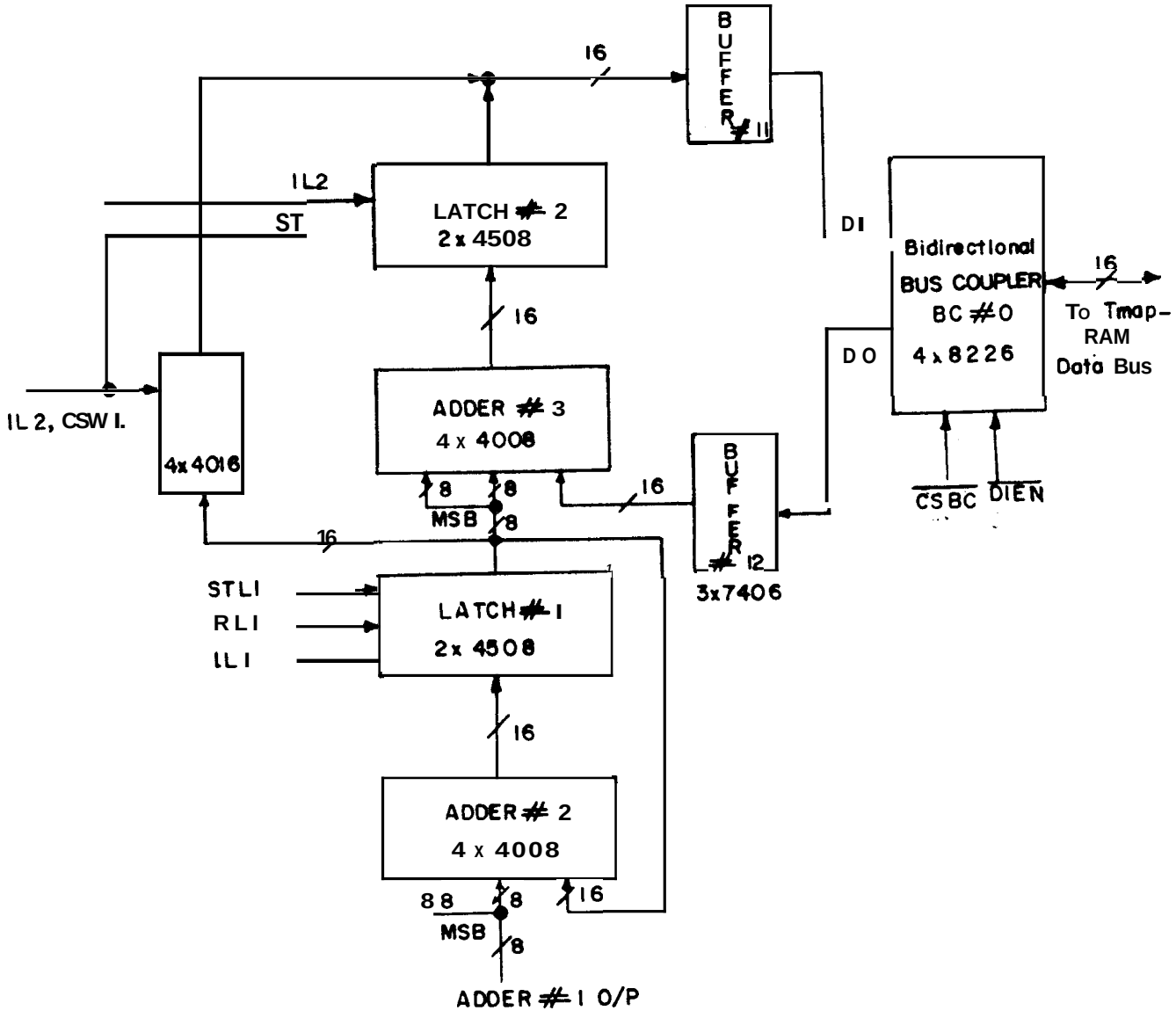


FIG. 4.13. POST – INTEGRATION IMPLEMENTATION.

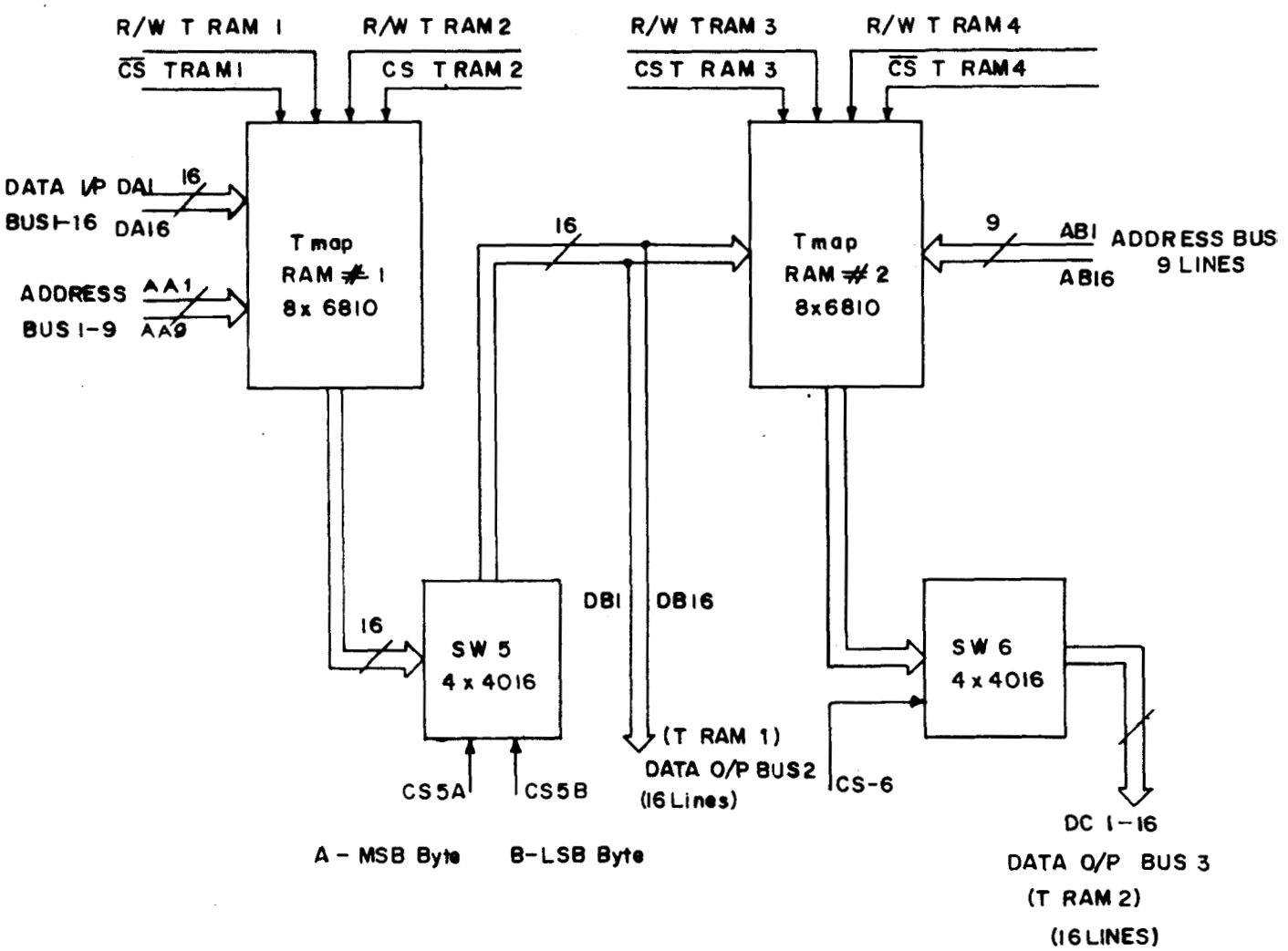


FIG. 4.14 T MAP - STORAGE

memory formed by 8 chips (Motorola 6810) having an organisation of 128 bytes each. They are formed from two banks of 512 bytes long by suitably conbining through control signals R/WTamp 1 and 2 and CSTmap 1 and 2. There are 2 sets of 512 by 16 bit RAMs going through bilateral switches for connecting Tmap-RAM in the buffer mode. The data bus having 16 bits is connected through a bus coupler, while the address bus having 9 bits is connected from LATCH-3 Output (Fig 4.15) corresponding to the bean number.

Fig 4.15 gives the circuit diagram of the control circuit. The MONO-19 pulse (Fig 4.9A) triggered by the falling edge of Q7CO allowed in the normal mode through SW3 to strobe the counter-1 output of LATCH-3. 'Chis provides the address for Tmap-RAM, which is held valid till the next falling edge of Q7CO. The address for Tmap-RAM is staggered by half the periocl of Q7CO, enabling pipeline processing. This is achieved by triggering MONO-19 on the falling edge of the Q7CO pulse. Buffer 13 provides TTL Compatible output. SW4 provides facility to address Tmap-RAM externally under console control.

R/W Tmap is taken from the $\overline{Q}$ output of NONO-16, which is always high thus enabling the read operation. The $\overline{\text{DIEN}}$ signal taken from FF10 connects the Tmap-RAM data to one of the **ADDER-3** (Fig 4.13) inputs through the bus coupler, BC-0, the other input being taken

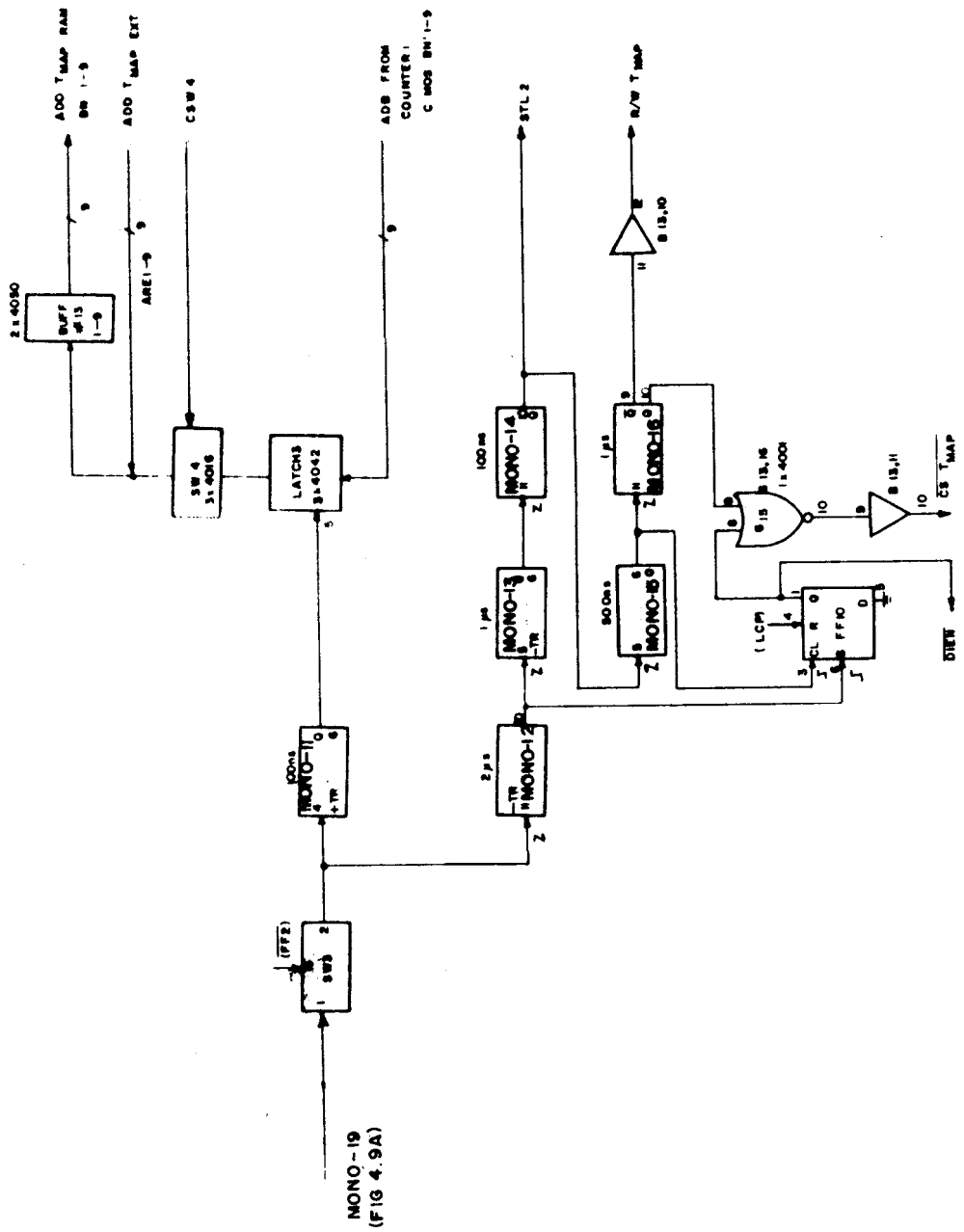


FIG.4.15.GENERATING CONTROL SIGNALS FOR T MAP – RAM.

from the LATCB-1 output. A strobe signal for A/L-2, STL2, is given after a delay of 1 μs to account for the delay in BUF-12 and ADDER-3. Now $\overline{\text{DIEN}}$ is such as to connect LATCH-2 output to the Tmap-RAM through BUF-11 and the bidirectional bus coupler, BC-0. A R/W Tmap pulse of 1 μs is generated after a delay of 500 ns to account for the propagation delay of BUF-11 and BC-0. Chip select signal, CS Tmap, is enabled, both when Tmap-RAM is read i.e. during $\overline{\text{DIEN}}$ signal, and during writing in Tmap-RAM. This is effected by gate, G15, (Fig 4.15). Fig 4.17 gives the timing diagram of the above circuit.

Post-integration control is provided by the circuit shown in Fig 4.16 and the timing diagram for this circuit is also given in Fig 4.17. An intialise pulse from the console sets FF8 and resets FF9. The Q output of FF8 enables the MONO-1 (Fig 4.4) output at the end of the phase correction mode and loads the DOWN COUNTER-2 with the post-integration factor set by the thumbwheel switch at the console. In addition, the MONO-1 pulse resets FF8 and sets FF9 after 2 gate delays of G9 and G10, since the borrow output of the down counter is high. The first MONO-1 pulse going to the clock input of the down counter is ineffective since the preset counter input dominates.

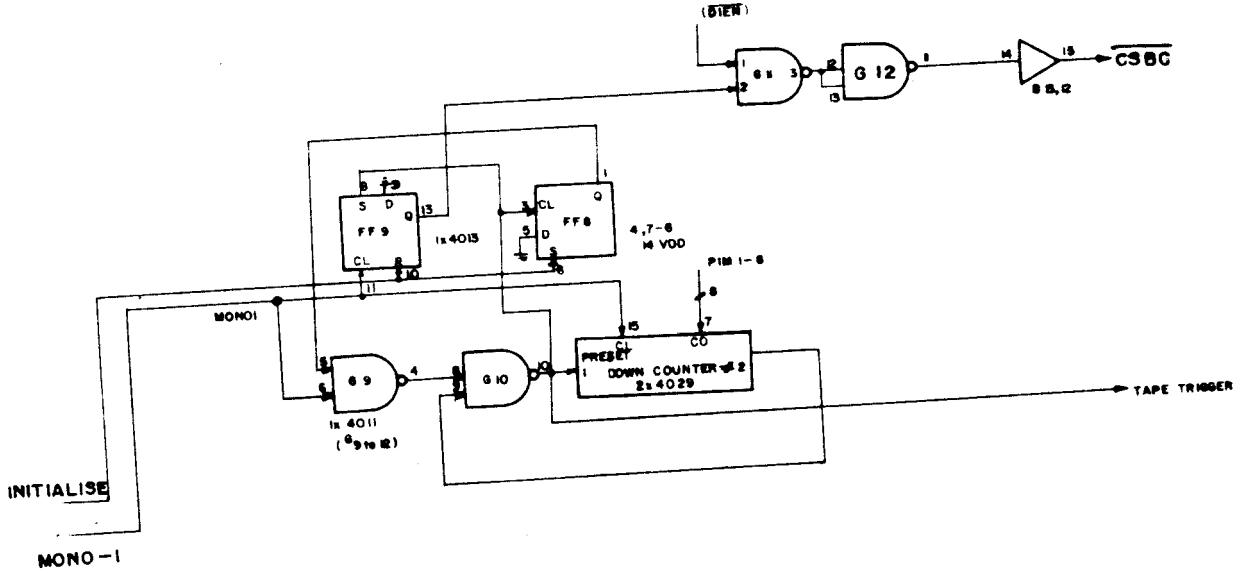
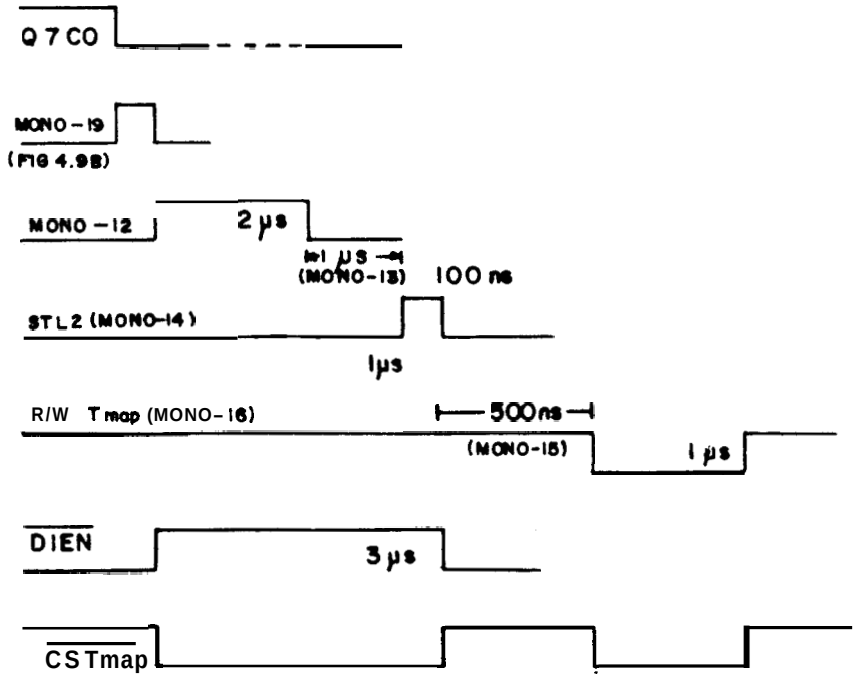


FIG. 4.16 CONTROL CIRCUIT FOR THE TAPE TRIGGER SIGNAL.

((ı) CONTROL SIGNALS FOR Tmap RAM



(b) CONTROL SIGNALS FOR TAPE TRIGGER & BIDIRECTIONAL BUS

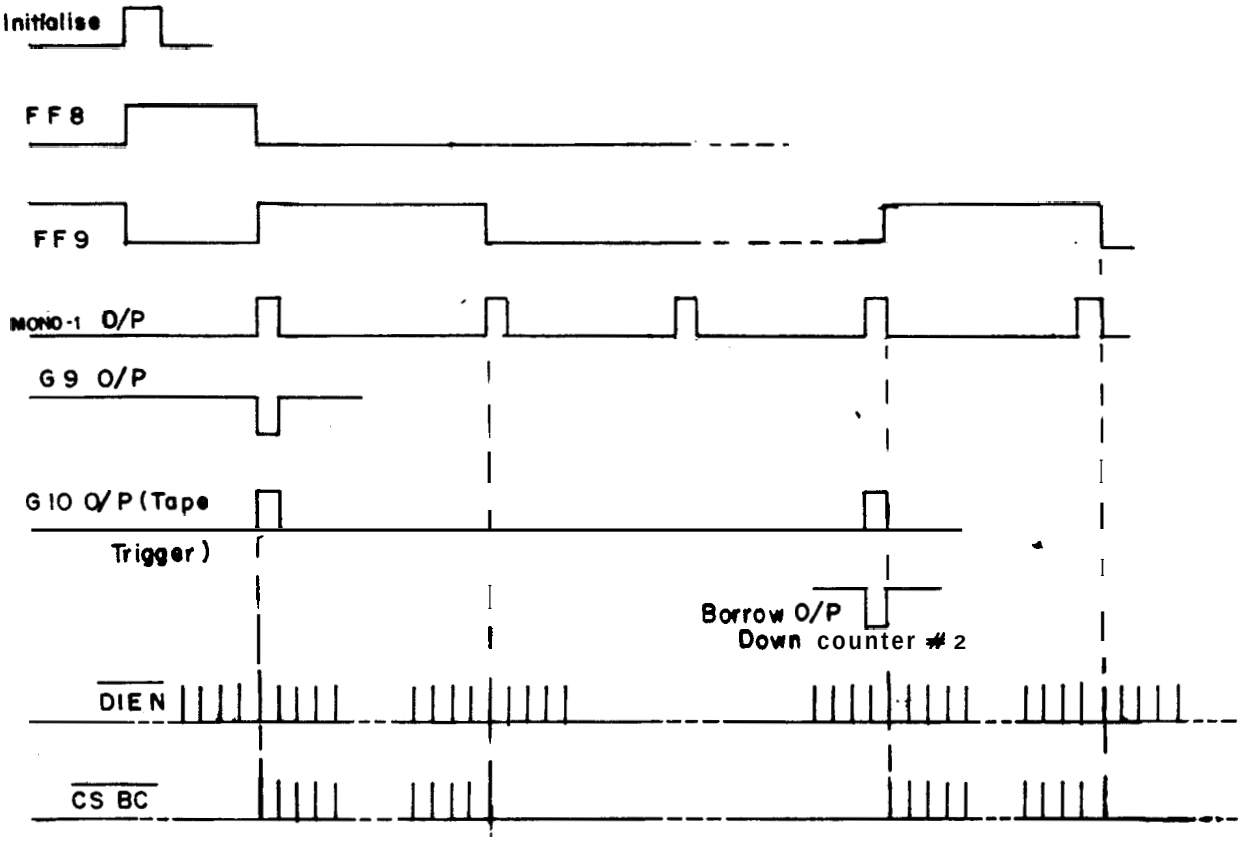


FIG . 4.17. TIMING DIAGRAM FOR CONTROL CIRCUITS SHOWN IN FIG.4.15 & 4.16

FF9 is reset again by the following MONO-1 pulse and remains low till the borrow output from the down counter sets it again. $\overline{\text{DIEN}}$ signals are gated by the Q output of FF9, thereby producing Q bus coupler signal, $\overline{\text{CSBC}}$, when the data corresponding to each beam is valid at the output of Tmap-RAM. This is effected by Gate S1, G11 and G12. The G10 output is effectively the trigger signal to take the data outside the system, and is designated as the TAPE TRIGGER pulse and is issued at the end of each post-integration period. Two operations are performed simultaneously. E'irst the data from Tmap-RAM is read out to the microcomputer by the chip select signal, $\overline{\text{CSBC}}$. Second, this signal inhibits bus coupler, BC-0, and forces a zero input to the ADDER-3, since fresh data has to start accumulating. Subsequent tape trigger pulses are obtained by using the borrow output of the down counter to load the post-integration factor again. Thus the memory add-in feature is obtained in the Tmap-RAM.