CHAPTER 3

FRONT END OF THE DIGITAL RECEIVER SYSTEM

3.1 Introduction

In the design of the digital correlator system to replace/supplement the old analog correlator system, advantage has been taken of the recent developments in the field of digital techniques. Digital correlation withmany channels can be performed by using inexpensive digital integrated circuits. Low cost and high accuracy are the main features in the design of the multichannel receiver system described here.

The 34.5 MHz signal from the antenna is down converted to IF band (Ref. Sec. 2.2.2.1). By employing bandpass sampling, DSB signals are produced. There are several advantages of using such a DSB system as compared to a SSB system. Front end circuitry is simpler in a DSB conversion scheme as compared to SSB conversion, which requires sharp cutoff filters etc. The delay compensation necessary for the path length differences in the interferometer can be changed in coarse steps (presently a time delay step of 1/2 μs is employed) without affecting the phase in the DSB system (See eg. Radhakrishnan etal, 1971). Thus, DSB system allows slightly inaccurate delay settings, while such

settings in a SSB system will cause unacceptably large phase jumps. Also, in a DSB system, the local oscillator frequency is the "operating frequency" of the interferometer whatever is the bandwidth or frequency of the IF sections of the receiver. As the local oscillator frequency is known precisely, the determination of the various base lines of the interferometer in wavelengths can be done trivially and exactly,

The S/N ratio of a DSB system as compared to that of an SSB system depends on a number of factors. In the present case, becauee of the low operating frequency of the telescope, the major contribution to system noise is from the sky background which can exceed receiver noise by a large factor. Hence, it is necessary to "unfold? the two sidebands to get the full benefit of the RF bandwidth at the frontend before mixing. This is achieved, as shown later in this chapter, by employing 4 correlator circuits and 2 adders for each channel, DSB signals can thus directly be correlated without unfolding the sidebands. In practice, the implementation of this technique for analog correlator circuits, is difficult in view of the increased cost and complexity of the correlator circuits. Since four one-bit correlators are incorporated in an inexpensive digital integrated circuit, such a scheme of correlating DSB signals is employed in the present system. As a trade-

off between the cost and the signal-to-noise ratio for different levels of quantisation of the sampled signal, one-bit (2 level) quantisation was chosen.

The one-bit digital correlation technique with infinitely clipped signals has the following advantages:

i) As the digital correlator is relatively inexpensive, the multi-channel system required for directly correlating DSB signals is feasible at a modest cost.

ii) Gain variations in the system have practically no effect, since the signals are infinitely clipped.

iii) Different delays required to steer the beam in declination, can be set digitally for different channels by using shift registers. This avoids cables or other phase shifters, and cumbersome associated switching systems as would be required in analog systems.

iv) In a one-bit system, the signals are converted to digital form right at the front-end, thus avoiding expensive sample/hold and analog-to-digital converters which would otherwise be required for final data acquisition in digital form.

v) Integration times can be easily programmed using variable length counters to accumulate the one-bit correlated signals.

vi) Transformation of correlation coefficients in 2's-complement form required for further digital processing is easily carried out.

The sub-systems discussed in this chapter are:

i) The delay system, where the infinitely clipped signals pass through shift registers for equalising path lengths in the North-South and the East-West channels.

ii) The correlator system, where digital correlation of DSB signals is carried out without unfolding the sidebands.

iii) The integration and multiplexer system, where the correlated one-bit signals are accumulated for a preassigned integration time and are then time-division multiplexed for the processor.

iv) The 2's - complement converter, where the accumulator value is transformed to a correlation value in binary 2's - complement form for further processing; and

v) The Van-Vleck corrector, where the one-bit correlated signals are corrected.

3.2 Delay System

It is necessary that the time delays in the signals from both the North-South array and the East-West array for different positions of the beam in the meridian plane are made equal. In addition, compensation for the unequal cable lengths from each of the North-South elements, as already mentioned in Sec. 2.2.2.2. has also to be provided.

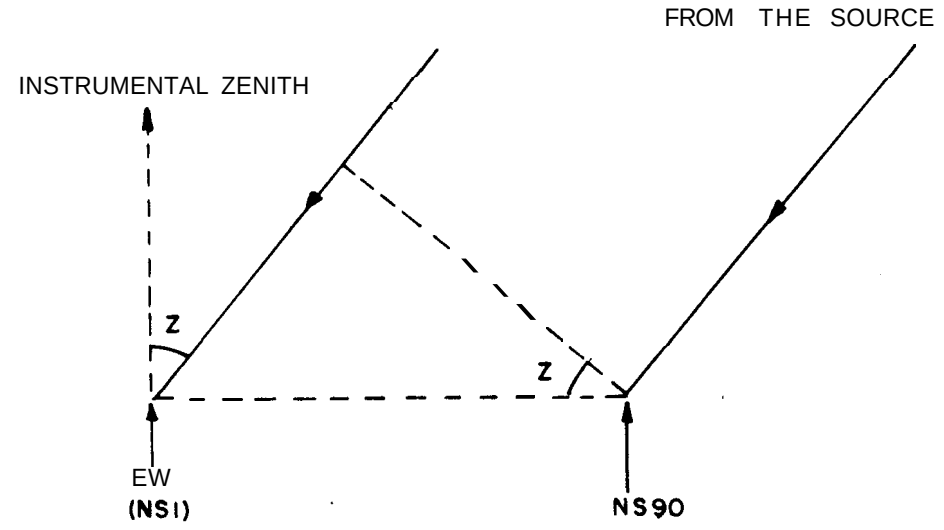
From the Fig 2.2, it is clear that the cable lengtha from any antenna in the East-West array to the final

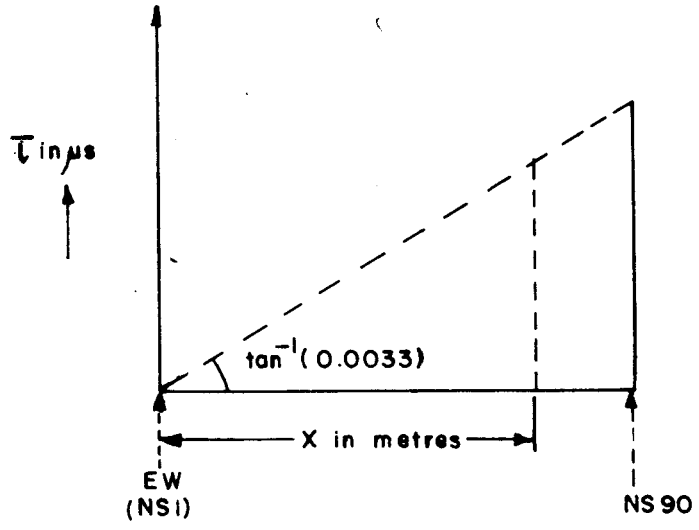
Group amplifier, (located at the centre of the East–West array), is 800 metres. From the centre of the East–West array, the signal is taken to the laboratory through a cable length of 340 metres. In operation, signals from the interferometers formed by the final output of the East–West array and the elements of the North–South array taken 'individually', are obtained and processed. For a source in the meridian plane, at an angle Z from the instrumental zenith, hereafter to be referred to as zenith angle, the signal from the North–South element, located at a distance of x metres from the East–West array (Fig 3.1), is, therefore, to be delayed by

$$\tau_i = \frac{x}{C} \text{ Sin } Z = 0.0033 \text{ x Sin } Z \ \mu s \quad \ldots.(3.1)$$

where C is the velocity of propagation of electro–magnetic waves in free space and Z can be either positive or negative depending on whether the source is to the North or South of the instrumental zenith respectively.

Table 3.1 gives the actual cable lengths for the 90 elements of the North–South array to the laboratory and also the additional lengths required to make this length equal to 340 metres to compensate for the cable length from the centre of the East–West array to the laboratory. However, instead of physically adding the





LEGEND

EW – CENTRE OF THE E-W ARRAY

NS1 – ELEMENT No.1 OF THE N-S ARRAY

NS90 – ELEMENT No.90 OF THE N-S ARRAY

Z – INSTRUMENTAL ZENITH ANGLE

X – DISTANCE, IN METRES, OF N-S ELEMENT FROM THE CENTRE OF THE E-W ARRAY GIVEN BY $X = 5(N_{NS}-1)$ METRES, N_{NS} BEING THE ELEMENT No. OF THE N-S ARRAY.

τ DELAY REQUIRED TO BE COMPENSATED GIVEN BY

$\tau = \frac{X}{c}$ SIN Z in Sec. $= 0.0033 \times \sin Z$ In μs,

c BEING VELOCITY OF LIGHT.

FIG. 3.1 SCHEME FOR DELAY COMPENSATION.

Table 3-1 Cable lengths from each of the N-S element to the Laboratory

Element No. in N-S Array	Actual cable length to control room from final group amplifier in the field In metres.	Length L to be added to make the cable length from the N-S element to the Control room equal to 340m.
1 & 2	334	6
3 & 4	326	14
5 & 6	314	26
7 & 8	306	34
9 & 10	294	46
11 & 12	276	64
13 & 14	266	74
15 & 16	256	84
17 & 18	246	94
19 & 20	236	104
21 & 22	226	114
23 & 24	216	124
25 & 26	206	134
27 & 28	196	144
29 & 30	186	154
31 & 32	200	140
33 & 34	190	150
35 & 36	180	160
37 & 38	172	168
39 & 40	160	180
41 & 42	160	180

Table 3-1 contd.....

43 & 44	172	168
45 & 46	180	160
47 & 48	190	150
49 & 50	200	140
51 & 52	182	158
53 & 54	192	148
55 & 56	202	138
57 & 58	210	130
59 & 60	222	118
61 & 62	220	120
63 & 64	230	110
65 & 66	240	100
67 & 68	250	90
69 & 70	260	80
71 & 72	272	68
73 & 74	280	60
75 & 76	290	50
77 & 78	300	40
79 & 80	310	30
81 & 82	324	16
83 & 84	332	8
85 & 86	344	-4
87 & 88	354	-14
89 & 90	362	-22

required cable lengths, equivalent delays have been incorporated by using shift registers. A separate shift register is used in each NS channel to compensate for the cable lengths of 800 metres of the East-West element to the final East-West group amplifier.

Assuming the velocity of propagation of the electro-magnetic waves through cables to be βc, where $\beta \sim 0.66$, the compensating delay to be produced is given by:

$$\tau_2 = \frac{L}{\beta c} = 0.0051\ L\ \mu s \qquad \ldots\ldots\ (3.2)$$

where L is the length of the cable in metres.

Thus the total delay to be compensated for any zenith angle is given by:

$$\tau = \tau_1 + \tau_2 = (0.0033 \times \mathrm{Sin}\ Z + 0.0051\ L)\ \mu s \qquad \ldots\ldots (3.3)$$

From the equation(3.3) ,the amount of delay to be introduced for the signals arriving from various elements of the North-South array may be calculated for a given zenith angle, Z, and a curve may be plotted. This has been done for various zenith angles from -60° to $+60^\circ$ and a typical curve for Z of 5° is given in Fig 3.2. As mentioned earlier, the delay compensation is effected by means of a 4-bit shift register clocked at 2 MHz rate. The delay can, therefore, be corrected in steps of 0.5 μs only. Bearing this in mind, the

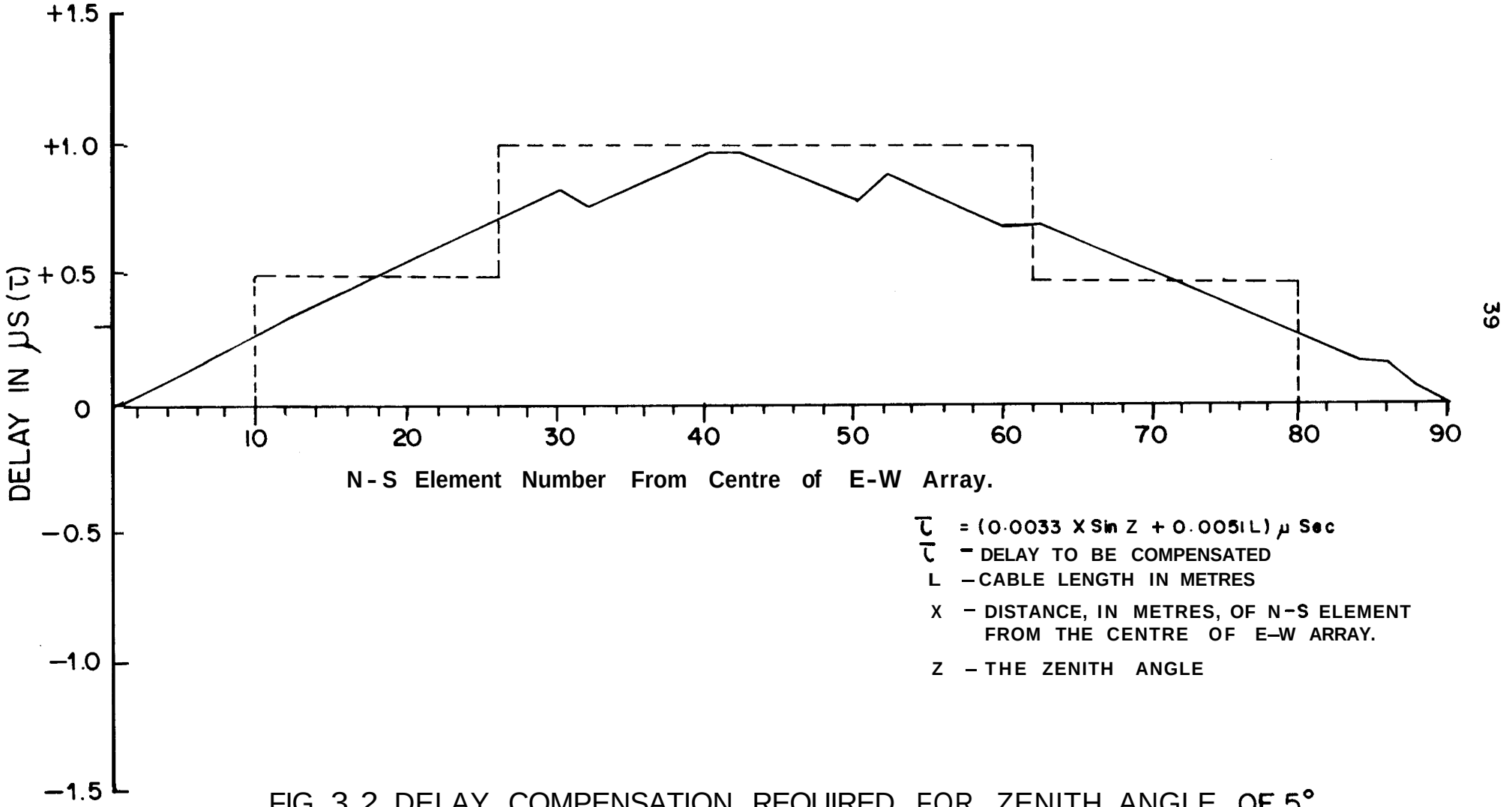


FIG 3.2 DELAY. COMPENSATION REQUIRED FOR ZENITH ANGLE OF 5°.

curve of Fig 3.2 is digitised, so that the error in delay for individual elements does not exceed $\pm$ 0.25 μs. This gives rise to some decorrelation, whose magnitude is given by (Christiansen and Hogbom, 1969).

$$B(\Delta\tau) = \frac{\sin \pi \Delta\tau \Delta\nu}{\pi \Delta\tau \Delta\nu} \quad \ldots\ldots \quad \ldots\ldots \quad \ldots\ldots\ldots\ldots (3.4)$$

where $\Delta\nu$ is the bandwidth of the signal;
and $\Delta\tau$ is the departure from the time delay required.

Table 3.2 gives the delay decorrelation for different $\Delta\tau$'s and $\Delta\nu$'s of the signal.

The variation of the decorrelation factor with zenith angle was investigated for different North-South element grouping schemes. (Grouping of elements implies that the signals from all the elements in a particular group are delayed by the same amount. A grouping scheme may consist of dividing the 90 North-South elements into groups of 2, 4, 6, 8). It was found that a scheme wherein the 90 North-South elements were split into 23 groups - the first 22 being of four elements each, and the twentythird being a group of two only - was fairly optimum. Further, it was found that the zenith angle range of -60° to $+60^{\circ}$, may be conveniently divided into the 8 zones indicated in Table 3.3. This arrangement results in the least decorrelation, the factor not exceeding 6% for a signal bandwidth of 1 MHz and $\Delta\tau$ of 0.2 us maximum as shown in Fig 3.3.

Table 3-2: DELAY DECORRELATION (B) FOR ERRORS IN DELAY COMPENSATION ($\Delta\tau$) AT DIFFERENT BANDWIDTHS ($\Delta\nu$)

$\Delta\nu$ In MHz	$\Delta\tau$ in μs	BW delay product ($\Delta\nu$. $\Delta\tau$)	Delay Decorrelation B($\Delta\tau$)
0.25	0.15	0.375	0.9975
	0.2	0.05	0.995
	0.5	0.125	0.98
0.5	0.15	0.075	0.99
	0.2	0.1	0.98
	0.5	0.25	0.90
1.0	0.15	0.15	0.97
	0.2	0.2	0.94
	0.5	0.5	0.64

From the above it is seen that if delay is kept within 0.15 μs rms, the correlation coefficient worsens to about 0.97 at 1 MHz Bandwidth.

Table 3.3: TIME DELAY (IN MICROSECONDS)

Zenith Angle Zones	NS Group Numbers																							
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23
-60° to -45°	0	0	0	0.0	0.5	0.5	0.5	0.5	0.5	0.5	0.5	0	0	0	0	-0.5	-0.5	-0.5	-0.5	-1.0	-1.0	-1.0	-1.0
-44° to -30°	0	0	0	0	0.5	0.5	0.5	0.5	0.5	0.5	0.5	0.5	0	0	0	0	0	-0.5	-0.5	-0.5	-1.0	-1.0	-1.0
-29° to -14°	0	0	0	0.5	0.5	0.5	0.5	0.5	0.5	0.5	0.5	0.5	0.5	0.5	0.5	0	0	0	0	-0.5	-0.5	-0.5	-0.5
-13° to + 1°	0	0	0	0.5	0.5	0.5	0.5	0.5	0.5	1.0	1.0	0.5	0.5	0.5	0.5	0.5	0.5	0.0	0	0	0	0	-0.5
+ 2° to +15°	0	0	.5	0.5	0.5	0.5	1.0	1.0	1.0	1.0	1.0	1.0	1.0	1.0	1.0	0.5	0.5	0.5	0.5	0.5	0	0	0
+16° to 36°	0	0	.5	0.5	0.5	0.5	1.0	1.0	1.0	1.0	1.0	1.0	1.0	1.0	1.0	1.0	1.0	1.0	1.0	0.5	0.5	0.5	0.5
37° to 55°	0	0	.5	0.5	0.5	1.0	1.0	1.0	1.0	1.5	1.5	1.5	1.5	1.5	1.5	1.5	1.5	1.0	1.0	1.0	1.0	1.0	1.0
56° to 60°	0	0	.5	0.5	0.5	1.0	1.0	1.0	1.5	1.5	1.5	1.5	1.5	1.5	1.5	1.5	1.5	1.5	1.5	1.5	1.5	1.5	1.0

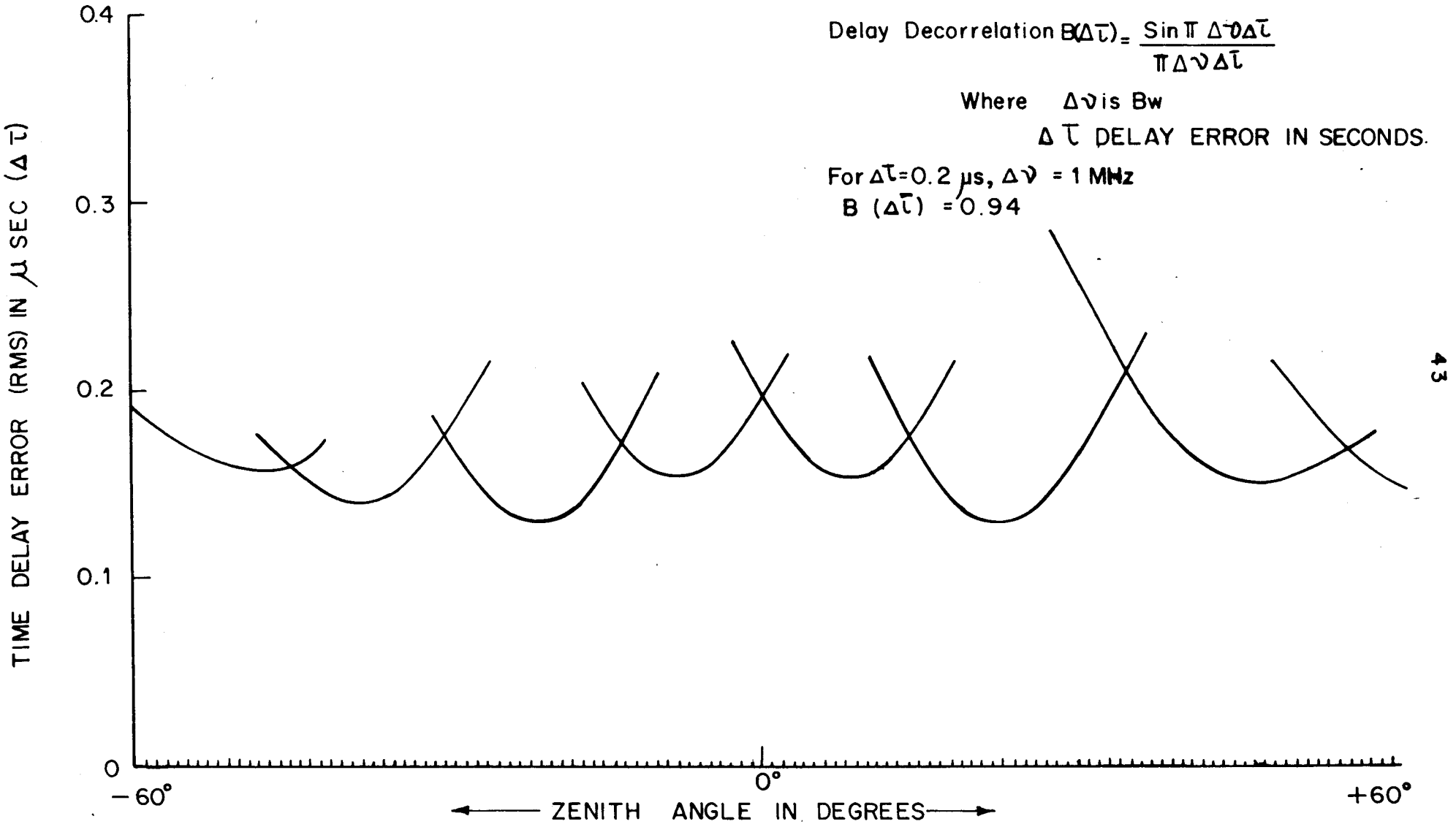


FIG. 3.3 DELAY ERROR FOR DIFFERENT ZENITH ANGLES.

Table 3.3 gives the time delay setting in microseconds of various groups of North–South elements for different zenith angle zones. The negative time delay in the North–South Channel is provided by delaying the signal in the East–West channel, also with a 4–bit shift register. Table 3.4 gives the arrangement of control bits for the shift registers in the North–South and East–West channels. 2 Control bits are required to set the delay in the 4–bit ahift register, thereby requiring 48 bits or 6 bytes of control data for each zenith angle zone to all the shift registers in the 23 groups of North–South elements and one East–West channel. A look–up table 48 bytes long provides the control data for all the 8 zenith angle zones. The selection of a particular zenith angle zone is made by setting a thumb–wheel in the console.

3.3 Digital Correlation Circuit

The signal at 34.5 MHz at the antenna is down converted to IF band and bandpass sampling (Sec. 2.2.2.1) is employed to give the DSB signal.
Correlating the DSB signals so obtained is not quite simple, since the information band is folded after conversion. However, using extra mixers and correlators, one need not unfold the signal before correlating as discussed below:

Let the unshifted signals be S_1 and S_2 of the

Table 3.4: ARRANGEMENT OF CONTROL BITS FOR THE DELAY SHIFT REGISTER

Zenith Angle Zones	E-W Array	Group Numbers in N-S Array																						
		1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23
-60° to 45°	2	2	2	2	2	3	3	3	3	3	3	3	2	2	2	2	1	1	1	1	0	0	0	0
-44° to -30°	2	2	2	2	2	3	3	3	3	3	3	3	3	2	2	2	2	2	1	1	1	0	0	0
-29° to -14°	1	1	1	1	2	2	2	2	2	2	2	2	2	2	2	2	1	1	1	1	0	0	0	0
-13° to $+1^{\circ}$	1	1	1	1	2	2	2	2	2	2	3	3	2	2	2	2	2	2	1	1	1	1	1	0
2° to 15°	0	0	0	1	1	1	1	2	2	2	2	2	2	2	2	2	1	1	1	1	1	0	0	0
16° to 36°	0	0	0	1	1	1	1	2	2	2	2	2	2	2	2	2	2	2	2	2	1	1	1	1
37° to 55°	0	0	0	1	1	1	2	2	2	2	3	3	3	3	3	3	3	3	2	2	2	2	2	2
56° to 60°	0	0	0	1	1	1	2	2	2	3	3	3	3	3	3	3	3	3	3	3	3	3	3	2

2 elements of the interferometer and the 90^{o}-shifted signals be S_1' and S_2'. Let the cosine and sine correlations be a_n and b_n respectively. a_n and b_n are given by:

$$\begin{aligned} a_n &= S_1S_2 + S_1'S_2' \\ b_n &= S_2S_1' - S_1S_2' \end{aligned} \qquad (3.4)$$

Appendix-1 gives the derivation of the above expressions. Thus by employing 4 correlators to obtain S_1S_2 , $S_1'S_2'$, S_2S_1' and S_1S_2' and by adding appropriate terms, the cosine and sine correlation coefficients may be obtained as shown in Fig 3.4. Since the signals are infinitely clipped, inexpensive one-bit correlator circuits are employed to obtain cosine and sine correlations. The one-bit signal after passing through the 4-bit shift-register for delay compensation, is correlated by simple digital circuits (EXOR and EXNOR gates) to obtain the product terms as shown in Fig 3.5. The EXNOR gate measures coincidences between the two strings of pulses and is used in the present system. The cosine correlation value is obtained by adding the outputs of two EXNOR gates to give the functions $S_1S_2 + S_1'S_2'$ and is fed to a counter. The sine correlation is obtained

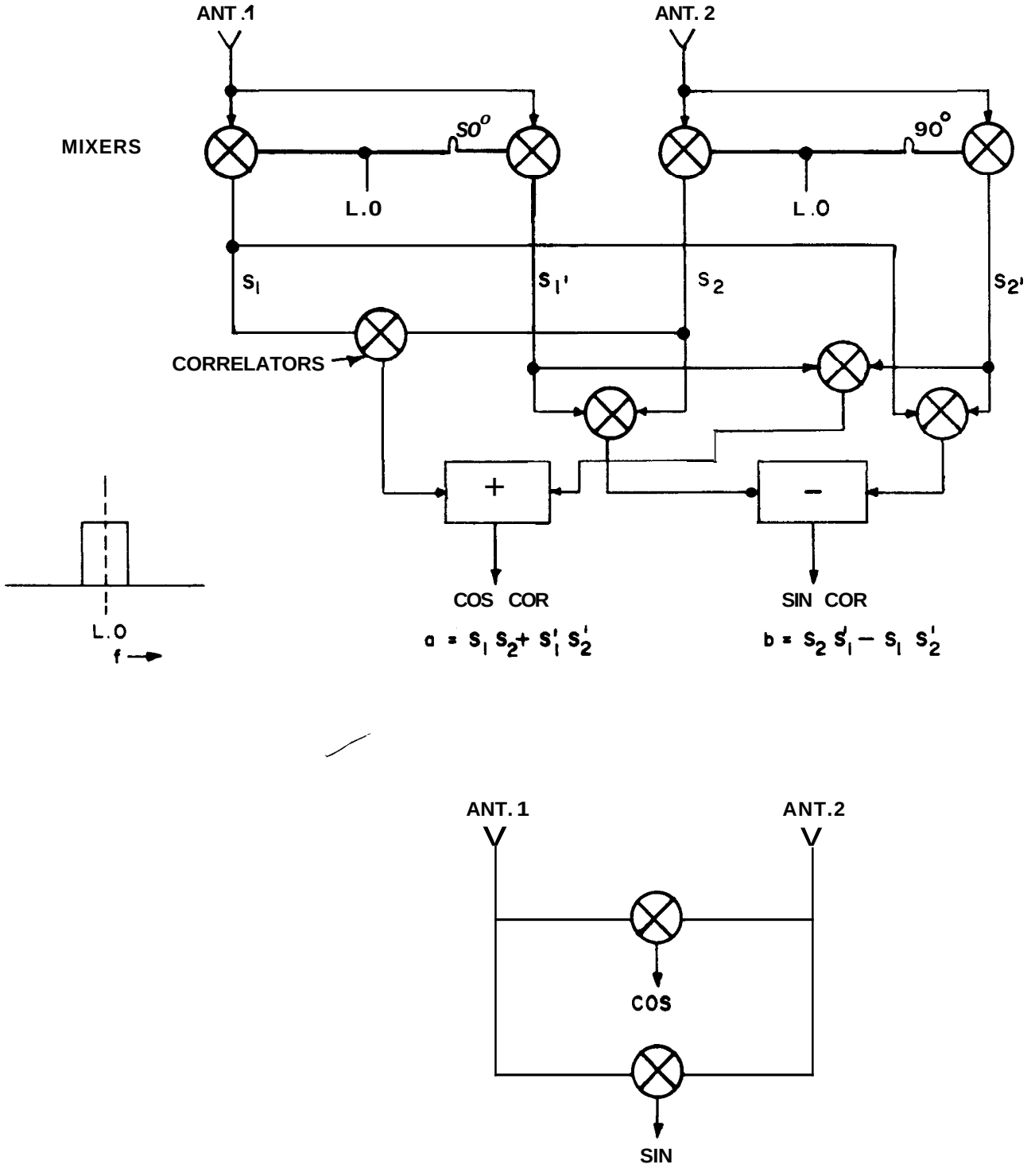


FIG. 3.4.DOUBLE SIDE-BAND CORRELATOR CIRCUIT.

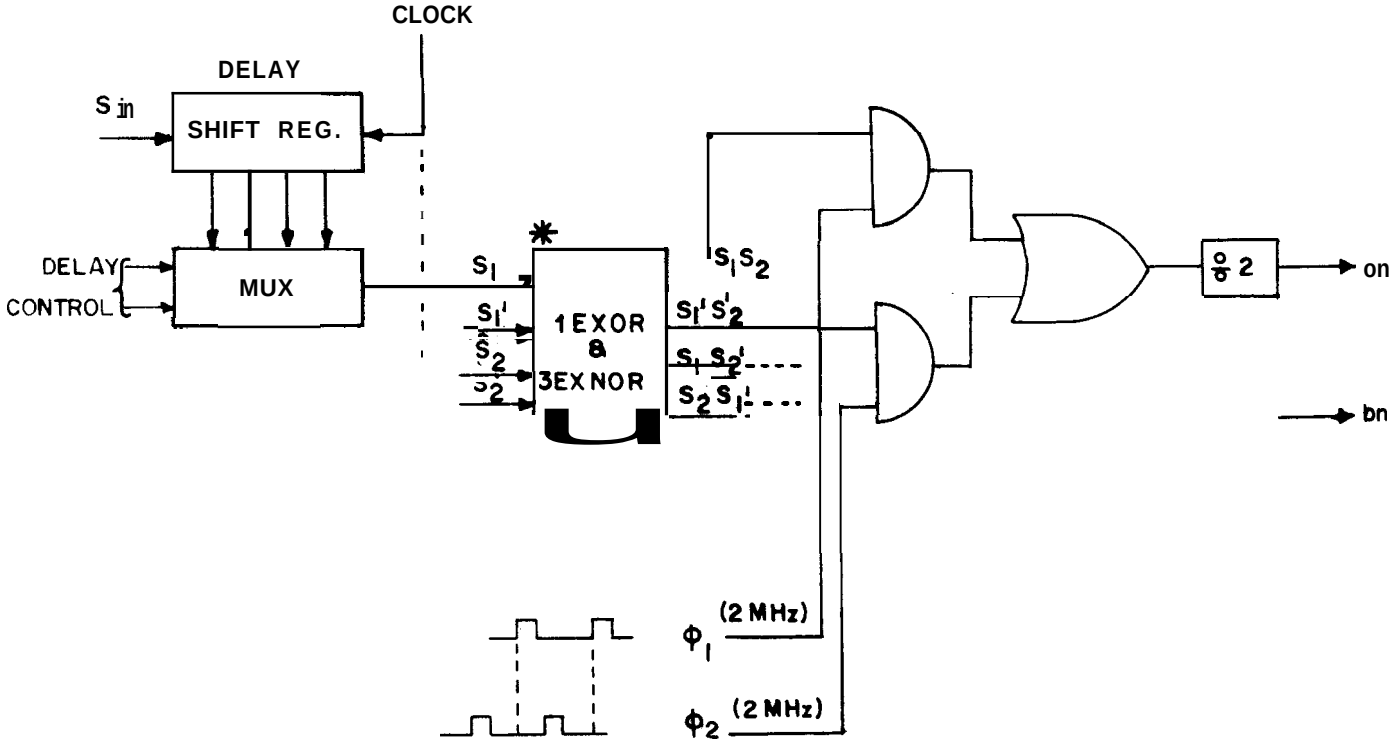
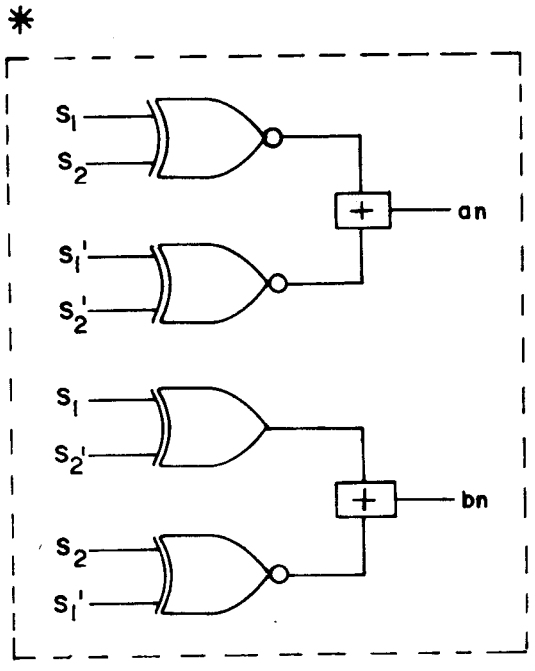


FIG.3.5. DELAY CORRECTION & DIGITAL CORRELATION.



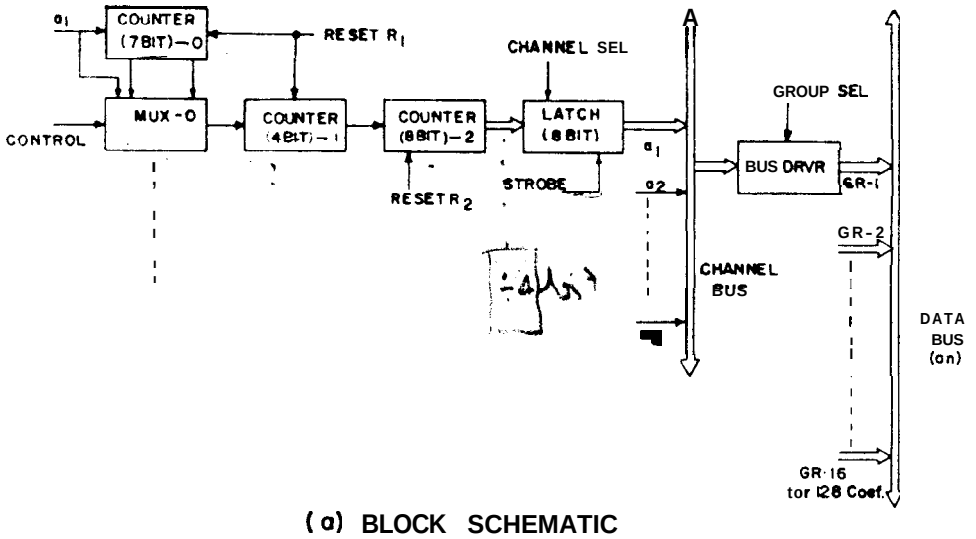
LOGIC CIRCUIT OF THE CORRELATOR.

by adding the output of one EXNOR gate to that of one EXOR gate to give the function $S_2S_1' - S_1S_2'$.

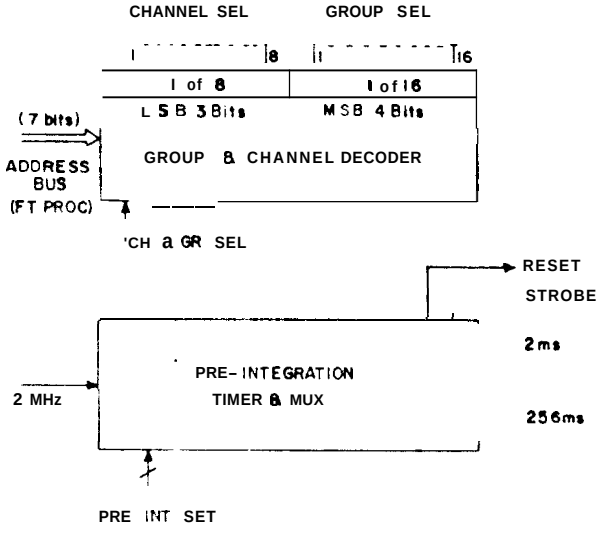
Addition of the terms is carried out by employing AND/OR gates using 2 phase clocks ϕ_1 and ϕ_2 at 2 MHz rate as shown in Fig 3.5. This method avoids the use of expensive conventional adder circuits. The output of the AND-OR gate is at a 4 MHz rate because of two-phase clocking, and hence a divide-by-two circuit is included in the correlator circuit to normalise the signal to a 2 MHz rate.

3.4 Digital Integration and Multiplexing Circuit

The correlator output is fed to a variable length counter to cater for different pre-integration times. The length can be varied from 12 bits of accumulation for the smallest pre-integration period of 2 ms, upto 19 bits for 256 ms pre-integration time. At a maximum signal rate of 2 MHz the counter will not overflow for any pre-integration time selected. In fact, the length of the counter and the pre-integration time can be independently controlled. Fig 3.6(a) gives the schematic for the data integration and multiplexing. The correlated signal in each channel passed through the counter -0 and the parallel output from the 7-stage counter -0, along with the counter input



(a) BLOCK SCHEMATIC



(b) CONTROL CIRCUIT.

FIG. 3.6. DATA INTEGRATION AND MULTIPLEXING CIRCUIT.

signal, ia given to the 8-channel Multiplexer,'MUX-0'. The Control input to the MUX-0 is given according to the pre-integration time selected. The signal then passes through the 4-stage counter -1 followed by the 8-stage counter -2.

A strobe pulse is generated at the end of each pre-integration time which latches the 8-bit output of the counter -2 in the 8-bit latch circuit. There are in all 128 channels each for a_n and b_n, although presently only 90 channels are used. a_n and b_n are multiplexed to the Fourier Transform processor unit in 2 levels of multiplexing. Tri-state latch circuits are used in the first-level multiplexing by grouping 8 channels at the channel-bus. 16 such groups are multiplexed in the second-level multiplexing using tri-state bus drivers at the data-bus separately for a_n and b_n. Since the MSB 8 bit counter value is used for further processing, only counter -2 is reset after latching the counter -2 value at the end of the pre-integration interval. This minimises the truncation error in the correlation values.

Fig 3.6(b) gives the control circuit. The 7-bit address for selecting 128 channels sequentially can be split into 2 groups having MSB 4-bits for group-select

signals and LSB 3-bits for channel-select. The Strobe pulse goes simultaneously to all the latch circuits in each channel. The Channel-select signal comes out independently for all the groups and is driven commonly from the decoded LSB 3-bits. Thus, the signal will be enabled at the channel BUS, from any one of the channels all the time, but the data will not reach the a_n or b_n-BUS, unless that group is selected.

A timer in the Control Circuit generates a STROBE pulse at the end of each pre-integration interval. Pre-integration times can be set as 2^n milli-sec, where n may be chosen to be 1, 2, 3.....8 as already mentioned. A counter driven from a 2 MHz internal clock, along with an 8-channel multiplexer, gives the selectable pre-integration times. The counter can also be driven from an external clock. The timer issues a RESET pulse at the end of each STROBE pulse to reset the data counters as already indicated.,

3.5 The 2's Complement Converter Circuit

The transformation from ,counter value to correlation value (ρ_c) is given by the relation:

$$\rho_c = \frac{K_c - K_a}{K} \qquad .....(3.5)$$

where: K_c is the number of coincidences,
K_a is the number of anticoincidences, and
K is the number of samples.

The transformation thus requires numerical processing which involves time. In an on-line processing system, this is a serious factor which can limit the speed of operation. It is shown in Appendix 2 that the correlation values in 2's complement form can be very easily obtained from the measured counter values by simple logic, by complementing only the most significant bit. Since most of the digital processing circuits use 2's complement notation, getting the correlation values directly in this notation is an extra bonus. A fast multiplier chip, like the TRW 8AJ, is used in the processor which requires the data to be given in 2's complement form.

3.6 Van-Vleck Corrector Circuit

The degradation of the correlation value of one-bit signal is about 66% compared to that for an unclipped signal (Weinreb, 1963). The true correlation value may be obtained by using the formula:

$$\rho_T = \mathrm{Sin}\left(\frac{\Pi\rho_m}{2}\right) \qquad .....(3.6)$$

where ρ_m and ρ_T are the measured and true correlation values respectively.

For small values of ρ_m, $\rho \simeq \Pi\rho_m$ and the error is less than 1% for correlation values of upto 16. For weak sources the correlation values may be much smaller than 16% and hence the correction may

be neglected. However, for strong sources such as may be observed for system calibration, the application of the correction will be necessary.

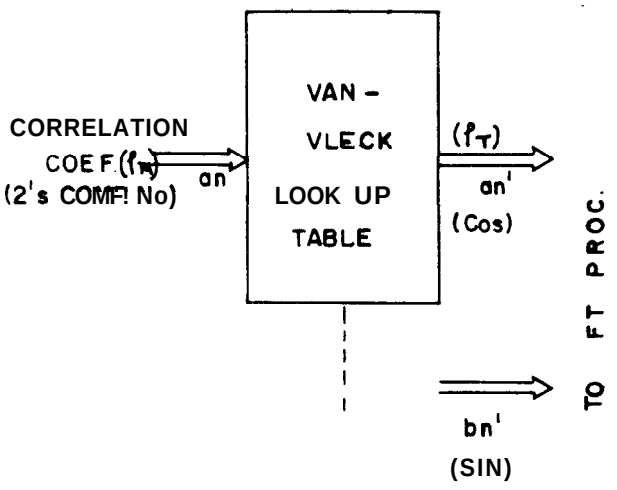
A look-up table is provided for implementing the Van-Vleck Correction (Fig 3.7). This uses a 256 byte ROM programmed to give directly the 2's complement true correlation coefficient. It has an access-time of less than 500 ns. The propagation delay of the two-level multiplexer for a_n and b_n together with the access tire of the above mentioned ROM should be less than the basic cycle time.(1.75 μs) of the Fourier Transform Processor. The system speed is thus not slowed down.

CORRECTION Of THE MEASURED CORRELATION VALUE OF INFINITELY CLIPPED SIGNAL (1BIT SIGNAL) WASGIVEN BY VAN–VLECK AS FOLLOWS:

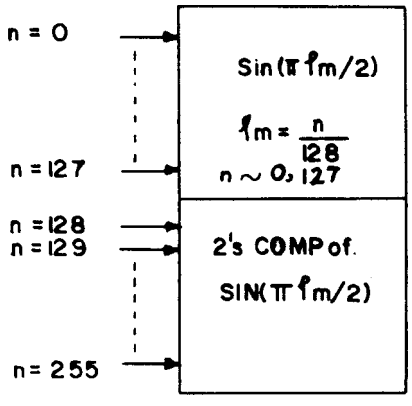
$f_T = \sin(\pi f_m/2)$

Whre f_m is measured Correlation value of clipped signal.

f_T is corrected cor. coef.



(a) SCHEME FOR VAN-VLECK CORRECTION.



(b) COMPLEMENT SINE TABLE

FIG. 3.7. IMPLEMENTATION OF VAN–VLECK CORRECTION.