RRI Internal Technical Report – Library_ref_no. TR: AA-2007-1

Synchronizing Receiver Node Hardware Operations and Node M&C and hardware Interaction: Version 1.0

Authors: D. Anish Roshi[1]
Affiliation: [1] **Raman Research Institute, Bangalore, India**

Date: June 5, 2007, (v1.01)
Class: MWA: Receiver Node

Abstract

This report describes the synchronization of state machines in the receiver node. The basic functions of the Node M&C, its interaction with the Receiver Node hardware and the needed synchronization signals for the M&C are discussed. Method to generate the Walsh bit at the Nodes with the proper delay is also described.

1 Introduction

We consider that the MWA will be synchronized using a centrally generated clock and synchronization signal. Fig. 1 shows the schematic of the clock and synchronization signal distribution for the array. In this report, we consider the generation of synchronization signals at the receiver node based on this scheme. The sampling clock is assumed to be 660 MHz (CLK), which is generated at the Nodes from the reference clock (REF_CLK). The synchronization scheme does not depend on the actual value of the clock. The basic integration cycle needed for calibration is ~ 8 sec (Briggs 2007a). So we consider that the period of the primary synchronization signal to be 5×2^{30} CLK cycles, which is about 8.13 sec. Following Briggs (2007a) we refer to this signal as SCTN (Start Counting Ticks Now).

2 SCTN and Walsh signals at the Receiver node

Fig. 2 shows the SCTN and Walsh signal propagation delays due to their distribution. One of the requirements of the clock and synchronization (CLK/SYNCH) circuit at the Node is to compensate the differential delay of SCTN due to τ_i. This compensation will align the synchronization signal at the Nodes. Since the differential delay can change with time, the delays should be programmable from the LM&C (local Monitor and control). The accuracy of this delay compensation will be $+/-$ half the reference clock (REF_CLK) period distributed from the central station.

The Walsh signals are generated at the Receiver Node and are distributed to the 8 Tiles that are connected to the Node. The propagation delay due to this distribution ($\tau_\beta ij$; i is the Node number and j is the Tile number) as well as the cable delay suffered by the signal need to be compensated to demodulate the Walsh in the ADFB (Analog-to-Digital converter Filter Bank) board. This delay compensation can be in the Walsh generation board (see Section 4). The accuracy to which this delay needs to be adjusted is set as ~ 50 nsec.

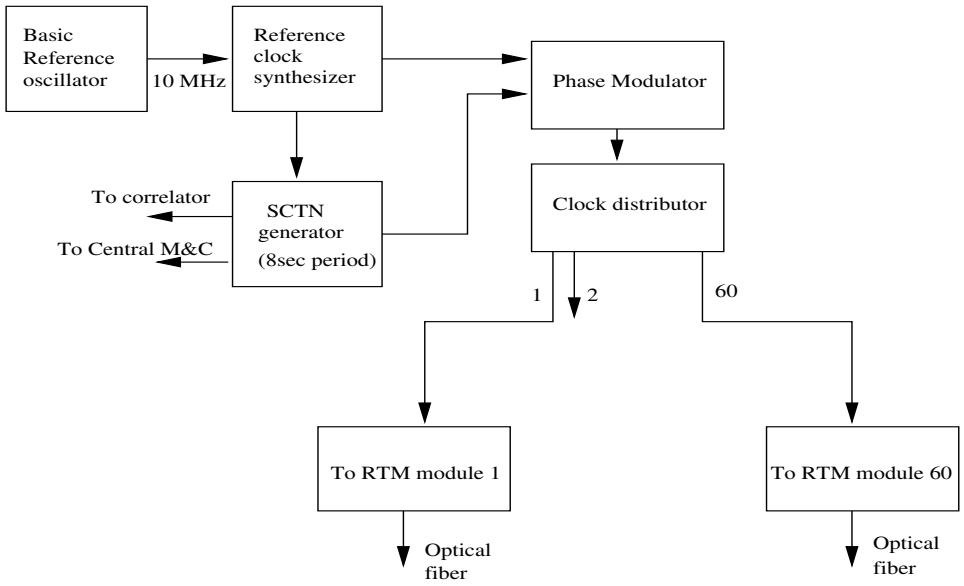

Figure 1: Clock and Synchronization signal distribution

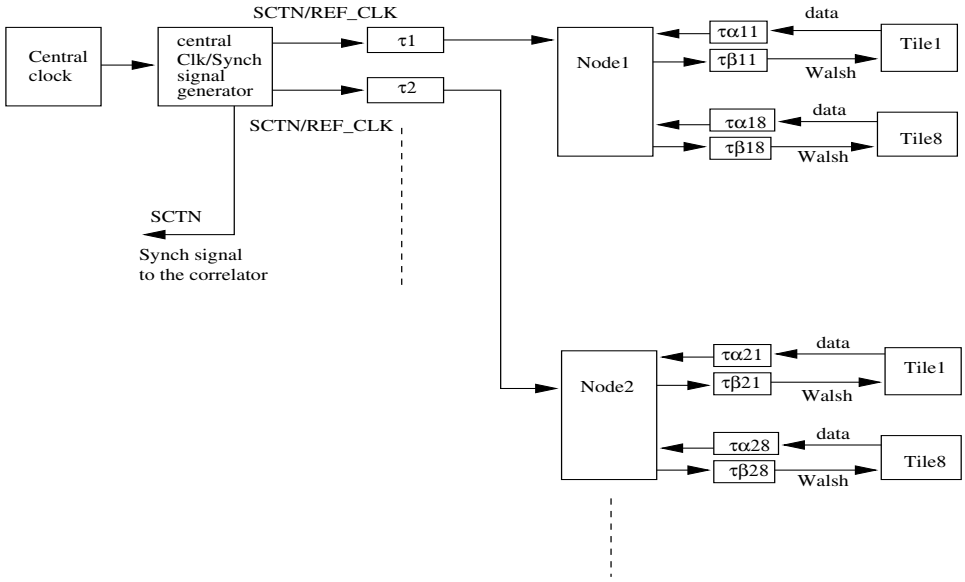

Figure 2: Delay suffered by SCTN, Walsh and signal from the Tile

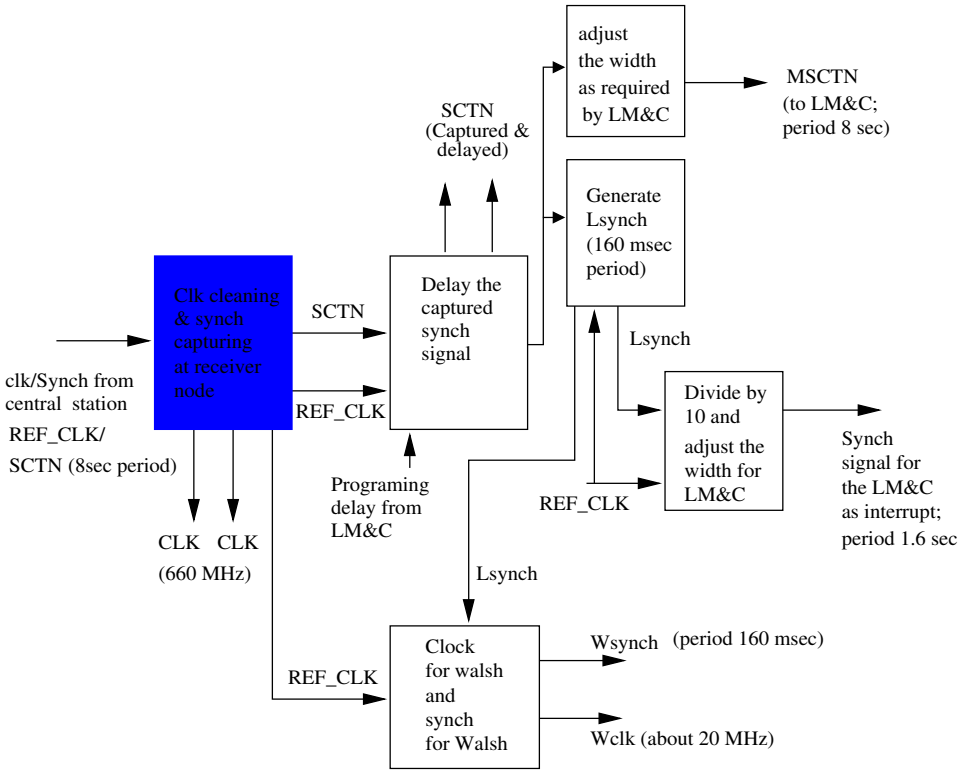

Figure 3: Clock recovery and SCTN capturing blocks at the Receiver Node

3 Local Synchronization signals needed at the Receiver Node and their requirements

The Walsh period is considered to be $\sim$ 10 msec (Briggs 2007b). 16 Walsh states are required for the two polarizations of the 8 Tiles connected to a Node. Thus the Walsh cycle period is $\sim$ 160 msec. The hardware operations in a FPGA in the ADFB will be synchronized with a signal with the Walsh cycle period. We refer to this synchronization signal in the ADFB as Lsynch (Local synchronization signal) The Lsynch generated at different FPGAs in ADFB boards has to be synchronized, which is done using the delay compensated SNTC signal (see Fig. 3).

The current thinking is that the Data Aggregation and Formatting (AgFo) board will also use SCTN signal. The synchronization signal needed for the Walsh generation, Wsynch, will have a periodicity of Walsh cycle (see Section 4). The LM&C will be provided with two synchronization signals – MSCTN and Msynch (see Section 6). MSCTN has the same periodicity of SCTN but the pulse width is adjusted as required by the single board computer. Msynch is generated at $\sim$ 1.6 sec, which the LM&C will use to read the hardware status registers (see Section 6).

4 Walsh signal generation at the Receiver Node

The Walsh states are generated with a clock (Wclk) which is derived from the reference clock. As mentioned above, the Walsh signal send from the Receiver Node suffers a delay $\tau_\beta ij$, before it reaches the multiplier in the Tile electronics. The signal from the telescope after the phase flip introduced by the Walsh modulation suffers a delay of $\tau_\alpha ij$ before it reaches the ADC. The Walsh demodulation is done at the output of the ADC and this hardware process needs to know the total

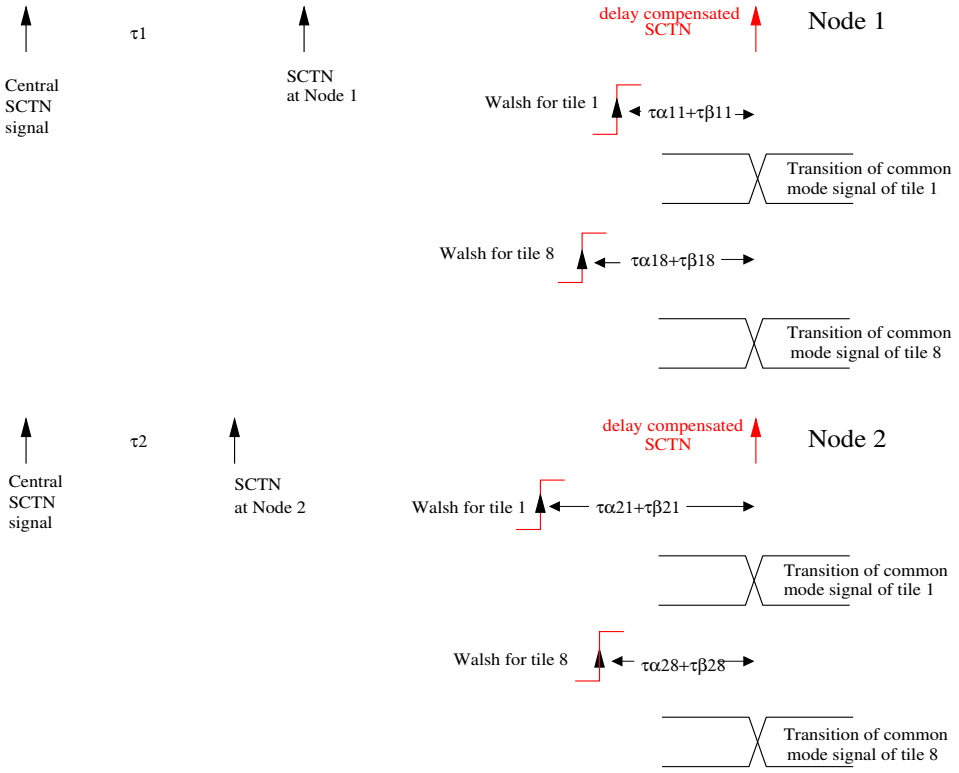

Figure 4: Timing diagram showing the generation of synchronization and Walsh pattern at the Receiver Node

delay. To align the demodulation process with the phase transition in the telescope signal, the Walsh states are advanced by $\tau_\alpha ij + \tau_\beta ij$ (see Fig. 4). We consider that the accuracy of the delay compensation of Walsh states be about 50 nsec. This delay compensation is achieved with Wclk and hence its frequency should be about 20 MHz. A block diagram for generating Walsh signal is shown in Fig. 5. The Walsh sequence is re-synchronized at the end of Walsh cycle using Wsynch.

5 Do we need delay compensation at the receiver node ?

$\tau_\alpha ij$ is not the same for the 8 Tiles in a Node. If MWA uses cables of standard lengths 150, 100 and 50 meters, then the maximum delay between the Tiles in a Node is $\sim$ 0.5 microsec, which is ten times smaller than the maximum expected geometric delay. Therefore it is not necessary to compensate for the delay between the Tiles in a Node.

6 Synchronizing M&C and the Receiver Node

The LM&C will be provided with two synchronisation signals (MSCTN and Msynch; see Fig. 3). MSCTN has a periodicity of 8 sec. LM&C can use MSTNC to determine the boundary of the basic integration cycle. Msynch signal, which has a period of about 1.6 sec, can be used to read the status registers in the hardware. Fig. 6 and 7 give, respectively, the state and timing diagram for the Node M&C operation.

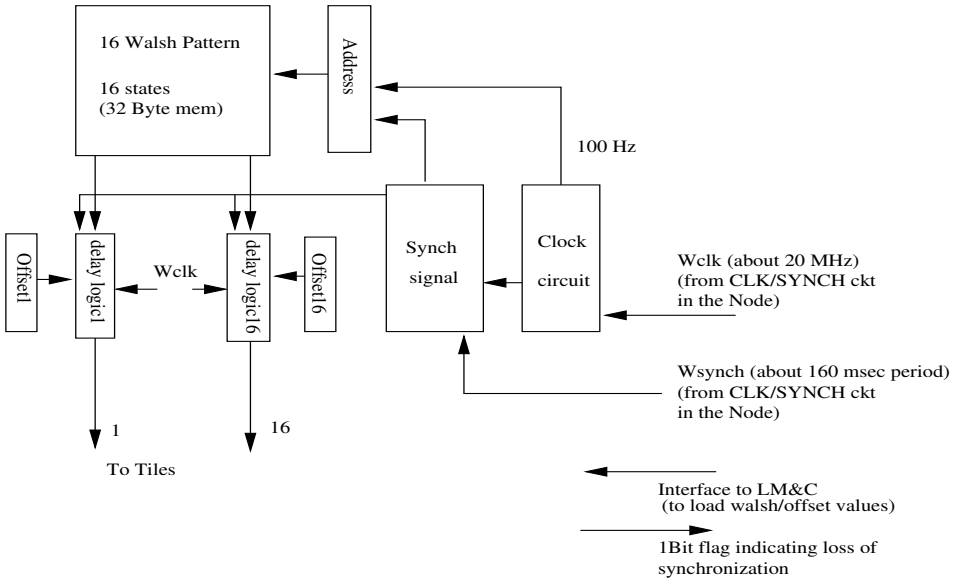

Figure 5: Block diagram of Walsh pattern generation at Receiver Node

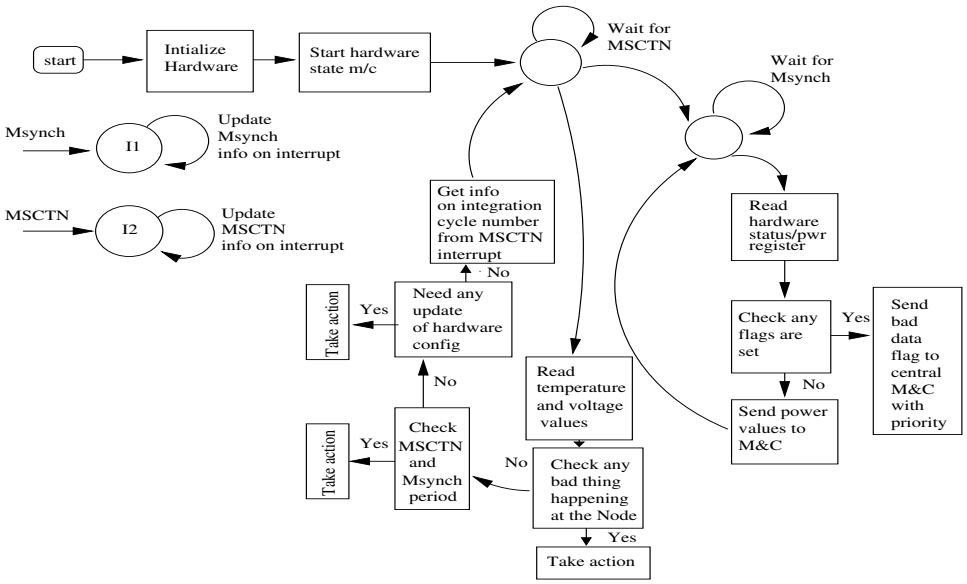

Figure 6: State diagram for the Receiver Node M&C

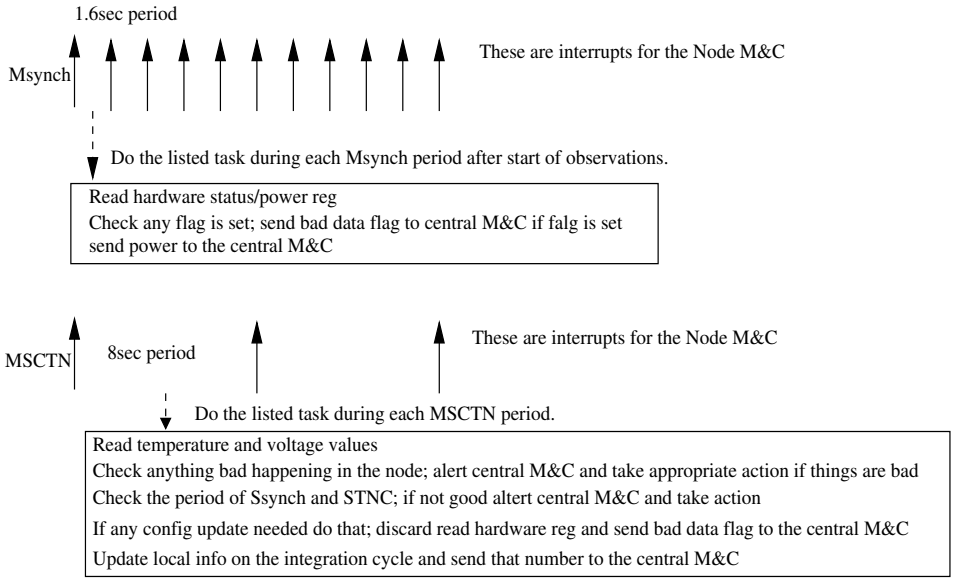

Figure 7: Timing diagram of the M&C operations

Acknowledgment

I acknowledge the many useful discussions I had with Annino, Frank, Mark and Prabu which helped to bring the work reported here to the present state.

Reference

Briggs, F., 2007a, January 7, MWA Knowledge Tree
Briggs, F., 2007b, February 25, MWA Knowledge Tree

Revision History

V1.0 – June 5, 2007

V1.01 – July 25, 2007
SCTN is needed at ADFB for synchronization. So it has been decided to provide only SCTN from the node clock and synch circuit. The 160 msec period Lsynch will be generated inside the ADFB FPGAs.