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BANGALORE-67

A PROJECT REPORT
ON

DESIGN AND DEVELOPMENT OF A BROADBAND LOW NOISE AMPLIFIER

Carried out at

RAMAN RESEARCH INSTITUTE

Submitted by

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In partial fulfillment of the requirement for the award of the degree of

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Visveshwaraiah Technological University

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Certificate

This is to certify that the project titled

"Design And Development Of A Broadband Low Noise Amplifier"

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ABSTRACT

Radio astronomy is a field of science in which the celestial bodies are studied using Radio Techniques with the help of Radio Telescopes .The Radio Telescopes collects the electromagnetic radiations incident on an area of ground and amplify them to detectable levels. Typically a Radio Telescope consists of an antenna, Low Noise Amplifier, Hetrodyning system to convert the frequency band of interest to a particular frequency range, and detectors.

The most important of all the above Receiver components next to the antenna is the Low Noise Amplifier. In general the power levels of the astronomical signals are extremely weak and are of the order 10^{-26} Watts/m^2 Hz or less. So practically all the astronomical signals are hidden in the man made as well as the terrestrial noise. When the radiation is collected, they will be amplified in order to increase their signal level. While doing so, it must be ensured that as minimum noise as possible is added on to the sky signal to minimize the degradation in the S/N ratio. This is possible only when the amplifier following the antenna contributes very low noise of its own .In general the quality of a given Radio Receiver depends upon the noise contribution of the first stage of the amplifier.

The main aim of this project work is to build a Low Noise Amplifier operating over a large bandwidth. The design of it will be based upon the Scattering Parameters of the transistors . RF CAD package will be made use of in simulating and optimizing the performance of the amplifier.

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1. INTRODUCTION

1.1 Definition of noise

Noise is a random signal consisting of all the frequency components, which are random both in amplitude and phase. The exact amplitude at any instant of time cannot be predicted. Generally the noise is characterized by its statistics.

1.2 Types of noise

Generally we come across four different types of noise : (i) Johnson noise (ii) Shot noise (iii) 1/f noise (iv) Partition noise. Each of it is discussed in brief below.

Johnson noise

Randomly varying voltage across the ends of a conductor due to the random collision of charge carriers within the conductor is termed as Johnson noise. This noise is also referred to as thermal or white noise.

Consider a resistor of resistance R at a physical temperature T °K (Refer Fig 1.1). Let E_n represent the rms thermal Noise voltage appearing across it at any instant of time. It is related to the noise bandwidth, its physical temperature and its resistance in a way given by Eq.1.1.

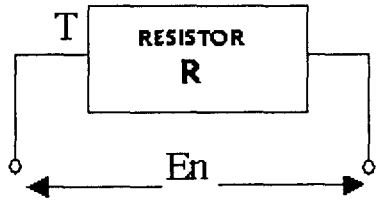


Fig 1.1 Resistor R at a physical temperature T ° K

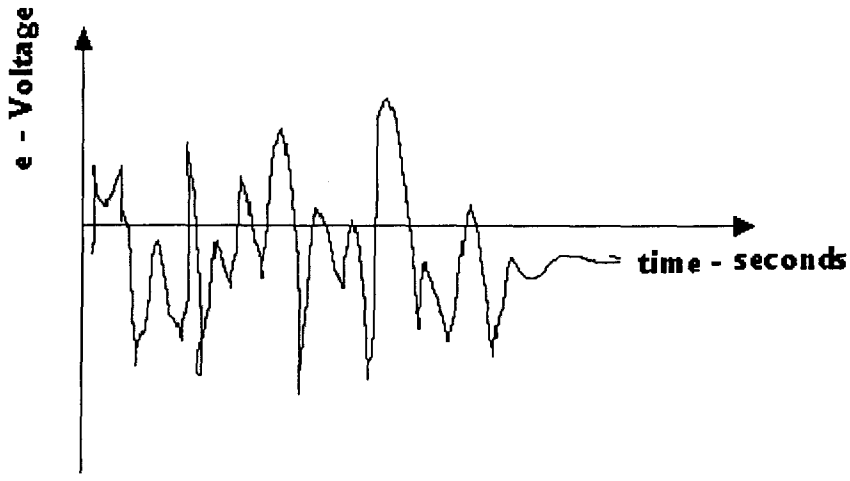


Fig 1.2 Characteristics of Thermal noise voltage.

$$En = \sqrt{4RKTB_n} \qquad 1.1$$

Where R is Resistance of the conductor, ohms
T is Conductor temperature, Kelvin
B_n is Noise bandwidth, Hz
K is Boltzmann's constant = 1.38×10^{-23} J / °K

Shot Noise

Shot noise is a random fluctuation that accompanies any direct current crossing a potential barrier due to non-simultaneous crossing of carriers across the junction (Refer Figs1.3 and1.4). Although it is always present, it is not observed during the measurement because it is small compared to the DC value. However, it does contribute significantly to the noise in the amplifier circuit.

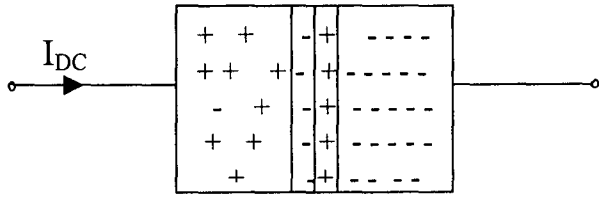


Fig 1.3 A P-N junction diode

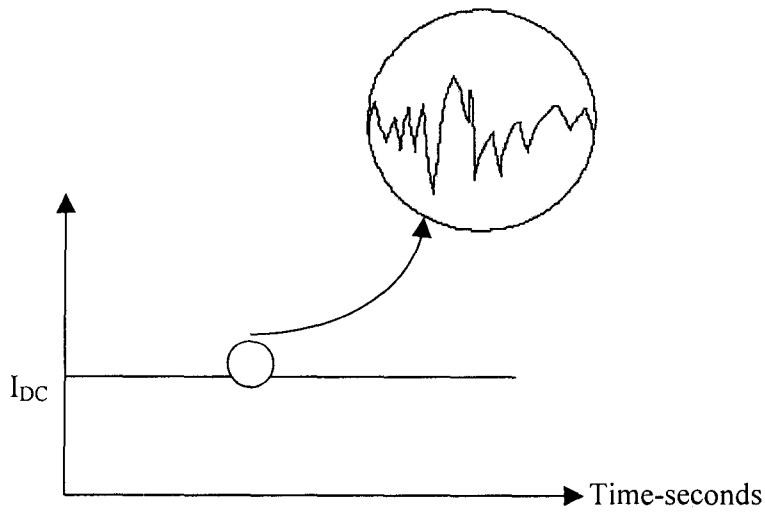


Fig 1.4 Superposition of shot noise current over DC

The rms shot noise current is related to the Noise bandwidth and the direct current in a way given by Eq.1.2

$$I_n = \sqrt{2\, I_{dc}\, qe\, B_n} \qquad 1.2$$

Where I_{dc} is the direct current in amperes and

q_e is the magnitude of electron charge $= 1.6 \times 10^{-19}$C

1/f noise

1/f noise arises from the fluctuation in the carrier densities in a semiconducting material. This gives rise to fluctuations in the conductivity of the material. The spectral density of this noise increases as frequency decreases.

Partition Noise

Partition noise occurs whenever current has to divide between two or more electrodes .It is due to the random fluctuations in the division. It has got flat Noise spectrum.

1.3 Relevance of noise in Radio Astronomy

In general the signal from any astronomical sources will be as weak as 10^{-26} to 10^{-30}W/m^2-Hz .The background noise will be much larger than the desired signal and hence the signal will be completely hidden in Noise. The various sources contributing to the background noise are (i) Noise contribution from the sky, (ii) Noise contribution from the ground, (iii) Noise contribution from the receiver system. So, successful detection of the astronomical source depends upon a good S/N ratio at the receiver output. Every attempt has to be made to minimize the degradation of the S/N ratio due to the receiver itself as the signal gets processed in it.

1.4 Basic definitions

Signal-to-Noise-Ratio:

It is the ratio of magnitude of the desired signal to the ratio of magnitude of noise signal in a given input signal. It is defined in terms of voltages and power as follows

$$S/N = P_s/P_n = V_s^2/V_n^2 \qquad 1.3$$

Where P_s = Signal power

P_n = Noise Power

V_s = Signal voltage

V_n = Noise voltage.

Noise figure:

The Noise figure F of any device is defined as the ratio of the signal-to-noise power ratio at the input to the signal-to-noise power ratio at the output.

$$F = \frac{P_{Si} / P_{Ni}}{P_{So} / P_{No}} \qquad 1.4$$

Noise temperature:

In radio astronomy, the receiver noise is always expressed in terms of noise temperature. Noise temperature of any device represents the total Noise power available over a bandwidth B when it is at a physical temperature of T deg. K.

The relationship between the receiver noise temperature and the noise figure is given by

$$T_R = (F - 1)\, T_o \qquad 1.5$$

Where T_R = noise temperature in deg Kelvin

F = noise factor

T_o = ambient temperature.

Voltage reflection co-efficient:

Voltage reflection Co-efficient is defined as the ratio of reflected voltage to the incident voltage in a two port network.

$$\Gamma = V_r / V_i \qquad 1.6$$

Return loss:

When the load is mismatched, then, not all the available power from the generator is delivered to the load. This is called Return Loss. It is defined in dB in Eq 1.7

$$RL = 20 \log(|\, V_r / V_f \,|) = 20 \log (|\, \Gamma \,|)\ \text{dB} \qquad 1.7$$

where Γ is the reflection coefficient.

1.5 General receiver configuration in a Radio Telescope

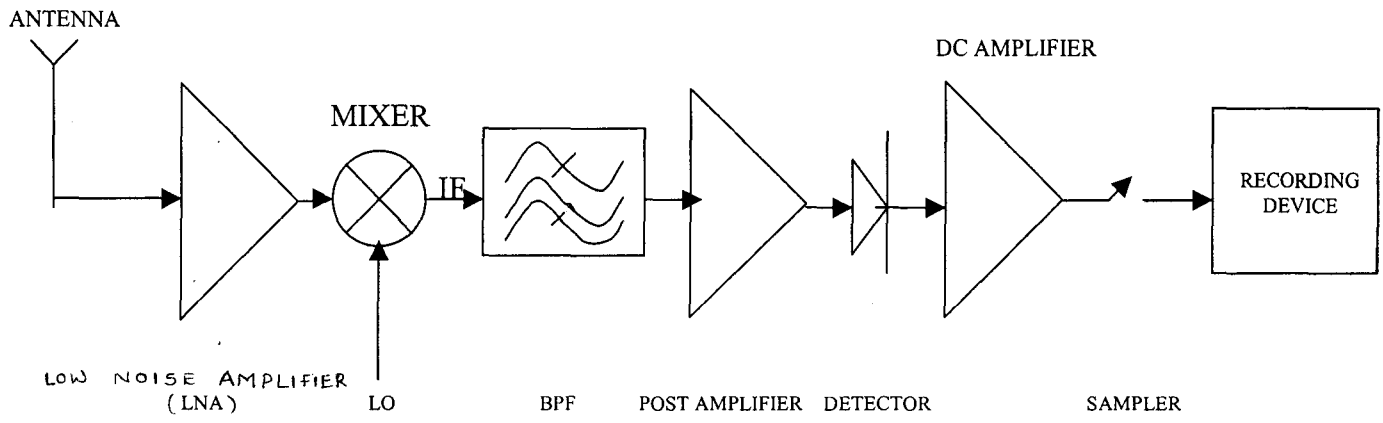


Fig.1.5 General Receiver configuration in a Radio Telescope

The above Fig shows a typical receiver setup of a Radio Telescope. The received signal from the antenna is amplified using the Low Noise Amplifier and down converted using a mixer. The IF signal obtained is band limited to reject any unwanted signal and is further amplified using a post amplifier. The output from the post amplifier is fed to the detector circuit in which a DC output proportional to the RF input power is obtained. The detected signal is further amplified using DC amplifier and sampled .It is then stored in a recording device.

1.5.1 Importance of Low Noise Amplifier in the Radio Receiver

As we see from Fig.1.5 the receiver consists of a number of RF devices and each one of them contributes its own Noise. The major Noise contribution comes from the very first stage .The noise contribution of the subsequent stages will be very small only when the gain of the first stage amplifier is large. This follows from friis formula for overall Noise factor of amplifiers in cascade.

$$F = F_1 + \frac{F_2 - 1}{G_1} + \frac{F_3 - 1}{G_1 G_2} + \ldots\ldots\ldots + \frac{F_i - 1}{G_1 G_2 .. G_{i-1}} \qquad 1.8$$

Where F is overall Noise factor

F_i & G_i are the Noise factor and the gain of the i^{th} stage amplifier.

Since the first stage in the receiver is an amplifier the Noise contribution of it must be made as low as possible. In general the quality of any Radio receiver is decided by the noise performance of the first stage amplifier.

2. DEVICE THEORY

2.1 Devices available for low Noise applications

There are many devices available for building an amplifier. Not all of them are suitable for low noise application. The various devices available are

i. HEMT
ii. GaAs MESFET
iii. GaAs-AlGaAs HBT
iv. Si MOSFET
v. Si bipolar transistor

Comparison of the electrical properties of the above devices is shown in the Table 2.1

Table 2.1 Comparison of the electrical properties of devices available for low noise amplifier

Device	Frequency (GHz)	Noise	Power	Speed
HEMT	Up to 70	Very good	Very good	Excellent
GaAs MESFET	40	Good	Good	Good
GaAs-AlGaAs HBT	20	Good	Good	Excellent
Si MOSFET	10	Poor	Very good	Very poor
Si bipolar transistor	1	Poor	Poor	Good

2.2 Description of various devices

The following sections describe various aspects of a few devices mentioned in the table 2.1

2.2.1 Structure of GaAs MESFET

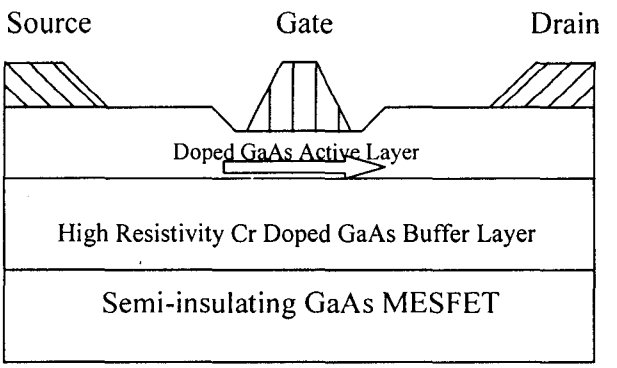


Fig 2.1 Structure of GaAs MESFET

By chemical vapor deposition technique, a buffer layer is grown first on a semi-insulating GaAs substrate. This layer has very high resistivity, hence, is an extension to the substrate in effect. Above the buffer layer, n-type active layer is grown epitaxially. A trench is etched in to this layer and the Schottky barrier gate is formed. Depositing highly doped n type GaAs on to the epitaxial layer to form the ohmic contacts forms source and drain.

2.2.2 Principle of operation of GaAs MESFET

With the source at ground potential and the drain at $+V_{ds}$, electron flow is from source to drain. A negative voltage $-V_{gs}$ reverse biases the rectifying metal semi- conductor gate junction, producing a depletion layer that controls the depth of the conducting channel. This modulation of the channel current consumes little power, since current into the reverse biased gate junction is small.

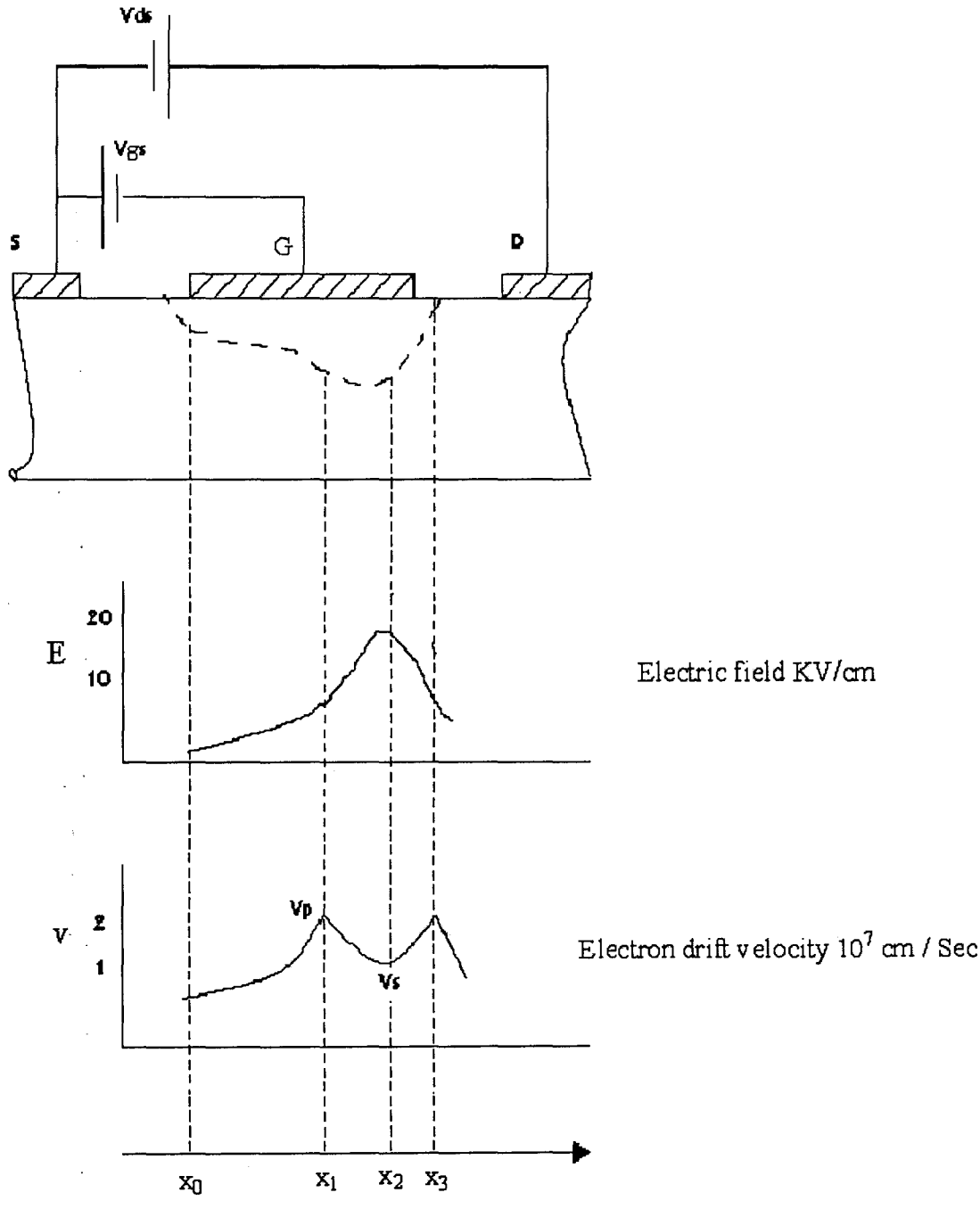


Fig 2.2 Physical conditions in a short gate FETs

Fig.2.2 shows a voltage V_{ds} applied across the source and drain and another voltage Vgs applied across the source and gate of the MESFET. Within the channel under the gate, a region near the drain (x_1) is at a higher potential than x_0. So the reverse bias and the depletion –layer width are greater at x1 than at x_0 .Since the channel is narrowing, the electric field E and electron drift velocity 'v' must increase from x_0 to x_1 to maintain current. As Vds is increased, the channel reverse bias increases and the depletion depth at x_1 extends nearly to the bottom of the channel .At this point, the channel is said to be pinched off, and the current increases slowly with increasing Vds.This leads to the familiar DC characteristics shown in the Fig 2.3

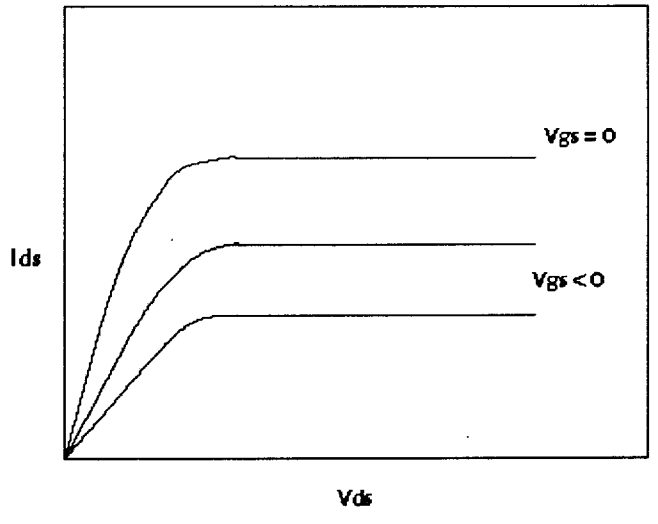


Fig 2.3 DC characteristics of GaAs FET

2.2.3 Equivalent Circuit Of GaAs MESFET

The small signal equivalent circuit of a GaAs FET in a common source configuration is as shown in Fig 2.4

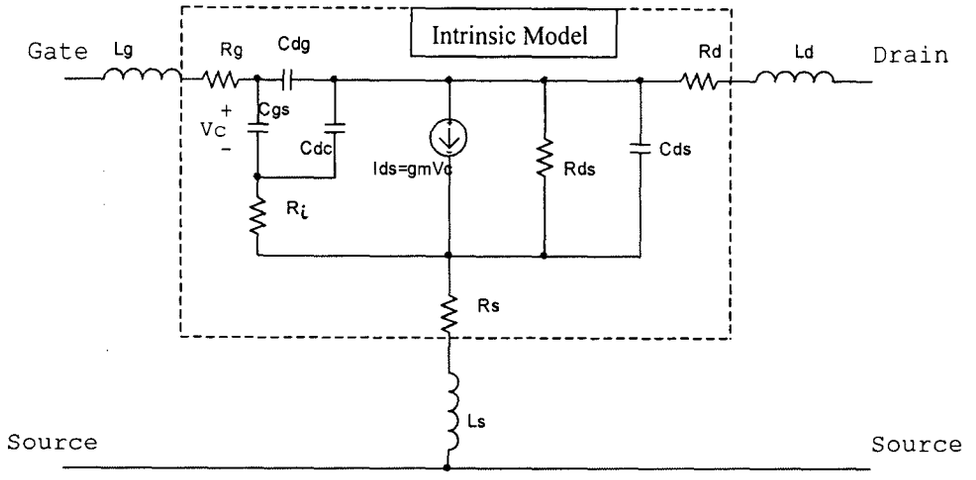


Fig 2.4 Equivalent circuit of GaAs FET

C_{gs} and C_{dg} is the total gate to channel capacitance intrinsic to the FET, Cdc models the gunn domain or dipole –layer capacitance & C_{ds} the parasitic substrate capacitance. R_i & R_{ds} show the effects of channel resistance, I_{ds} embodies the gain mechanism in a current source controlled by the voltage V_c via a transconductance $g_{m.}$ Parasitic resistances R_S, R_g & R_d are strongly dependent on processing technology & affect microwave noise performance. Parasitic inductance L_S, L_g & L_d are associated with bonding wires that contact the transistor chip to the external circuit or to the package.

2.2.4 Structure Of HEMT

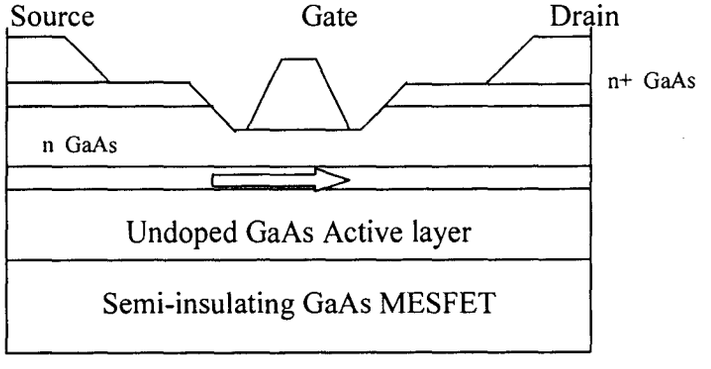


Fig 2.5 Structure of HEMT

A high electron-mobility transistor (HEMT), based on a modulation-doped GaAs-AIGaAs single hetrojunction structure, was developed by Fujitsu of Tokyo in the year 1979. In HEMT the density of the doping species is modulated so as to confine and control a two-

dimensional electron gas. Its frequency of operation is very high and is of the order of few tens of GHz. The HEMT offer low noise when compared to the GaAs MESFETs due to the high electron mobility in the device channel. The frequency of operation is also increased due to the same reason. The major improvements over MESFETs include shorter gate lengths, reduced gate and source contact resistances, and optimized doping profiles. Fig.2.5 gives structure of HEMT.

Unlike the MESFET, the channel is kept undoped, since; the doped donor atoms reduce the electron drift velocity and mobility. The charge carriers are electrons, which are supplied by the Aluminum in the AlGaAs layer. Since the undoped GaAs and AlGaAs have different band gap energies, the electron flow is confined to the interface between these two layers.

Thus the charge carriers are accumulated in the junction between these two layers, forming what is called an "electron gas" between these layers. These electrons have very high drift velocity and mobility, as there is no impurity scattering. The accumulated electron layer is extremely thin, so that, it can be assumed that the electrons within this layer have only two degrees of freedom. The low noise in the HEMT device is believed to be due to this, since the random motion of electrons, which causes noise, is limited to two dimensions. Due to the specific structure in HEMT, the electrons have higher mobility and also high sheet carrier density which results in high transconductance and a low noise figure than a GaAs MESFET.

2.2.5 Principle of operation of HEMT

The operation of HEMT is different from MESFET. In the latter, the depletion region width is modulated by the input signal, there by modulating the channel current. In HEMT, however, the channel width is fairly constant. It is the number of electrons flowing, which are regulated or modulated by the input signal .In other words, modulation on charge flow is direct. The I-V characteristics of HEMT is as shown in Fig 2.6

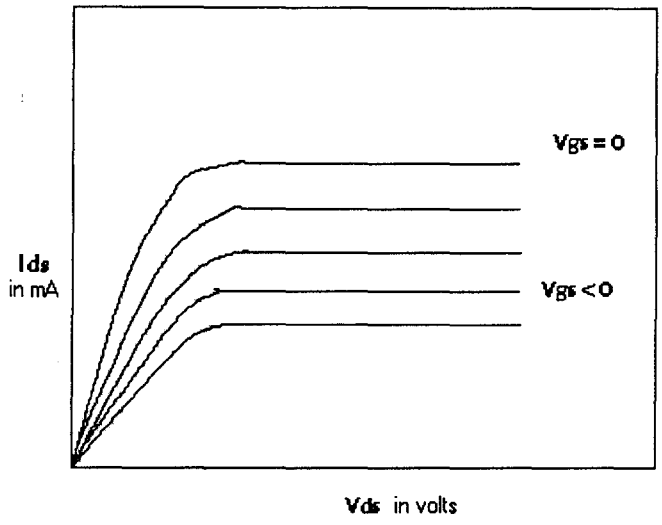


Fig 2.6 DC characteristics of HEMT

The major advantages of a HEMT are higher frequency, lower noise, and higher speed.

2.3 Different types of Noise in FETs

The sources of noise in FET can be broadly classified in to two

(i) Intrinsic noise sources

(ii) Extrinsic noise sources

(i) Intrinsic noise sources:

The noise sources intrinsic to the FET are thermal noise in channel and gate induced noise. The gate induced noise source is highly correlated with the noise generated in the channel since any fluctuation in the channel will induce a voltage at the gate. They primarily depend on the bias conditions.

(ii) Extrinsic Noise Sources:

The resistances associated with the FET, namely the gate metallization resistance Rg, the source resistance R_S and gate bonding resistance produce thermal noise within them. They form the major extrinsic sources of noise.

3. CIRCUIT THEORY

3.1 Scattering Parameters of a two-port network

The general theory of two port linear networks is well developed part of circuit theory. The behavior of any two-port network can be characterized by a (2×2) matrix whose elements may be Z (impedance), Y (admittance), h (hybrid) or ABCD parameters. These parameters cannot be measured accurately at high frequencies because the required short and open circuit tests are difficult to conduct at high frequencies. Also active devices such as transistors are very often not stable under open and short load conditions.

A set of parameters that characterize the behavior of two port network at microwave frequencies are defined in terms of travelling waves. These are called the scattering parameters (S parameters). The advantages of S parameters are simplicity in analysis and flow graph theory can be directly applied to them .S parameters can also be used in the characterization of ' N ' port networks.

The S parameters relate the outgoing waves b_i with the incident waves a_i at the input and output ports of a two-port network.

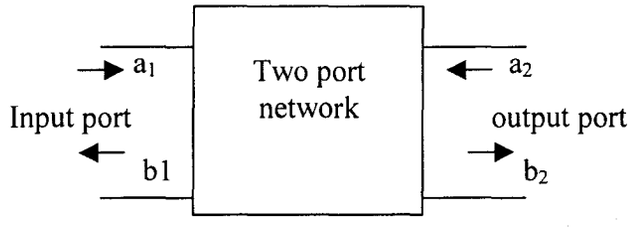


Fig 3.1 Two-Port Network

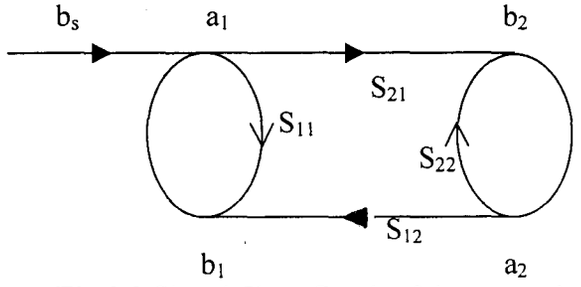


Fig 3.2 Signal Flow Graph of the network shown in Fig 3.1

$$\begin{bmatrix} b_1 \\ b_2 \end{bmatrix} = \begin{bmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{bmatrix} \begin{bmatrix} a_1 \\ a_2 \end{bmatrix}$$

where

a_1 represents the incident wave at the port 1

b_1 represents the reflected wave at the port 1

a_2 represents the incident wave at the port 2

b_2 represents the reflected wave at the port 2

Out of the four variables, the incident waves are taken as independent variables and the reflected waves are taken as the dependent variables.

Hence,

$$b_1=S_{11}a_1+S_{12}a_2$$

$$b_2=S_{21}a_1+S_{22}a_2 \qquad 3.0$$

The definition of various S parameters used in the equations above are defined below

Input reflection coefficient $S_{11}= (b_1 / a_1)\Big|_{a_2=0}$ 3.1

Forward transmission coefficient $S_{21}= (b_2 / a_1)\Big|_{a_2=0}$ 3.2

Output reflection coefficient $S_{22}= (b_2 / a_2)\Big|_{a_1=0}$ 3.3

Reverse transmission coefficient $S_{12}= (b_1 / a_2)\Big|_{a_1=0}$ 3.4

3.2 Network analysis of a Two-Port Network using S-Parameters

Let a two port be connected to a source V_S with a reflection coefficient Γ_S, at its input and a load Z_L with a reflection coefficient $\Gamma_{L,at}$ its output as shown in the Fig. 3.3

Let the scattering parameters of the two-port network be non-zero. Then the scattering parameters of the two port network connected to the source and the load are defined below Various equations given below can be obtained by applying the Mason's rule to the signal flow graph shown in Fig. 3.4.

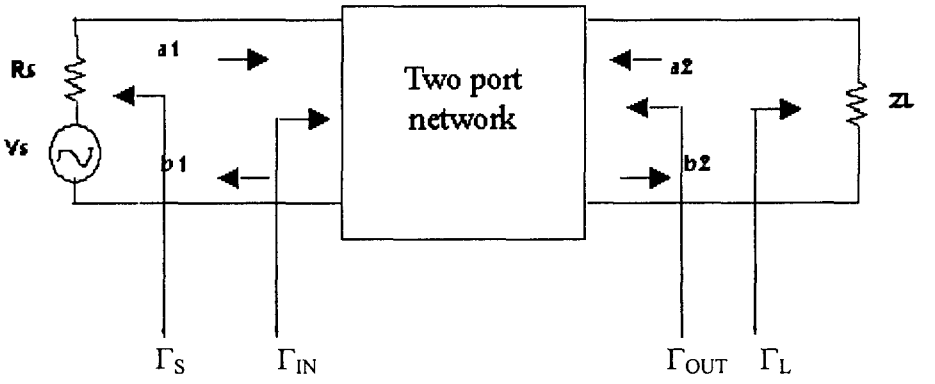


Fig.3.3 Two-port network with source and load

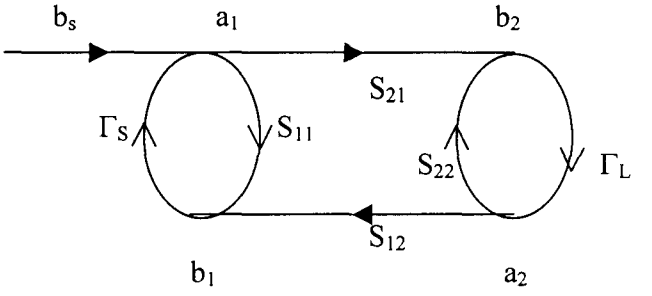


Fig 3.4 Signal flow graph of the two port network shown in Fig 3.3

Γ_S - source reflection co efficient

Γ_L - load reflection co efficient

b_S -signal contribution from the source

3.2.1 Basic definitions

Input reflection coefficient:

The input reflection coefficient Γ_{in} is the ratio of the reflected wave to the incident wave at the input terminals of the network. It is defined in terms of the S parameters of the two-port network, the source and the load reflection coefficients as follows:

$$\Gamma_{IN} = \frac{b1}{a1} \qquad 3.5$$

$$\Gamma_{IN} = S_{11} + \frac{S_{12}S_{21}\Gamma_1}{(1-S_{22}\Gamma_1)} \qquad 3.6$$

Output reflection co - efficient:

The output reflection coefficient Γ_{out} is defined as

$$\Gamma_{OUT} = \frac{b2}{a2} \qquad 3.7$$

$$\Gamma_{OUT} = S_{22} + \frac{S_{12}S_{21}\Gamma_S}{(1-S_{11}\Gamma_S)} \qquad 3.8$$

Transducer power gain:

The transducer power gain G_T is defined as

$$G_T = \frac{P_L}{P_{AVS}} = \frac{\text{Power delivered to the load}}{\text{Power available from the source}} \qquad 3.9$$

and is given by

$$G_T = \frac{1-|\Gamma_S|^2}{|1-\Gamma_{IN}\Gamma_S|^2} |S_{21}|^2 \frac{1-|\Gamma_L|^2}{|1-S_{22}\Gamma_L|^2} \qquad 3.10$$

$$= \frac{1-|\Gamma_s|^2}{|1-S_{11}\Gamma_s|^2} |S_{21}|^2 \frac{1-|\Gamma_L|^2}{|1-\Gamma_{OUT}\Gamma_L|^2} \qquad 3.11$$

Operating power gain:

The operating power gain G_P is defined as

$$G_P = \frac{P_L}{P_{IN}} = \frac{\text{Power delivered to the load}}{\text{Power input to the network}} \qquad 3.12$$

When $\Gamma_{IN} = \Gamma_S^*$, $P_{AVS} = P_{IN}$, under this condition G_T is called G_P

and is given by

$$G_P = \frac{1}{1-|\Gamma_{IN}|^2} |S_{21}|^2 \frac{1-|\Gamma_L|^2}{|1-S_{22}\Gamma_L|^2} \qquad 3.13$$

Available power gain:

The available power gain G_A is defined as

$$G_A = \frac{P_{AVN}}{P_{AVS}} = \frac{\text{Power available from the network}}{\text{Power available from the source}} \qquad 3.14$$

When $\Gamma_L = \Gamma_{OUT}^*$, $P_{AVN} = P_L$, under this condition G_T is called G_A and is given by

$$G_A = \frac{1-|\Gamma_S|^2}{|1-S_{11}\Gamma_S|^2} \; |S_{21}|^2 \; \frac{1}{1-|\Gamma_{OUT}|^2} \qquad 3.15$$

Simultaneous conjugate matching:

A two port network is said to be simultaneously conjugate matched if $\Gamma_{IN} = \Gamma_S^*$, and $\Gamma_{OUT} = \Gamma_L^*$. In these conditions * indicates the conjugate value of the corresponding parameters. In conjugate matching only the real parts of the source and the load impedance are matched simultaneously. The imaginary portions of the load impedance will be cancelled by incorporating the required reactive elements in the circuit.

3.2.2 Stability circles and its importance

The stability of an amplifier or its resistance to oscillate is a very important consideration in the design and it can be determined from the S-parameters, matching networks and the terminations.

In a two-port network, oscillations are possible when either input or output port presents a negative resistance. This occurs when $|\Gamma_{IN}| > 1$ or $|\Gamma_{OUT}| > 1$ .The two port

network is said to be unconditionally stable at a given frequency if the real parts of Z_{IN} and Z_{OUT} are greater than zero for all passive loads and source impedances.

If the two ports are not unconditionally stable it is potentially stable or conditionally stable that is some passive load and source terminations can produce input and output impedances having a negative real part.

The conditions for unconditional stability

$$|\Gamma_S| < 1 \qquad 3.16$$

$$|\Gamma_L| < 1 \qquad 3.17$$

$$|\Gamma_{IN}| = \left| S_{11} + \frac{S_{12} S_{21} \Gamma_L}{1 - S_{22} \Gamma_L} \right| < 1 \qquad 3.18$$

$$|\Gamma_{OUT}| = \left| S_{22} + \frac{S_{12} S_{21} \Gamma_S}{1 - S_{11} \Gamma_S} \right| < 1 \qquad 3.19$$

For a conditionally stable amplifier, the stability circles give the boundaries between the stable and unstable regions on the Smith chart.

The radii and centers of the circle where $|\Gamma_{IN}| = 1$ and $|\Gamma_{OUT}| = 1$ in the $|\Gamma_L|$ plane and $|\Gamma_S|$ planes respectively are given below

Γ_L values for $|\Gamma_{IN}| = 1$ (Output stability circle)

$$R_L = \left| \frac{S_{12}S_{21}}{|S_{22}|^2 - |\Delta|^2} \right| \quad \text{(radius)} \qquad 3.20$$

$$C_L = \left| \frac{(S_{22} - \Delta S_{11}^*)^*}{|S_{22}|^2 - |\Delta|^2} \right| \quad \text{(center)} \qquad 3.21$$

Γ_S values for $|\Gamma_{OUT}| = 1$ (input stability circle)

$$R_S = \left| \frac{S_{12}S_{21}}{|S_{11}|^2 - |\Delta|^2} \right| \quad \text{(radius)} \qquad 3.22$$

$$C_S = \left| \frac{(S_{11} - \Delta S_{22}^*)^*}{|S_{11}|^2 - |\Delta|^2} \right| \quad \text{(center)} \qquad 3.23$$

For the device to be stable the input and output stability circles should lie outside the smith chart. Fig.3.5 shows a typical input and output stability circles of an amplifier on the smith chart. The impedances offered by it both at the input and the output should not lie in the shaded regions as shown in the figure for stable operation.

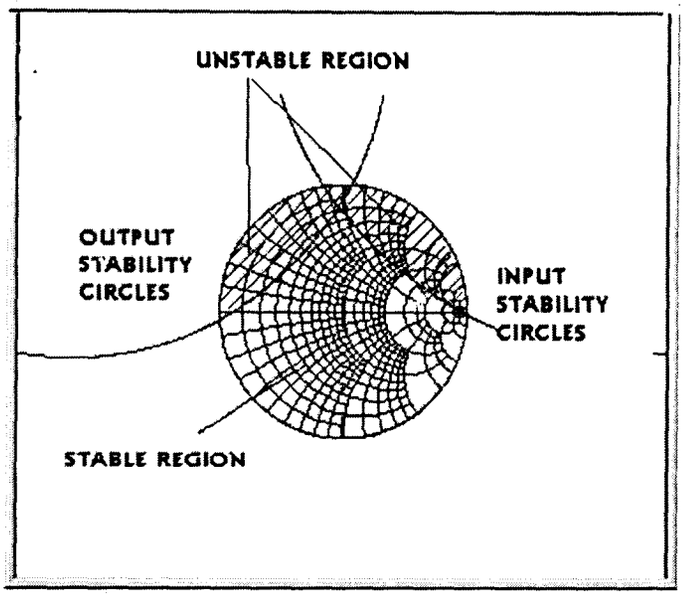


Fig 3.5 Smith chart showing input and output stability circles

A two-port network is said to be unconditionally stable provided the following necessary and sufficient condition is satisfied.

$$K = \frac{1-|S_{11}|^2 - |S_{22}|^2+|\Delta|^2}{2|S_{12}S_{21}|} > 1 \qquad 3.24$$

$$\Delta = |S_{11}S_{22} - S_{12}S_{21}| < 1 \qquad 3.25$$

K=1 implies network is marginally stable and K<1 implies network is potentially unstable.

3.3 Noise parameters of the transistor

The noise figure of any device can be characterized by four parameters

(i) F_{min} : Minimum Noise Figure

(ii) R_{opt} : Real part of the optimum source impedance for minimum noise

(iii) X_{opt} : Imaginary part of the optimum source impedance for minimum noise

(iv) R_n : Equivalent Noise resistance

The noise figure of the device is given by

$$F = \frac{F_{min}}{G_s} + r_n \left| Y_s - Y_{opt} \right|^2 \qquad 3.26$$

Where,

r_n = Normalized equivalent Noise resistance(R_n/Z_0)

G_s = Real part of source admittance

Y_s = Source admittance

Y_{opt} = Optimum source admittance

3.4 Methods of achieving Low Noise

As given in EQN (3.26), the Noise Figure F depends directly on the values of r_n and Y_s. Conditions for minimum Noise Figure are

(i) r_n - minimum

(ii) $Y_s = Y_{opt}$

Lower the value of resistance lesser will be the opposition to the flow of electrons and hence the fluctuations in the flow of electrons. When the fluctuations are less in the flow of current, minimum noise can be achieved. This is illustrated in Fig 3.6.

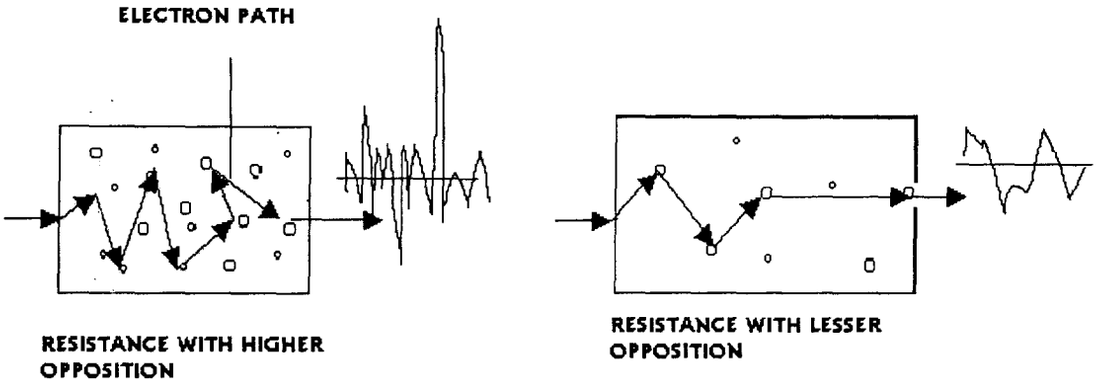


Fig 3.6 The effect of resistance in the fluctuation of electric current

The value of r_n is decided by Transconductance g_m of the transistor and their relationship is given in FIG 3.7.It shows that as the transconductance is increased the normalized noise resistance decreases. Hence to have low Noise we must have higher value of g_m.

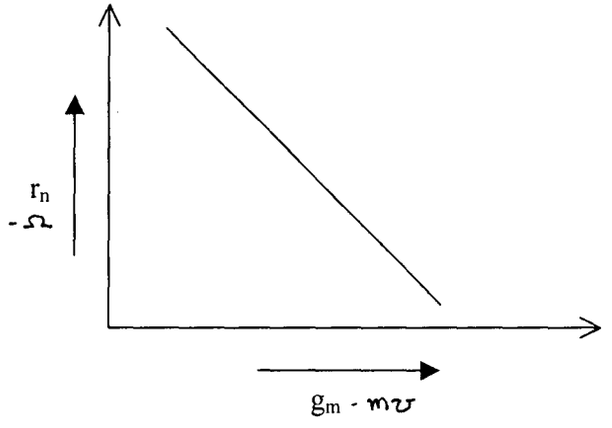


Fig 3.7 Relationship between g_m (m ʊ) and r_n (Ω)

In other words higher value of g_m implies higher current for a given voltage. Higher current can be achieved if the electrons posses have higher mobility (μ). The equation justifying this statement is given below

The conduction current density, Jc= I/A = nev

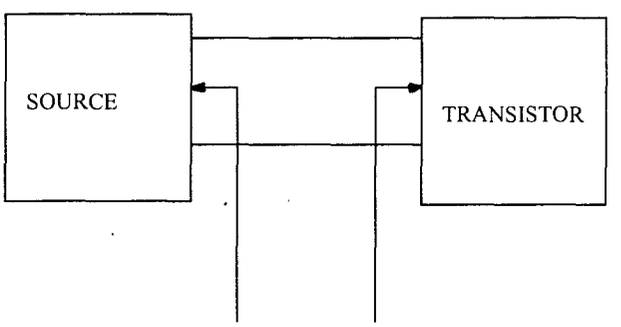
$$\Longrightarrow \quad I = nevA$$

$$= ne\mu EA \qquad 3.27$$

Where, A = Cross-sectional area of the conductor
n = Number of electrons
e = Electron charge
μ = Electron mobility
E = Electric field
v = Velocity of electrons

DEVICES HAVING HIGHER ELECTRON MOBILITY CONTRIBUTE LESS NOISE HEMT is one such device.

The Noise at the Gate and the Drain are correlated with each other. By making $Ys=Y_{opt}$ i.e., optimizing the source impedance, the phase of the signal at Gate is adjusted so that the correlated components of Noise at the Gate and Drain cancel each other at the Drain.



$\Gamma_s=\Gamma_{opt}$ $\Gamma_{in}=\Gamma_{opt}^*$

Fig 3.8 Source matching for low noise

3.5 Gain circles and noise circles

The unilateral power gain when $\Gamma_S = S_{11}^*$ and $\Gamma_L = S_{22}^*$ is given by

$$G_i = \frac{1 - |\Gamma_S|}{|1 - S_{ii}\Gamma_i|} \qquad 3.29$$

when $\Gamma_i = \Gamma_S$ (source)

$S_{ii} = S_{11}$

When $\Gamma_i = \Gamma_L$ (Load)

$S_{ii} = S_{22}$

The maximum value of the above gain is given by

$$G_{iMAX} = 1 / 1 - |S_{11}|^2 \qquad 3.30$$

The termination, which produces maximum gain, is called optimum termination. For $|\Gamma_{ii}| = 1$, the gain achieved will be minimum. Other values of Γ_{ii} between S_{ii}^* and 1 produce different gain in between 0 and maximum. The value of G_i, which produces a constant gain, is shown to lie on a circle in a smith chart. These circles are called constant gain circles.

Constant Noise figure circles

As it is already mentioned in previous section, the noise figure of a two port network is characterized by four parameters R_n, F_{min}, $Re(\Gamma_{opt})$, $Im(\Gamma_{OPt})$ and is given by

$$F = F_{min} + \frac{R_n}{g_s} \left| Y_S - Y_{opt} \right|^2 \qquad 3.31$$

If we express Y_S and Y_{OPT} in terms of reflection coefficients and substitute them in the noise figure expression, the resulting equation will represents a circle. Different values of Γ_S for a given noise figure F, will lie on this circle. The equations for these circles can be found, given the parameters Γ_{opt},F_{min} and r_n.

The center and radius of these circles is given by

$$C_{Fi} = \frac{\Gamma_{opt}}{1+N_i} \qquad 3.32$$

$$R_{Fi} = \frac{1}{1+N_i}\sqrt{N_i^2+N_i(1-|\Gamma_0|^2} \qquad 3.33$$

$$\text{Where } N_i = \frac{F_i-F_{min}}{4r_n}\left|1+\Gamma_0\right|^2 \qquad 3.34$$

A typical set of constant noise figure circles is given in Fig.3.9

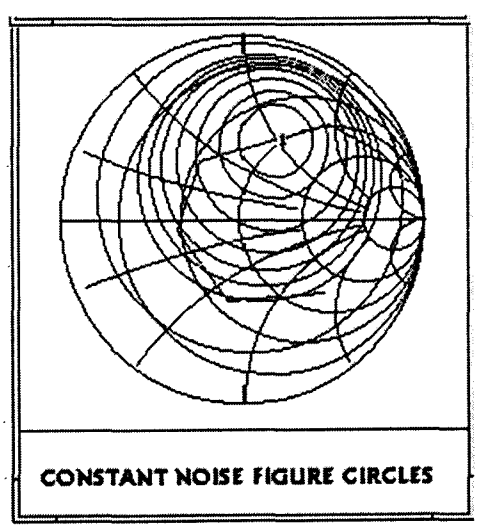


Fig.3.9 Constant Noise Figure Circles

The center of $F_i = F_{min}$ circle is located at Γ_{opt} with zero radius,that is,when

$$F_i = F_{min}$$
$$N_i = 0$$
$$C_{Fmin} = \Gamma_{opt}$$
$$R_{Fmin} = 0$$

The centers of all other noise figure are located along Γ_{opt} vector.

Constant gain circles can be overlaid on the noise figure circles. The resulting plot will clearly indicate the trade offs between gain and noise figure that have to be made in the design of low noise stages as maximum gain and minimum noise figure cannot be obtained simultaneously.

4. DESIGN OF THE AMPLIFIER

This chapter discusses the design procedure of a wideband Low Noise Amplifier and its simulated response using the RF CAD Package Genesys 7.5. The various specifications for which the amplifier has been designed are discussed below

Specification

- Frequency range of operation : 5-7 GHz
- Noise figure of the amplifier: as minimum as possible (0.7dB)
- Flat gain response
- Unconditional stability in the operation of the amplifier.

4.1 General block diagram of an amplifier

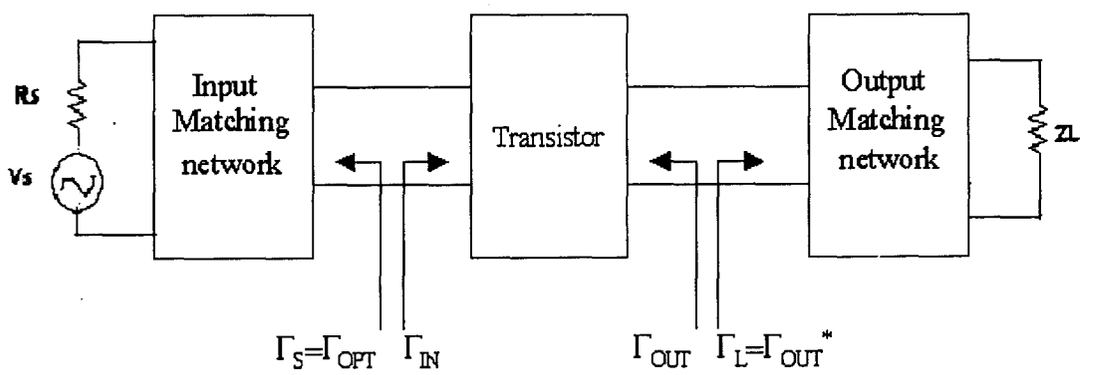


Fig 4.1 General block diagram of an amplifier

Fig 4.1 shows the general block diagram of an Amplifier. It consists of input matching network, which transforms the source impedance to the optimum impedance of the transistor for minimum Noise figure, and the output-matching network, which transforms output impedance of the transistor to the load impedance.

4.2 Electrical characteristics of the High Electron Mobility Transistor - HEMT FHC40LG

High Electron Mobility Transistor - FHC40LG has been chosen to build the amplifier in the desired frequency range since this has got lower Noise figure over the entire range.
The Noise parameters given in Table 4.1 are obtained when

Vds = 2V

Id = 10mA

Table 4.1 The Noise parameters of HEMT FHC40LG

Frequency (GHz)	NF_{min} (dB)	Γ_{OPT}		Rn/50
		MAG	ANG	
2	0.28	0.86	31	0.19
4	0.30	0.87	57	0.18
6	0.34	0.86	83	0.13
8	0.39	0 .81	108	0.09
10	0.47	0.74	132	0.05
12	0.55	0.63	156	0.03
14	0.67	0.49	179	0.04
16	0.81	0.33	-158	0.07
18	1.00	0.13	-136	0.11

4.3 Use of negative feed back technique to improve the stability of the device

The stability factor K was calculated from 5 to 7GHz and found to be less than 1 as shown in table 4.2. This implies that the transistor is potentially unstable at these frequencies and has a tendency to oscillate. The input and output impedances for which the amplifier oscillates lie in a region between the Smith chart and the overlapped stability circle. This is shown in Fig 4.2. The constant gain circles, constant noise circles (Fig.4.3) and stability circles (Fig.4.2) were drawn using the Genesys RF CAD package. It was found that the centers of the circles that represent maximum gain and minimum noise figure respectively were far separated. This means it is not possible to simultaneously match gain and noise for this transistor at this frequency. Also, the maximum gain point was lying at the edge of the Smith chart very close to the input and output stability circles. This means that the impedance to be provided to the transistor has to be chosen very carefully so that the amplifier does not become unstable.

Table 4.2 frequencies versus stability factor without inductance

Frequency	K Factor
5000	0.568
5200	0.589
5400	0.611
5600	0.634
5800	0.657
6000	0.681
6200	0.704
6400	0.729
6600	0.754
6800	0.78
7000	0.808

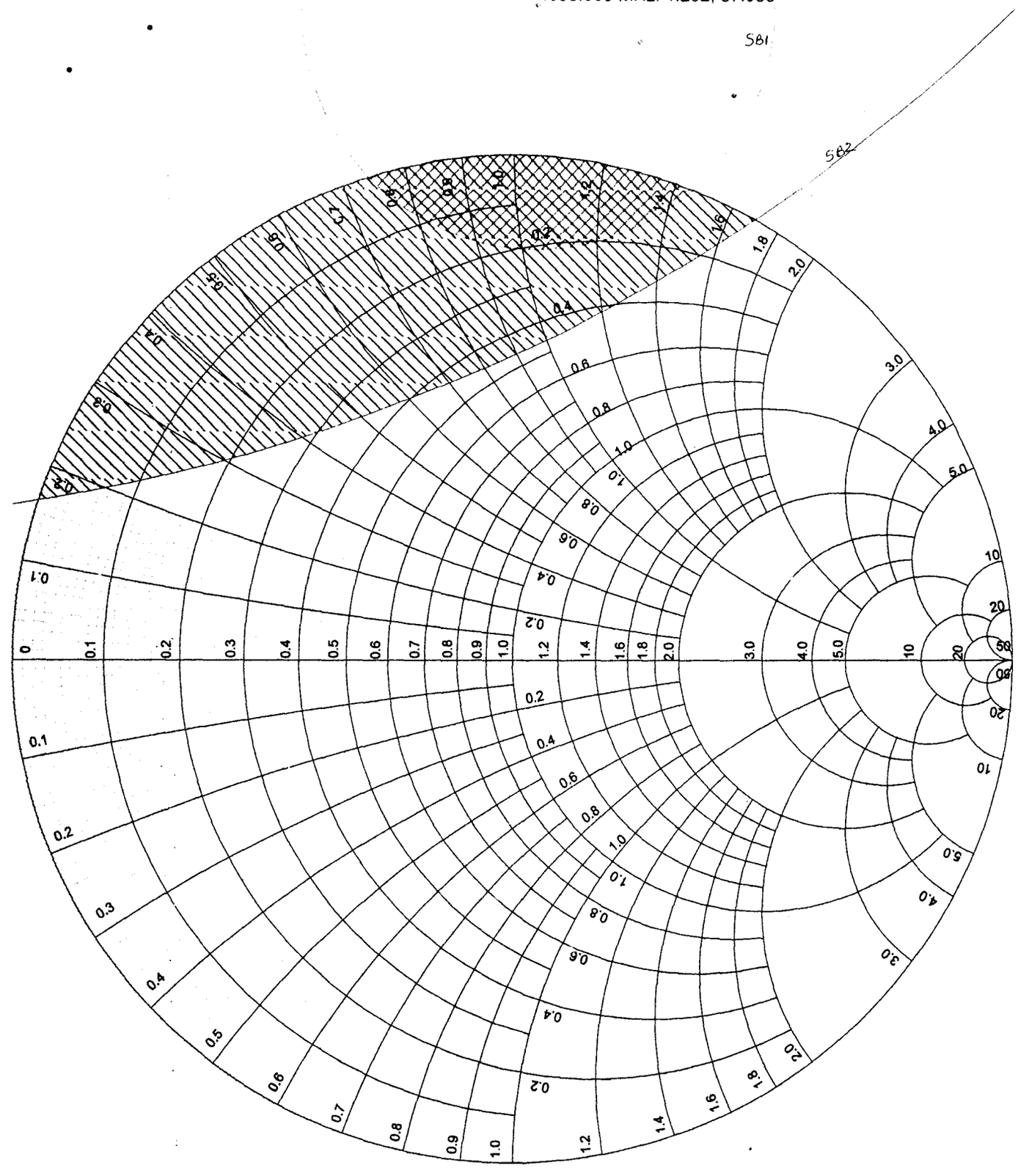


Fig 4.2: Stability circles of the Transistor without any feedback.

To overcome both these problems of stability and simultaneous matching of noise and gain, a small inductance is added to the source. A small inductance to ground at the source has an equivalent effect to the first order of adding a noiseless resistor of value $(g_m/C_{gs}) \times Ls$ at the input of the transistor, where g_m is the transconductance of the transistor, Cgs is the gate to source capacitance and Ls is the source inductance added. The modified S-parameters and the value of source inductance that makes k factor greater than 1 & also to make the input and output stability circles lie of smith chart, at the frequency range specified can be obtained by manually varying the value of Ls using Genesys. In this case it was found to be 0.101nH. The stability circles after addition of inductor value of 0.101nH to the source are shown in table 4.3 and figure 4.4 respectively.

Table 4.3

Frequency	K Factor
5000	1.015
5200	1.039
5400	1.06
5600	1.077
5800	1.091
6000	1.1
6200	1.104
6400	1.103
6600	1.099
6800	1.09
7000	1.078

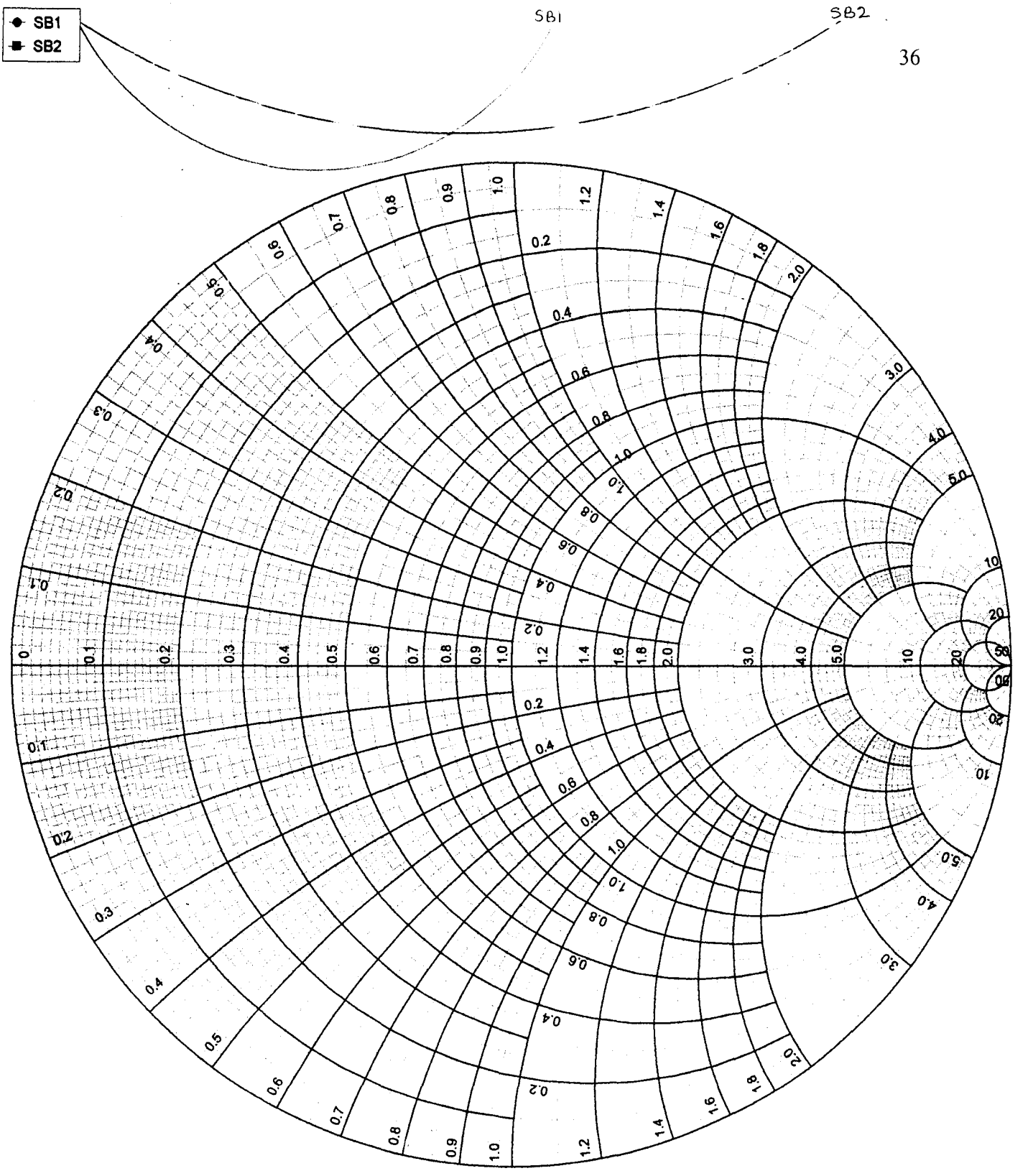


Fig 4.4 Stability circles with inductor in feedback path

4.4 Design of input and output matching section

Impedance matching techniques

One of the most important aspects of high frequency, circuit design is impedance matching. It is necessary to achieve

- Maximum power transfer between source and load
- Minimum power loss in the feed line
- Improvement in the signal to noise ratio of a receiver system by impedance matching sensitive receiver components like antenna, low noise amplifier etc.
- Minimum Noise contribution from the Amplifier.
- Must operate over a wide range of frequencies.

One of the most fundamental criteria is that a matching network must be ideally lossless to avoid unnecessary loss of power and others being simplicity, bandwidth, easy implementation and adjustability.

Different techniques of impedance matching are

(1) L-section impedance matching
(2) Single stub tuning
(3) Double stub tuning
(4) The quarter wave transformer
(5) Multisection transformer
    - Binomial multisection transformer
    - Chebyshev multisection transformer
(6) Tapered lines
    - Exponential taper
    - Triangular taper
    - Klopfenstein taper

Choice of an impedance matching technique depends on the application. The first three techniques mentioned here are not useful for wide band applications. Though multisectioin quarter wave transformers can be used for wide band applications, the overall length of the transformer becomes large as the number of sections is increased. Out of all, tapered line is the most optimum section for achieving all our requirements. The length of it is fixed at half the wavelength at lowest operating frequency.

Tapered lines

In a tapered transmission line the width of the line varies gradually from one value to another over a specified length with out giving rise to any discontinuities. Thus it has better reflection coefficient as compared to multisection transformer. Also tapered lines provide matching over an infinite bandwidth.

Various kinds of tapered lines possible are

(i) Exponential taper,

(ii) Triangular taper,

(iii) Klopfenstein taper.

Among everything Klopfenstein taper is considered to be most optimum. The performance of the Klopofenstein taper is optimum in the sense that for a given taper length the input reflection coefficient is minimum over the entire passband, and for a specified tolerance of reflection co-efficient magnitude, the taper has minimum length.

Analysis of Klopfenstein tapered design

Typically a tapered transmission line is as shown in Fig 4.5

The design of Klopfenstein tapered transmission line has been done following the design procedure given in the paper " A transmission Line Taper of Improved Design"- R.W.Klopfenstein(Proceedings of the IRE 1955)

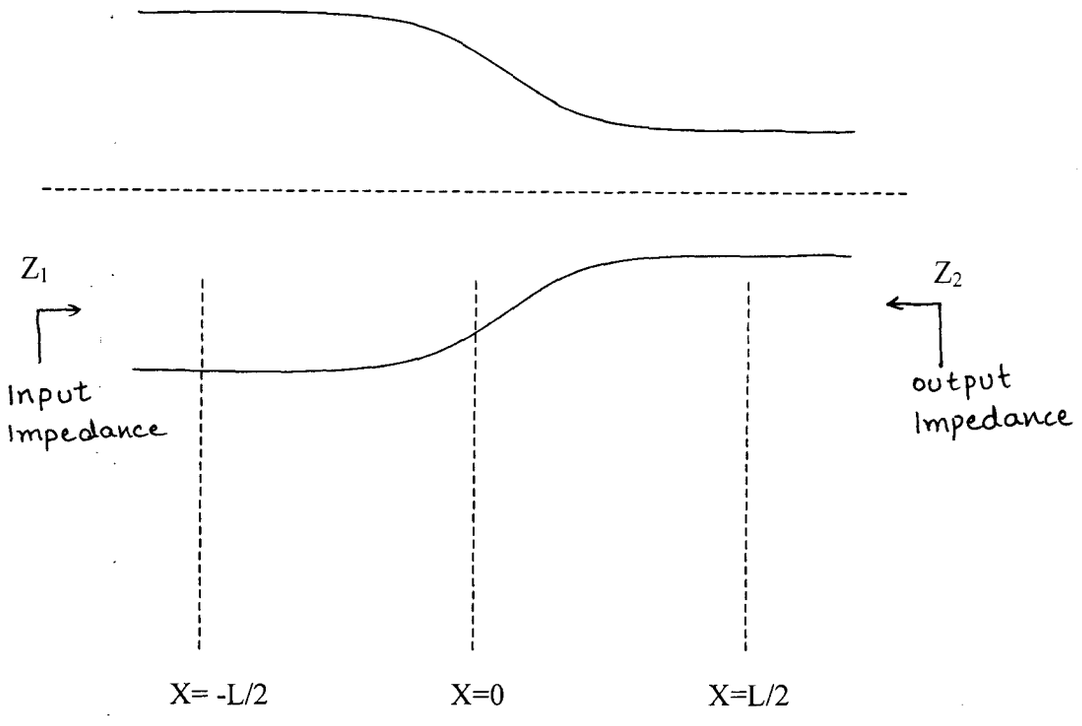


Fig 4.5 Klopfenstein Tapered Line

For maximum bandwidth with a fixed maximum reflection co efficient for a continuous taper takes the form

$$\Gamma \exp(j\beta l) = \Gamma_0 \frac{\cos\left[\sqrt{(\beta L)^2 - A^2}\right]}{\cosh(A)} \qquad 4.1$$

A is a parameter which determines the maximum reflection co-efficient in Γ_m the pass band which consists of all frequencies such that $\beta l >= A$.

The reflection co efficient takes on its maximum value $|\Gamma_0|$ at zero frequency and it oscillates in the passband with constant amplitude

Where

- U is the unit step function defined by,

$$U(Z) = 0 \qquad Z < 0 \qquad 4.3$$
$$U(Z) = 1 \qquad Z \geq 0$$

- ϕ is defined by

$$\phi(Z,A) = -\phi(-Z,A) = \int_0^Z \frac{I_1(A\sqrt{1-y^2})}{A\sqrt{1-y^2}}\, dy \qquad |Z| \leq 1 \qquad 4.4$$

For values of $\phi(z, A)$ for various values of $20\log_{10}\cosh A$ refer appendix

which takes special values $\phi(0,A) = 0$

$\phi(x,0) = Z/2$

$\phi(1,A) = \cosh(A) - 1/A^2$

- Γ_0 is the reflection co efficient at zero frequency given as

$$\Gamma_0 = \frac{Z_2 - Z_1}{Z_2 + Z_1} = 1/2\ \mathrm{Ln}\,(Z_2 / Z_1) \qquad 4.5$$

A plot of Z0 versus X/L is as follows

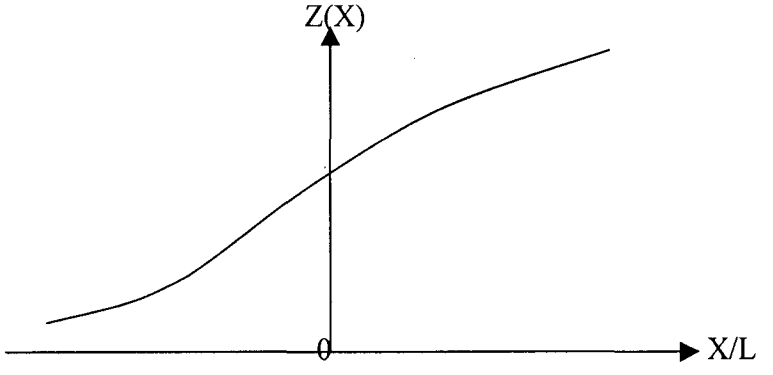


Fig 4.7 Variation of impedance in a Klopfenstein tapered line

Design of input matching section

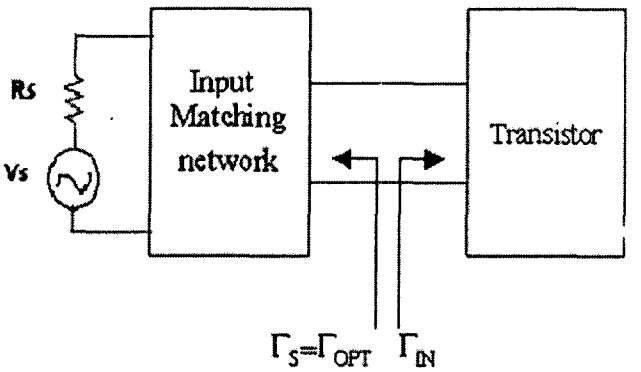


Fig 4.8 Design of Input matching section-block diagram

$R_S = 50\Omega$

Klopfenstein tapered lines has been used to transform the source impedance to Γ_{OPT} of the HEMT at 6.7 GHz.The value of Γ_{OPT} was read at 6.7GHz and the value of impedance corresponding to Γ_{OPT} was found to be 8.836+j 42.778. Hence 50Ω source was matched to 8.836Ω using tapered line and an inductor of 1.0161nH was connected to account for the imaginary part.

Design of Klopfenstein tapered line

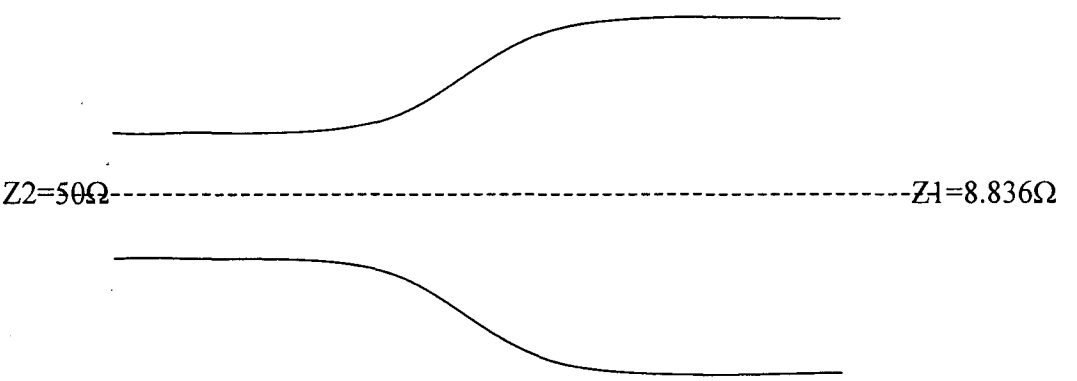


Fig 4.9 Ideal Klopfenstein tapered line for the input section

This tapered line was realized using 10 sections as in figure 4.10 and the length of each section is L/10 =λ/20.

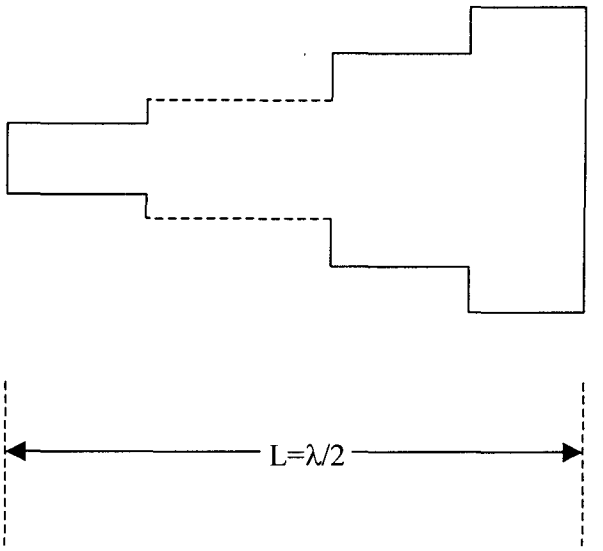


Fig 4.10 Practical realization of the Klopfenstein tapered line

1. Reflection Co-efficient (initial value)

$$\Gamma_0 = 1/2 \ln(Z_2/Z_1)$$

$$= 1/2 \ln(50/8.836)$$

$$= 0.866594$$

2. It is required that the maximum reflection co-efficient magnitude in the pass band shall not exceed $1/20^{th}$ of Γ_0

$$\cosh(A) = 20 = \frac{\Gamma_0}{\Gamma_m}$$

$$A = 3.68825$$

$$\begin{aligned} \text{LnZ}(x) &= 1/2 \ln(Z_1Z_2)+\Gamma_0/\cosh(A)\{A^2\Phi(2x/L,A)+U(x-L/2)+U(x+L/2), && |x| \le L/2 \\ &= \text{Ln}(Z_2), && x > L/2 \\ &= \text{Ln}(Z_1), && x < -L/2 \end{aligned}$$

The values of the impedance and width of each section is given in Table 4.4 The width was calculated using Genesys for ULTRALAM PCB for a rectangular microstip with ∈r value of 2.5 at the lower cutoff frequency 5 GHz.

Table 4.4 The values of the impedance and width of each section in the input Tapered line

X	Φ(2x/l,A)	U(x-L/2)	U(x+L/2)	ln(Z_0)	Z_0	Width of microstrip line
-0.5L	-1.316391	0	1	2.3128	10.103	16.703
-0.4L	-1.182484	0	1	2.3917	10.933	15.304
-0.3L	-0.976019	0	1	2.5134	12.348	13.357
-0.2L	-0.698767	0	1	2.6769	14.540	11.096
-0.1L	-0.365055	0	1	2.8735	17.700	8.834
0	0	0	1	3.0887	21.949	6.832
0.1L	0.365055	0	1	3.3039	27.219	5.232
0.2L	0.698767	0	1	3.5006	33.136	4.054
0.3L	0.976019	0	1	3.6640	39.019	3.2469
0.4L	1.182484	0	1	3.7857	44.068	2.7317
0.5L	1.316391	1	1	3.9079	49.799	2.2787

Design of output matching section

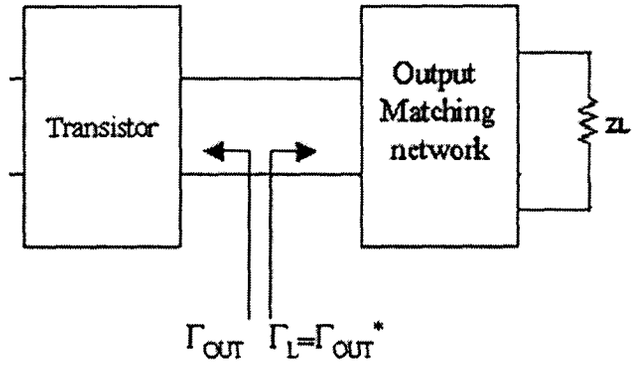


Fig.4.11 Design of output matching section-block diagram

Z_L= 50Ω

1. Reflection Co-efficient (initial value)

$$\Gamma_0 = 1/2\ \mathrm{Ln}(Z_2/Z_1)$$

$$= 1/2\ \mathrm{Ln}(50/8.836)$$

$$= 3.571428$$

2. It is required that the maximum reflection co-efficient magnitude in the pass band shall not exceed $1/20^{th}$ of Γ_0

$$\cosh(A) = \Gamma_0/\Gamma_m = 20$$

$$A = 3.68825$$

$$\mathrm{Ln}Z(x) = 1/2\ \mathrm{Ln}(Z_1Z_2)+\Gamma_0/\cosh(A)\{A^2\Phi(2x/L,A)+U(x-1/2)+U(x+1/2), \quad |x| \leq L/2$$

$$= \mathrm{Ln}(Z_2), \quad x > L/2$$

$$= \mathrm{Ln}(Z_1), \quad x < -L/2.$$

The values of the impedance and width of each section is given in Table 4.5

The width was calculated using Genesys for ULTRARAM PCB for a rectangular microstip with $\in r$ value of 2.5 at the lower cutoff frequency 5 GHz.

Table 4.5

X	Φ(2x/l,A)	U(x-L/2)	U(x+L/2)	ln(Z_0)	Z_0	Width of microstrip line
-0.5l	-1.316391	0	1.0	2.7036	14.934	10.761
-0.4l	-1.182484	0	1.0	2.7362	15.852	10.046
-0.3l	-0.976019	0	1.0	2.8552	17.379	9.025
-0.2l	-0.698767	0	1.0	2.9787	19.664	7.799
-0.1l	-0.365055	0	1.0	3.1274	22.816	6.517
0	0	0	1.0	3.2900	26.845	5.325
0.1l	0.365055	0	1.0	3.4527	31.587	4.318
0.2l	0.698767	0	1.0	3.6013	36.649	3.539
0.3l	0.976019	0	1.0	3.7249	41.468	2.981
0.4l	1.182484	0	1.0	3.8168	45.463	2.614
0.5l	1.316391	1	1	3.9093	49.865	2.274

The schematic of the over all amplifier circuit including the coupling capacitors, matching inductors and the transistor as realized using Genesys is as in Fig.4.14 and the layouts of the matching sections are as shown in Fig 4.15.

The length of the tapered line is calculated from the following relationship

$\beta L \geq A$ where $\beta = 2\pi/\lambda$

$L \geq (A\lambda_{medium}/2\pi)$; $\lambda_{medium} = \frac{\lambda_0}{\sqrt{\epsilon_r}}$; where $\lambda_0 = \lambda_{air} = \frac{c}{f_{(lower\ cut\ off)}} = \frac{3\times10^8\ m/s}{5\times10^9\ Hz} = 6cm$

For λ_0=6cm and A=3.688

$L \geq (A\lambda/2\pi\sqrt{\varepsilon_r})$ where ε_r is the permitivity of the medium(=2)

L=25mm

As we have considered 10 sections ,the length of each section is 25mm/10 = 2.5 mm

The Layout for the above design is as shown in fig 4.14.

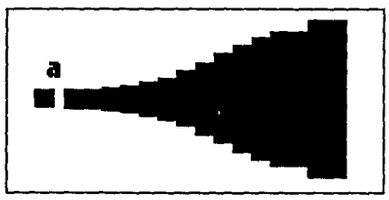


Fig.4.15(a) Input Section Layout

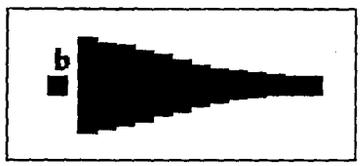


Fig.4.15(b) Output Section Layout

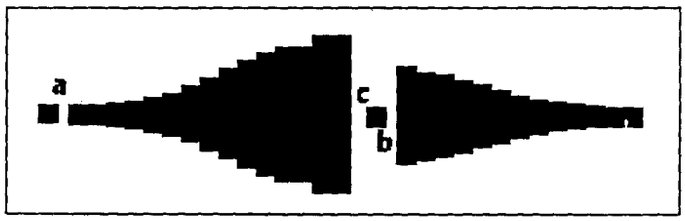


Fig.4.15(c) Overall Amplifier Layout

a is the gap for input coupling capacitor

b is the gap for output coupling capacitor

c is the gap for the transistor

Fig.4.15 Layouts of the amplifier

4.5 Modified values of the input and output matching network for optimum performance

The design was optimized using Genesys for optimum performance over 3 to 9 GHz.The modified input and output sections layout is as in figure 4.16.

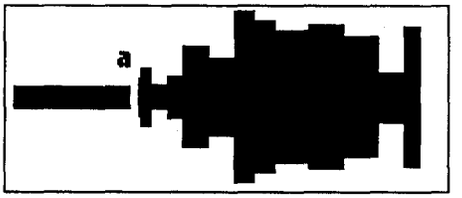


Fig.4.16(a) Input Section Layout

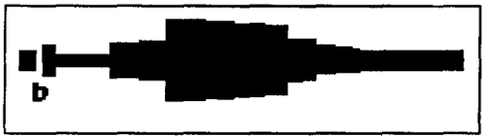


Fig.4.16(b) Output Section Layout

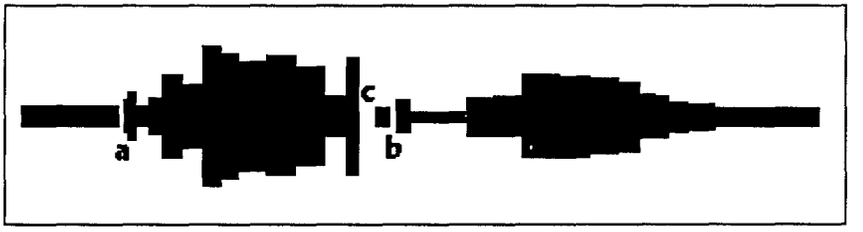


Fig.4.16(c) Overall Amplifier Layout

a is the gap for input coupling capacitor

b is the gap for output coupling capacitor

c is the gap for the transistor

Fig.4.16 Modified layouts of the amplifier

The schematic of the modified circuit is same as in Fig.4.14 . The coupling capacitors are chosen in such a way that their resonant frequency are much higher than the frequency of operation .The data sheet of the capacitor is found in the appendix.

4.6 Design of biasing section

The circuit used to provide biasing to the transistor is as shown in Fig 4.16.The resistance in the bias path is chosen such that the drain is maintained at 2V and a current of 10mA is passed through the device when 3V, is applied to the bias. The by pass capacitors are chosen such that they offer very low impedance at the frequency of operation

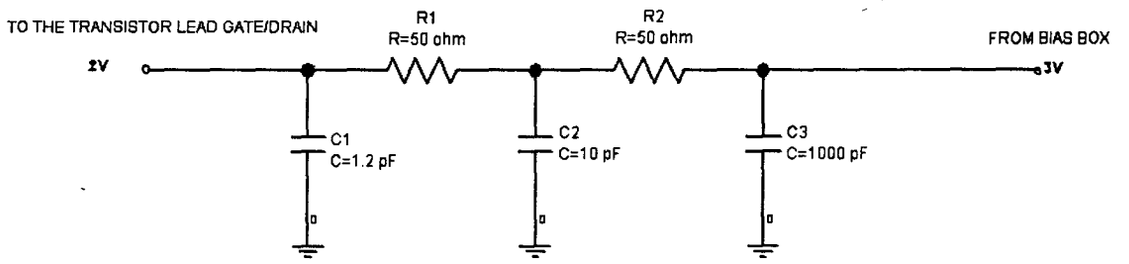


Fig 4.17 Biasing circuit for the transistor

The circuit diagram of the Amplifier is as shown in Fig 4.18

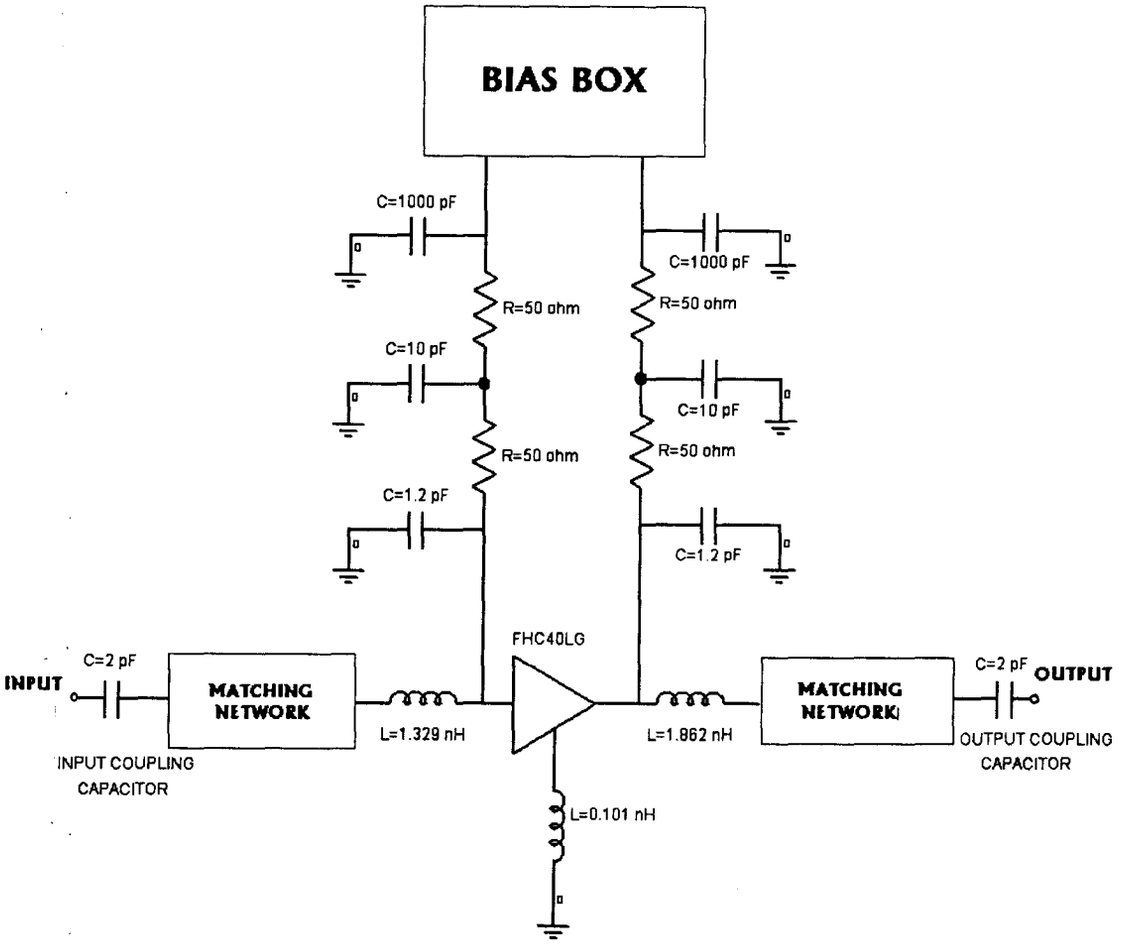
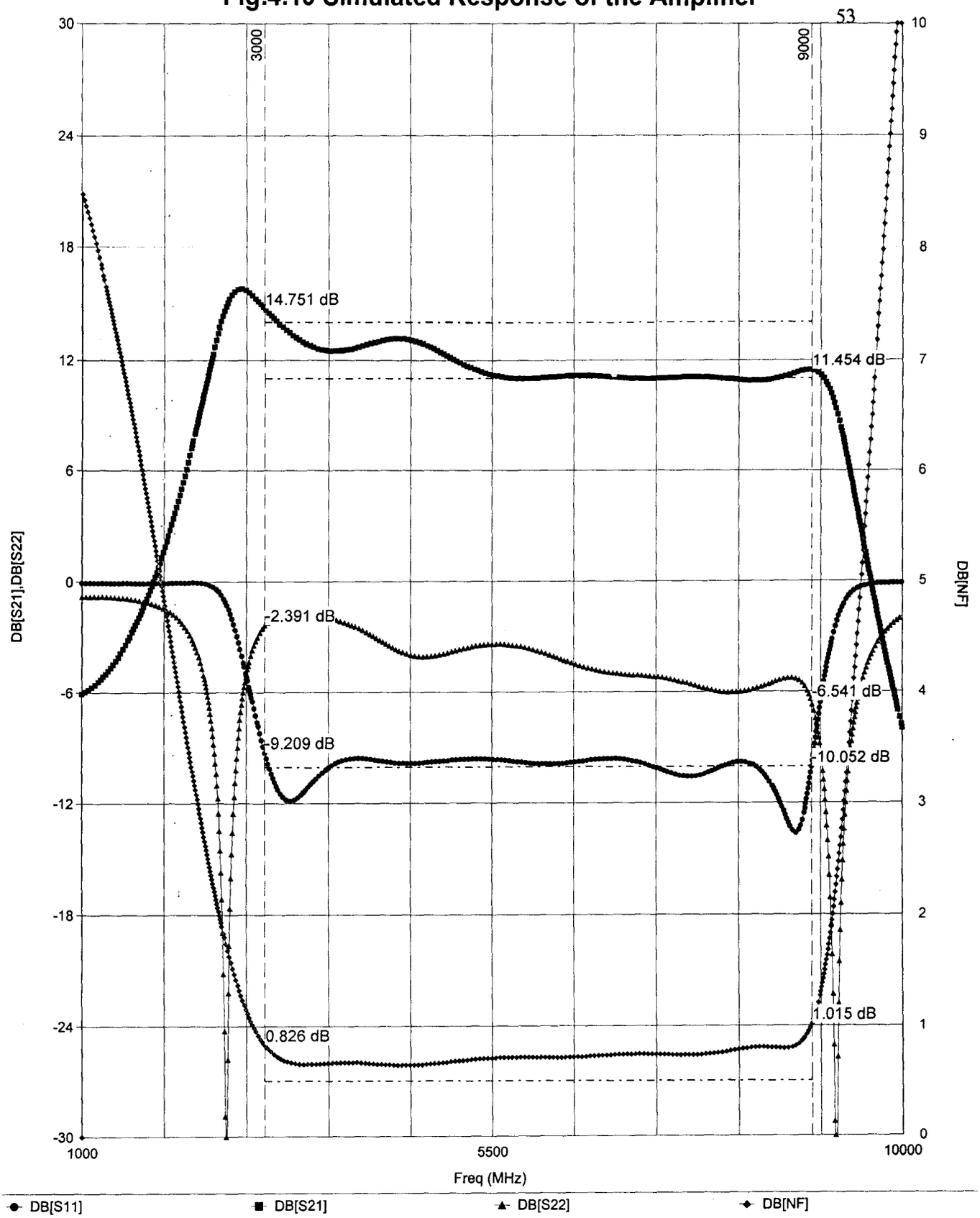


Fig 4.18 The Circuit diagram of the Low noise Amplifier

4.8 Simulation response of the amplifier

With the modified input and out put matching circuits the response of the amplifier is as in Fig.4.19. The response shows that the minimum noise figure can be obtained between 3GHz to 9GHz with an input return loss of about 10dB. The gain droop achieved over the above frequency range is approximately 3dB.

Fig.4.19 Simulated Response of the Amplifier

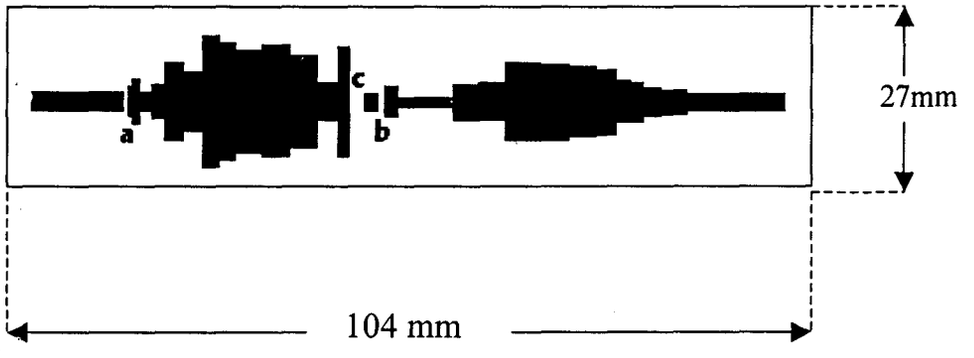


5. BUILDING AND CHARACTERIZATION OF THE LOW NOISE AMPLIFIER

5.1 Construction details of the amplifier

5.1.1 Amplifier card

The circuit was realized on ULTRALAM 2000 PCB from Rogers Corporation. ULTRALAM 20000 laminate is made of woven glass Teflon reinforced PTFE.This is designed for high reliability stripline and microstrip circuit applications. The dielectric constant $\in r$ of this laminate is typically 2.5. It has a low dissipation factor, tanδ of 0.0022 maximum of 10 GHz.The layout of the low noise amplifier etched on this PCB is shown in the Fig 5.1



a is the gap for input coupling capacitor
b is the gap for output coupling capacitor
c is the gap for the transistor

Fig 5.1 PCB Layout of the Amplifier

5.1.2 Transistor holder

The transistor would enter into oscillations due to the large value of parasitic inductance in its source lead. In order to avoid this the source leads are well grounded by mounting on a metallic holder. The mechanical diagram of the holder is given in figure 5.2.

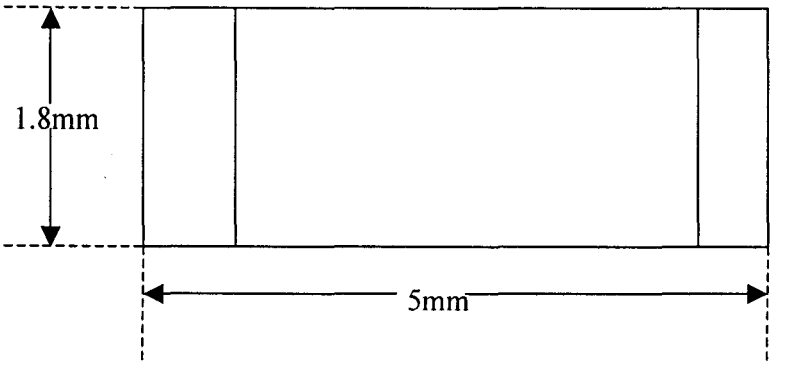


Fig.5.2(a) Top view

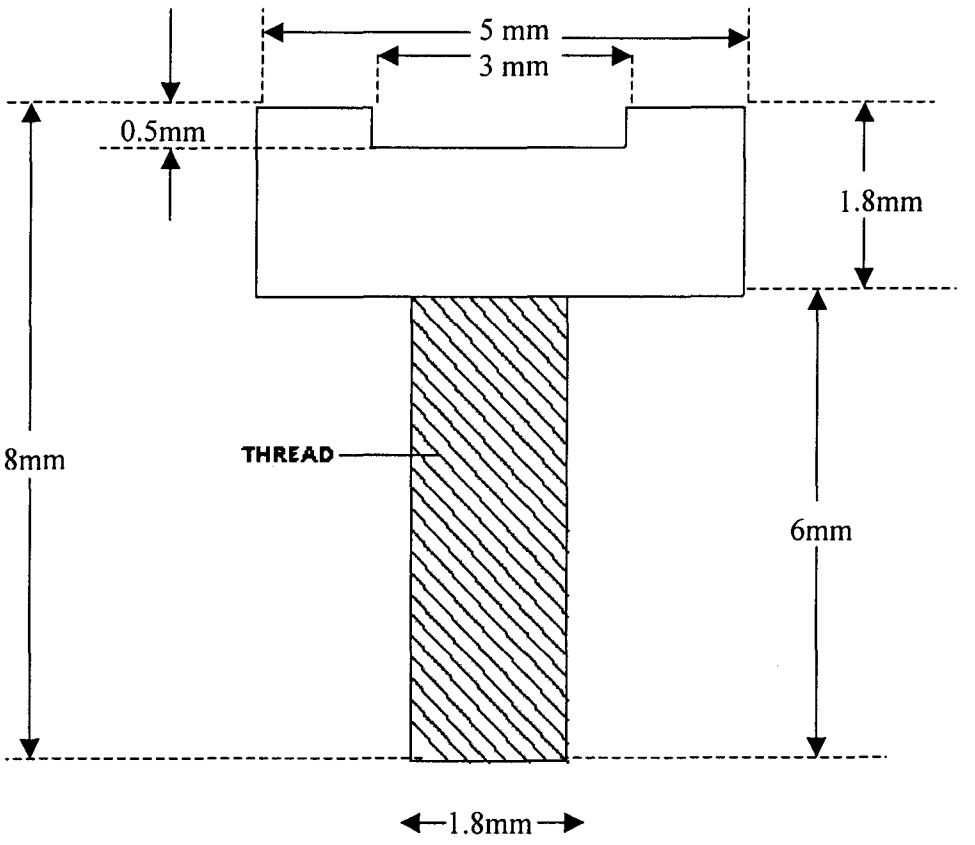


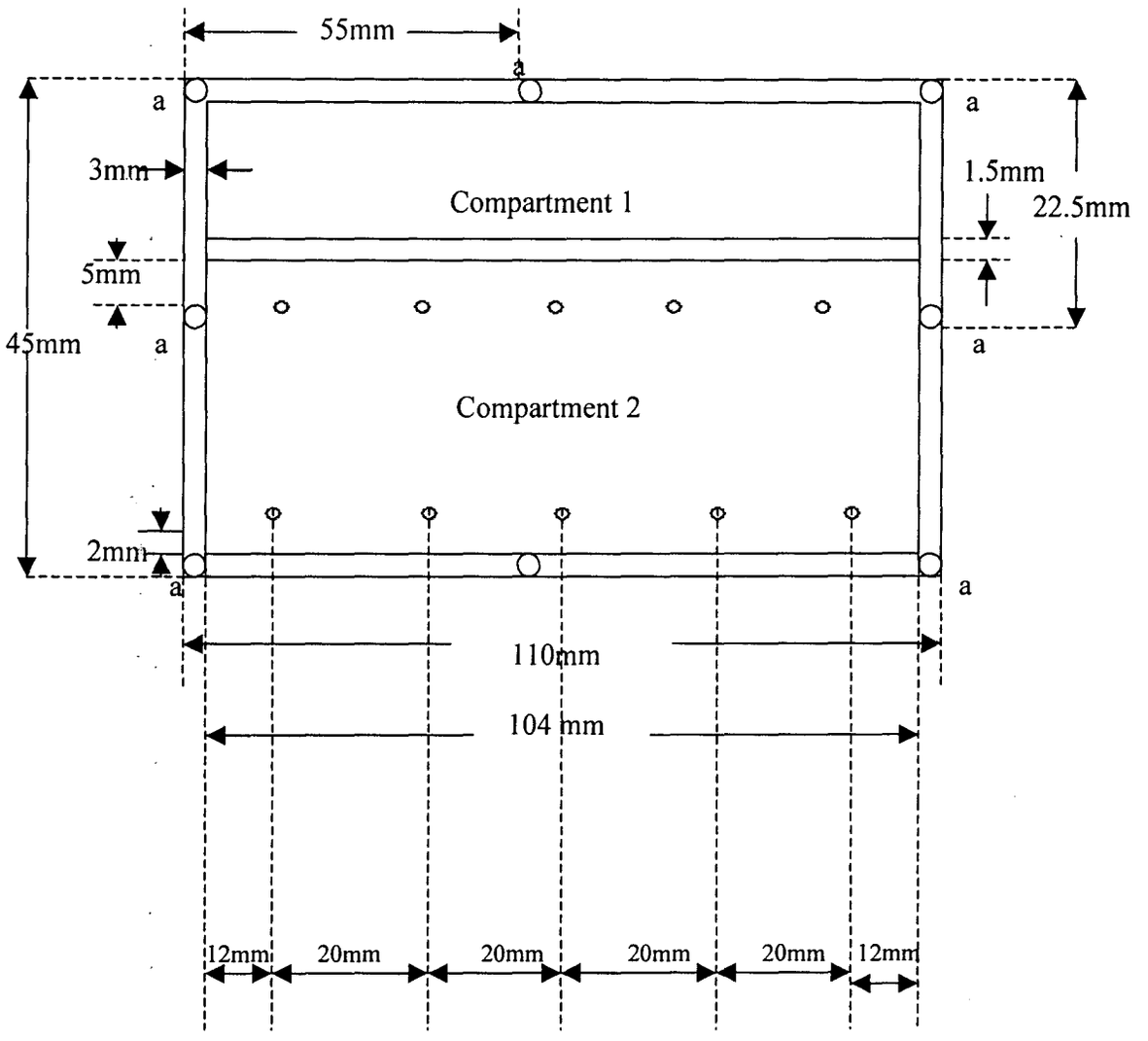
Fig 5.2(b) Front view

Fig.5.2 Transistor holder

5.1.2 Amplifier chassis

Amplifier chassis and the lid to house the amplifier was milled using brass stock. The chassis was designed with two compartments, one for the bias and the other for the RF section. The main purpose of providing two compartments was to avoid leakage of the Radio Frequency signal through the bias section .All the bypass capacitors in the bypass section were soldered directly on to the chassis. Depressions of 0.5mm depth were milled in the exact locations for these capacitors for ease of soldering. Enameled copper wires (Gauge #27) were used for providing bias to the transistor. Bias was given to the amplifier from a separate bias box outside the amplifier (refer appendix for the circuit diagram and operation of the bias box).

SMA microstrip launchers from omni spectra Inc were used for input and output RF connections to minimize co-axial microstrip transition loss. Chip capacitors from American Technical ceramics Inc were used for both bypass and coupling capacitors -ATC 100B for 1000pF bypass capacitor and ATC 100A for the rest. The transistors were mounted on the holders and the drain and source leads were mounted in plane with the PCB to reduce any additional inductance added to the circuit due to the leads. The PCB was fixed to the chassis using 10 screws (Refer Fig 5.3(a)). The mechanical diagram of the chassis is shown in Fig.5.3. The photograph of the amplifier is shown in Fig 5.4.



a : 2 mm Φ and 0.25 mm deep

Fig.5.3(a) Top View Of The Amplifier Chassis

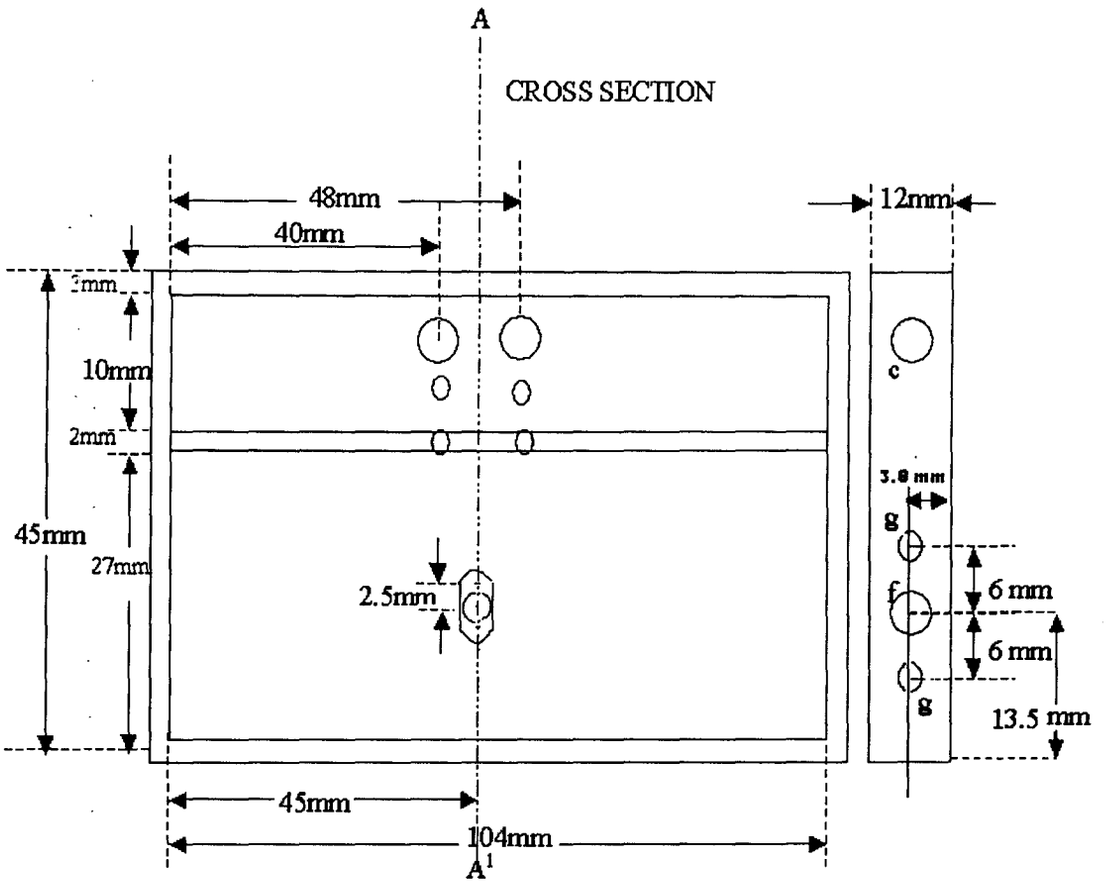


Fig.5.3(b)Top View Of The Amplifier Chassis

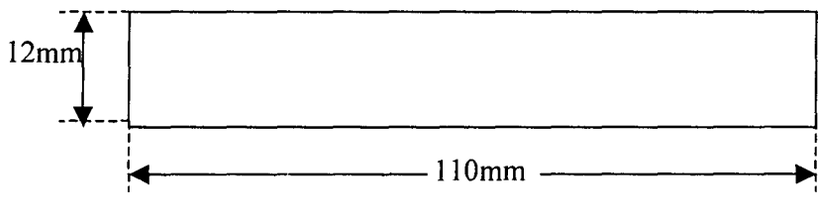
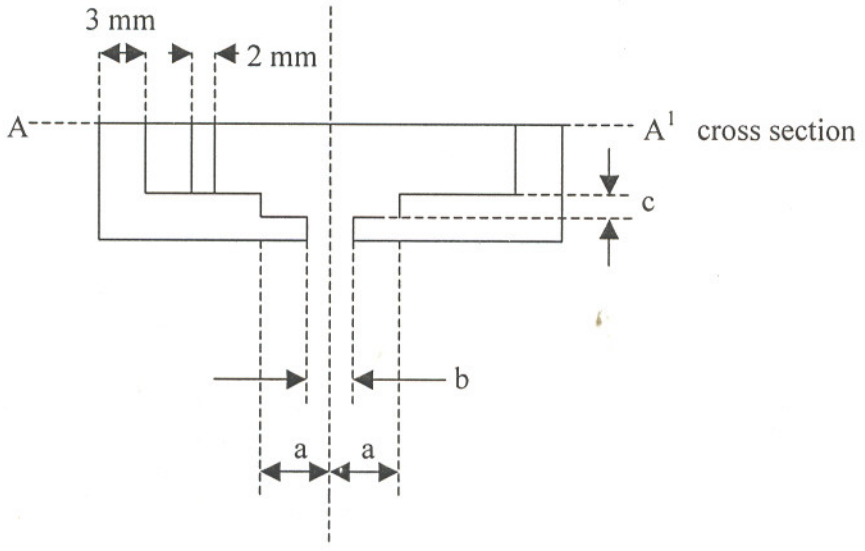


Fig.5.3(c) Front View Of The Amplifier Chassis

a: 2 mm Φ and 0.25 mm deep
b : 4 mm Φ and 0.4 mm deep
c : microtech bias connector
d : 18 mm Φ through hole
e : 8 mm Φ
f : 3 mm Φ
g : 2 mm Φ



a : 2.5 mm
b : 1.8 mm ϕ through hole
c : 1.2 mm

Fig 5.3(d) Cross Sectional View Of The Amplifier Chassis

Fig 5.3 Schematic diagram of the Amplifier chassis

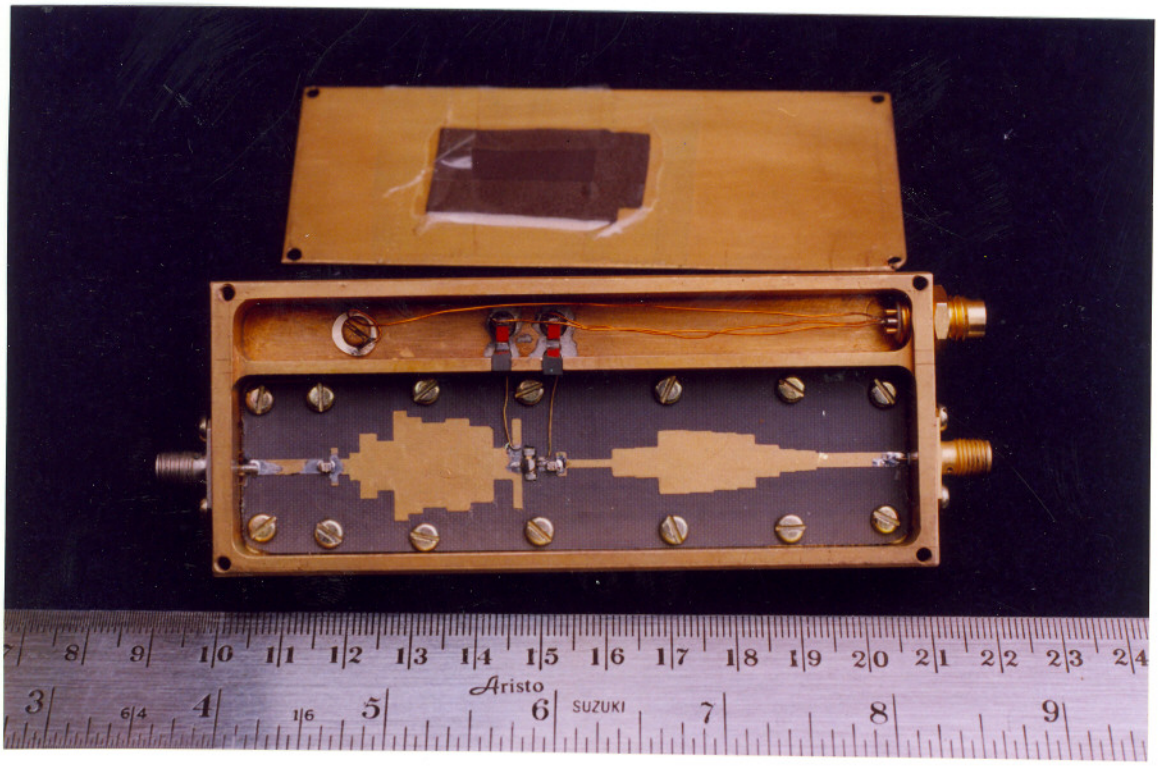


Fig 5.4 Photograph of the Amplifier

5.1.4 Amplifier assembling

LNA assembling is done as follows

1. **Placement Of Bypass Capacitors:**

NOTE: This procedure is done under the microscope with magnification 16.

The procedure followed for the placement of bypass capacitors is as follows.

a. Chassis was heated to >250 °C using the hot plate and the soldering iron.

b. Solder pullets (SN62) were placed in the depressions made in the chassis for placing the capacitors and the solder was spread using SuperSafe flux.

c. Capacitors were placed in their respective positions by inspecting under the microscope.

d. Chassis was removed from the metal plate and allowed to cool.

e. Capacitors were individually cleaned using toothpick, cotton and Isopropyl Alcohol (IPA).

f. chassis was immersed in Alcohol bath and kept for ultrasonic cleaning for about 5 minutes.

g. Chassis was removed and allowed to dry.

2. **Placement of resistors between by–pass capacitors:**

NOTE: This procedure is done under the microscope with magnification 16.

a. Two 50Ω resistors are soldered between 1000 pf and 10 pf capacitors.

b. Resistors between 10 pf and 1.2 pf were soldered only on top of 10 pf and the other side was soldered later while soldering the bias $\lambda / 4$ wires.

c. This entire operation was done under the microscope.

d. Extra flux was cleaned using IPA, cotton and toothpick.

3. Connection of bias connector:

a. Gauge No.27 Enameled Copper wires cut to right length plus 1 cm were used between the bias connector and top of 1000 pf by-pass capacitors.

b. The wires were routed properly to run in the channels between the 1000-pf capacitors and the chassis wall.

c. The length of the wire supplying the bias to the gate was maintained at the quarter of the wavelength at 6.7 GHz.

d. For ground connection, a ground tag was used on end of the Copper wire and screwed onto the chassis.

e. Extra flux was cleaned using IPA, cotton and toothpick.

4. Bias checking:

a. Bias cable was connected to the connector.

b. We set Vd1 (drain voltage knob)=3V in the bias box and adjusted the Id (drain current knob) to approximately 10 mA.

c. The bias box was put on and checked for the bias on top of the 1.2 pf capacitor. (V_d =2V,V_g=0.4V)

5. Soldering of the transistor to holder:

a. The working table was cleaned thoroughly.

b. The hot iron plate surface was cleaned thoroughly with sand paper and the setting was arranged for heating.

c. The holder was screwed onto the threaded holder hole on the hot plate.

d. The grounding of Aluminium plate on table, soldering iron, hot plate, holder, etc

were checked.

e. The well-grounded wristband was worn to remove static charges from our body.

f. The hot iron plate was heated to 250°C.

g. Some solder pellets were placed on the holder to solder leads. SuperSafe flux was used for even spreading. Care was taken not to put any solder/flux in the channel between source leads.

h. When the solder melted, transistor was placed on the holder using grounded tweezers.

i. It was allowed to cool on the hot plate itself.

j. It was removed carefully from the hot plate using tweezers/nose pliers holding the threaded portion of the holder lightly.

6. Card sizing:

a. The card is sized to exact dimensions.

b. Holes were filed for transistor holder using small flat file. Care is taken not to do any filing near the transmission lines. It was checked intermittently that the holder fits exactly.

c. The sharp edges of the first transmission matching line, input 50Ω line and 50Ω output line were chambered.

7. Card placing:

a. The transistor holder with transistor were placed in their respective places and the card was slid onto the chassis.

b. Using M 2.5 screws of the right length the card was screwed down.

8. Connector soldering:

a. Two radial connectors with 3mm long Teflon for both input and output were connected. M 2.5 screws were used to fix them. The center pins were soldered onto input and output 50Ω lines with minimum solder and flux. Extra flux was cleaned using IPA, Cotton and toothpick.

9. Coupling capacitor soldering:

a. The coupling capacitors were placed exactly in center of lines.

b. Both sides were soldered with minimum solder and flux.

c. Extra flux was cleaned using IPA, Cotton and toothpick.

10. Bias wire and transistor lead soldering:

a. Solder one end of the Gauge 30 Gold plated Copper wire on top of the 1.2pf bypass capacitor.

b. The transistor holder was tightened with nut and washer at the bottom of the chassis using right spanner.

c. The other end of the bias wire near the gate/drain leads were soldered using solder and flux at the low impedance portion of the input matching section.

d. Extra flux was cleaned using IPA, Cotton and toothpick.

11. Cleaning:

a. It was washed with alcohol.

b. It was allowed to dry and checked for performance.

5.2 Experimental setup for the measurement of Gain And Return Loss of the amplifier

Experimental setup for the measurement of Gain and Return loss of the LNA is as shown in figure 5.5. It consists of a scalar network analyzer (HP 8757D), a synthesized sweeper (HP 83752A), directional bridge and a detector.

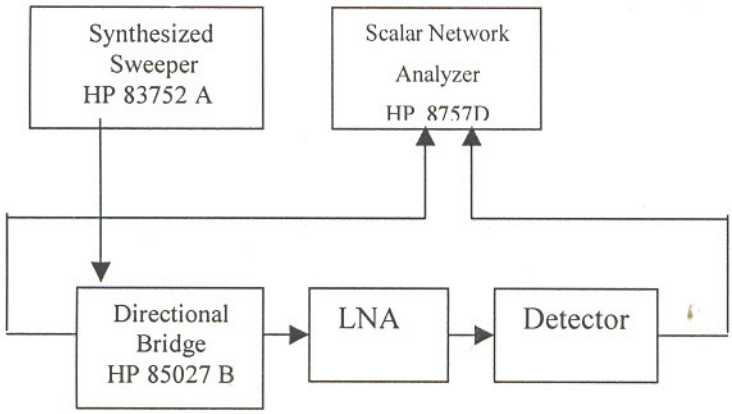


Fig 5.5 Experimental setup for Gain and Return loss

Initially the setup was made without connecting the LNA. The frequency range is set between 3GHz to 9 GHz. The power level was set to -30dBm. The system was calibrated to remove the instrumental effects. Then the LNA is connected in between the detector and the auto tester in the setup,the photograph of the setup is shown in Fig 5.6. The Gain and return loss of the amplifier are measured and the plots obtained are shown in Fig5.7

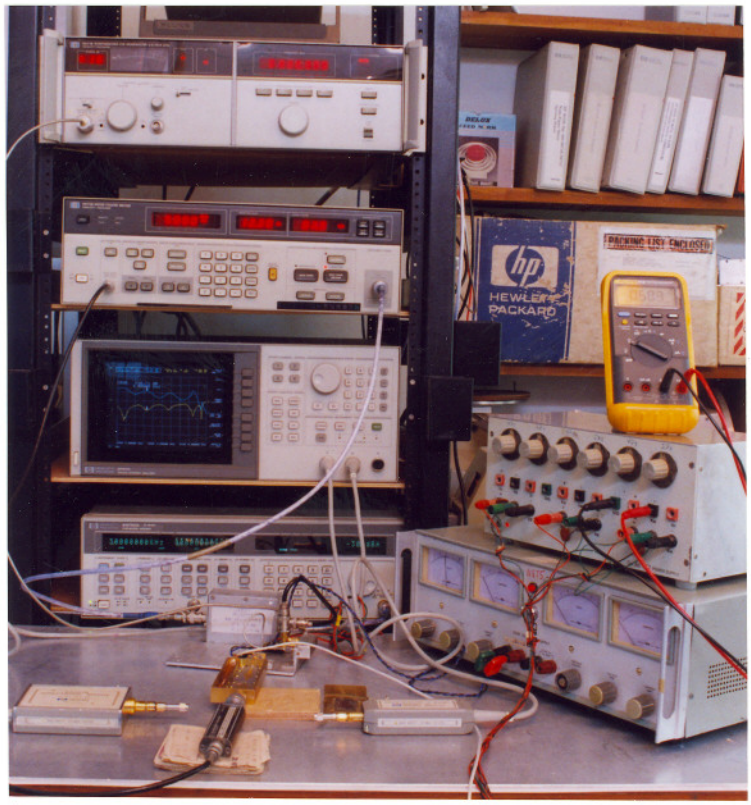


Fig 5.6 Photograph of the Experimental Setup

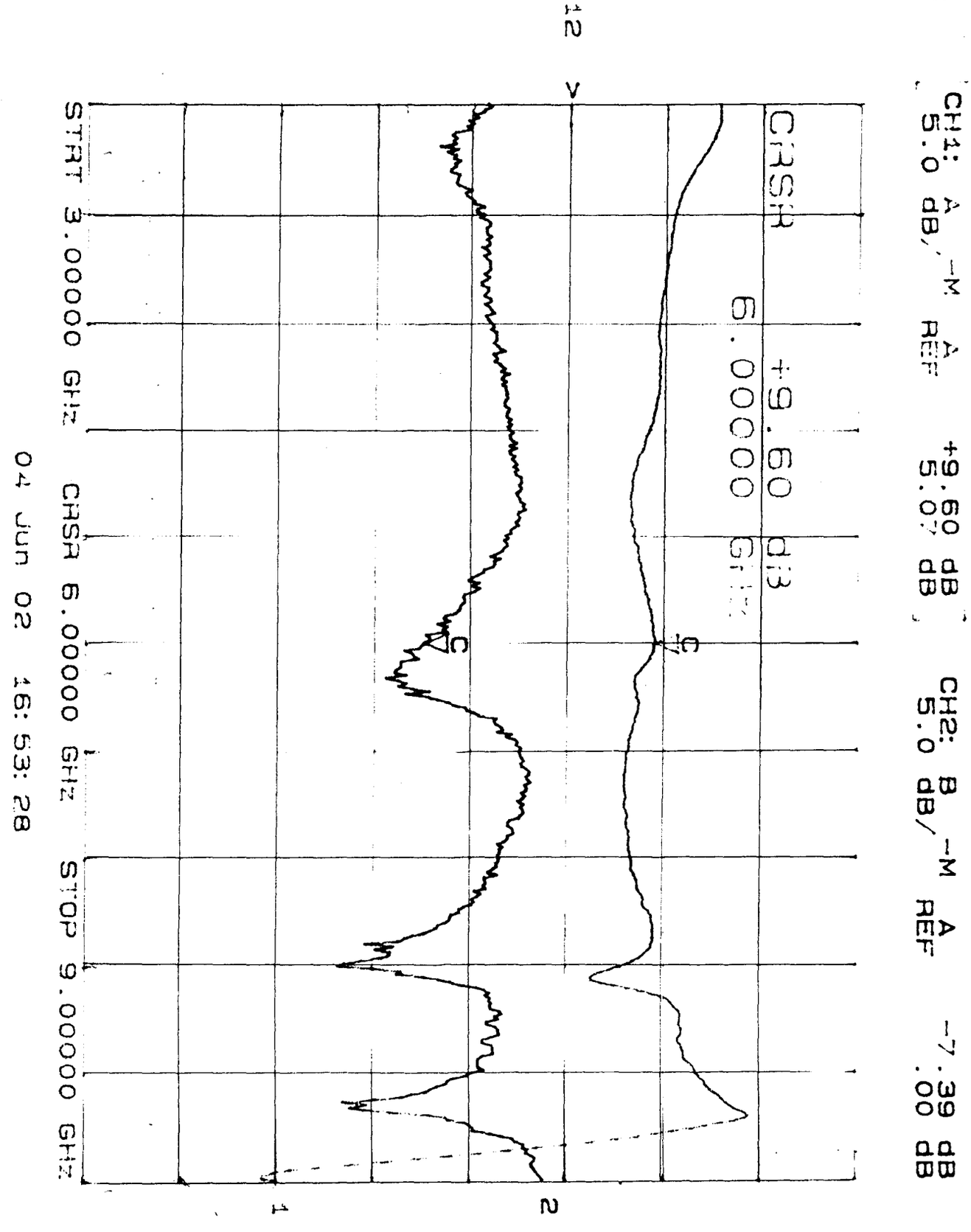


Fig 5.7 The measured gain and return loss of the amplifier

5.4 Experimental setup for the measurement of Noise figure of the amplifier

Experimental setup for the measurement of Noise Figure of the LNA is as given in figure 5.8. It consists of a Noise Figure Meter (HP 8970B) a Synthesized Sweeper.

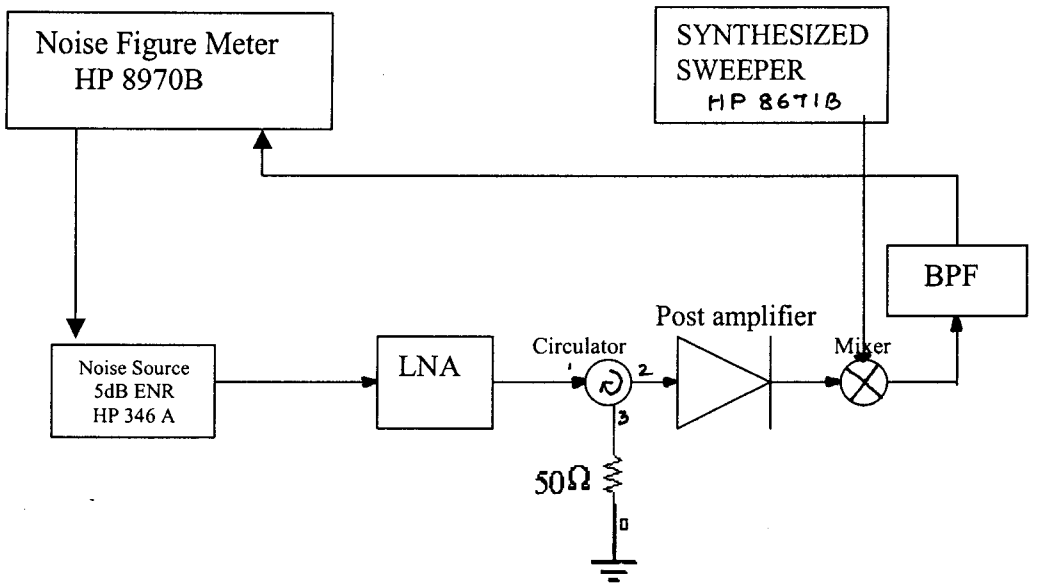


Fig 5.8 Experimental setup for Noise Figure

The measurement was carried out by down converting the high frequency to low frequency. This was done using a mixer. The setup consisting of the mixer and a band pass filter was included in the setup while calibrating the instrument. After the calibration, the LNA was incorporated in the setup to measure the noise figure and gain .The gain and noise figure of the amplifier is shown in figure 5.9

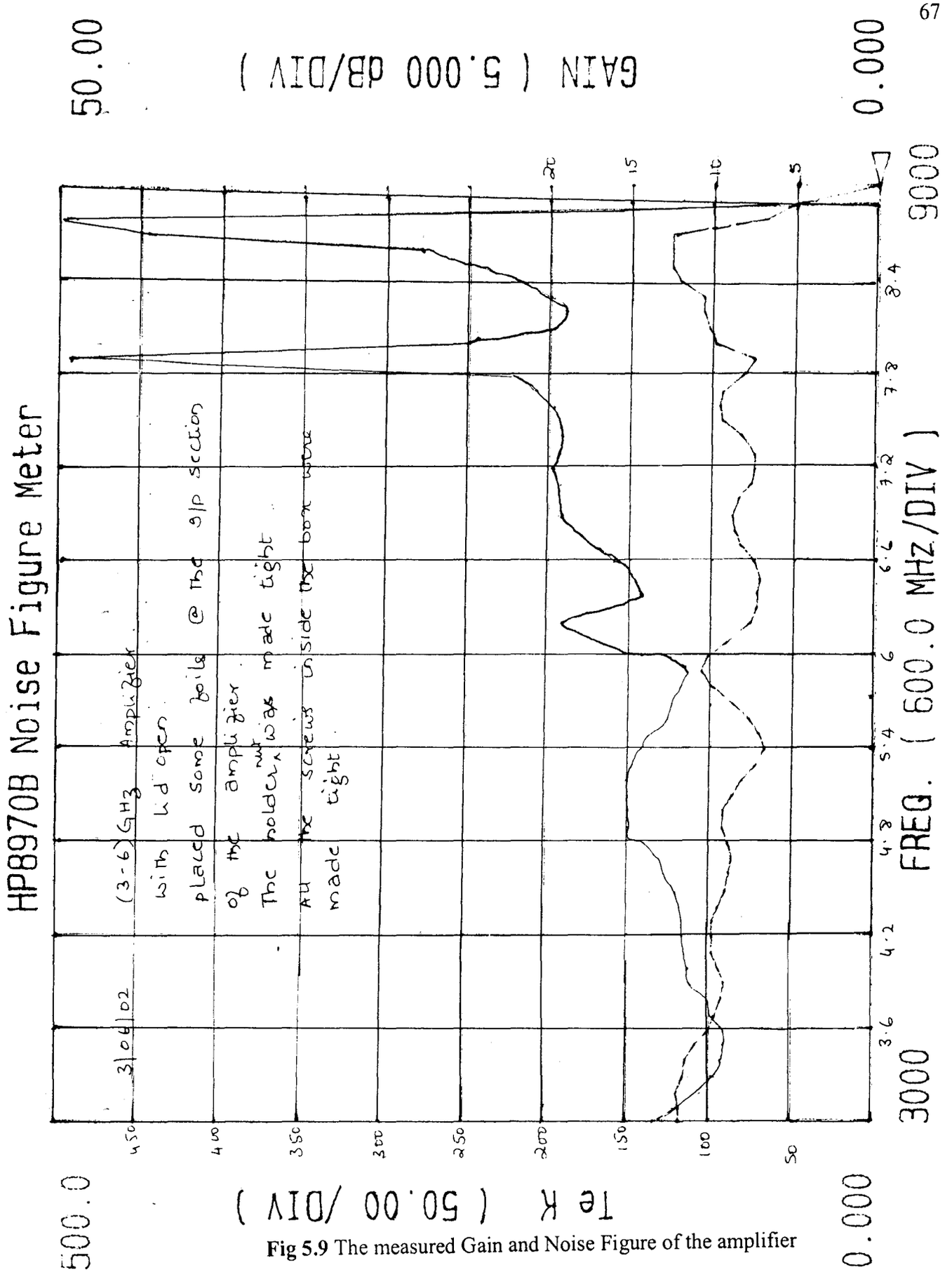


Fig 5.9 The measured Gain and Noise Figure of the amplifier

6. CONCLUSIONS AND SCOPE FOR FURTHER WORK

The low noise amplifier was successfully built and tested in the laboratory. The response of the amplifier could be improved by incorporating the missing inductances at the Gate and Drain leads of the transistor.

A short-circuited λ/4 transmission line has been used in the amplifier, in the bias section connecting the amplifier to the bypass capacitors. The main function of this line is to offer a high impedance to the RF line so that RF leakage into the bias section is minimum. This sort of arrangement is most effective over only narrow range of frequencies. If the leakage has to be minimized over a large range frequencies, the λ/4 transmission line should be replaced by a radial stub followed by a λ/4 transmission line.

PCB used to construct the amplifier has an εr=2.5. If a PCB having a higher εr value is used to construct the amplifier, the overall length of the amplifier. Chassis can be brought down quite substantially.

The amplifier built at present has a gain of only 10dB. So a multistage amplifier can be built to achieve larger gain.

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Edited by
Hatsuaki Fukui
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6. Microwave Transistor Amplifiers,
Guillermo Gonzalez,
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8. Appendix

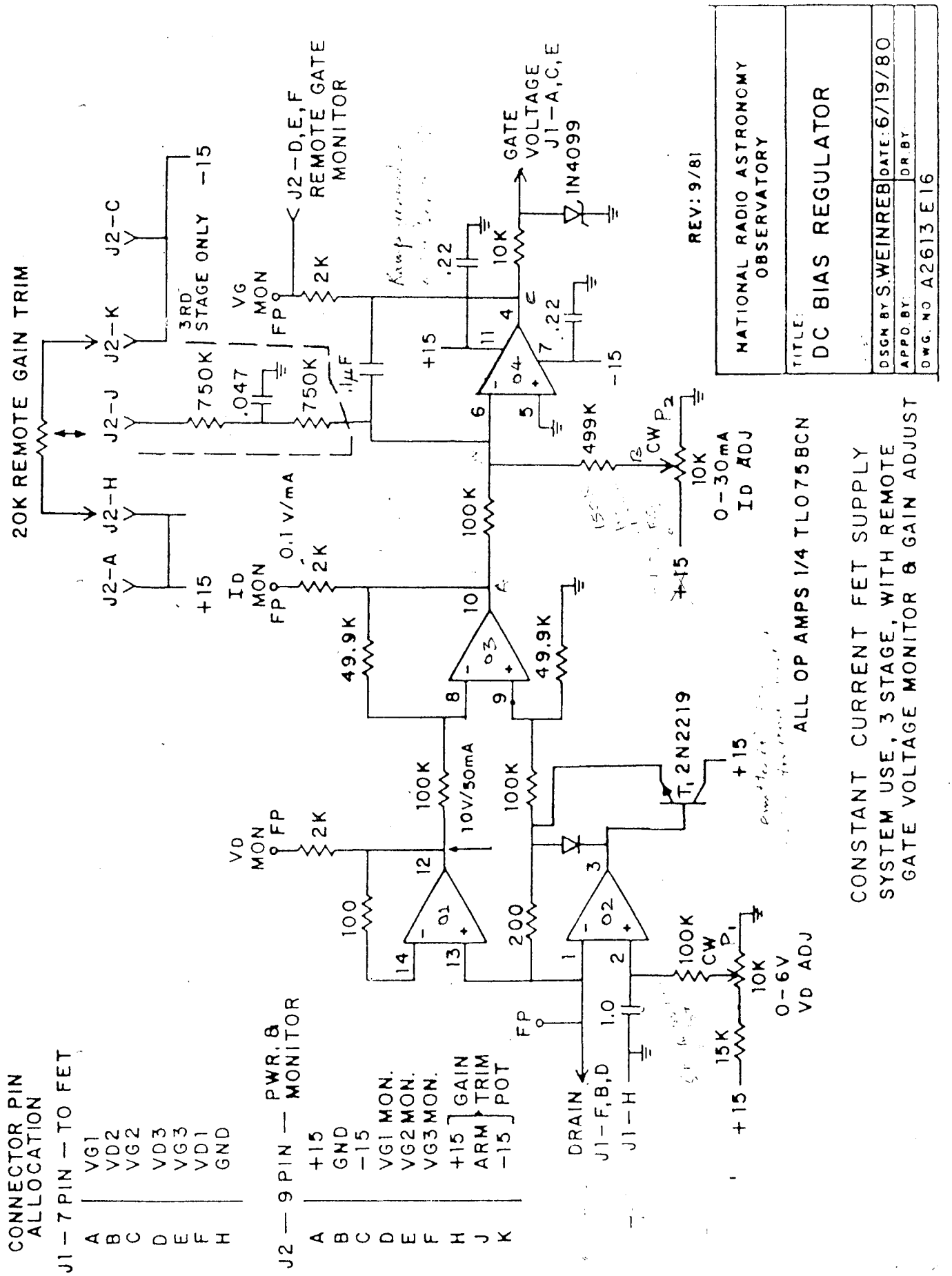
DC BIAS REGULATOR CIRCUIT OPERATION

The heart of the servo system lies in the ramp generator op amp 04(Quad TL084). Let us assume P2 is a 10K (wire wound) potentiometer. With the pot set at maximum value (with the dial at 30), Let us say that 30mA should be drawn by the FET (even though the FET will not be operated at this current, it induces that the current can be said set with the dial on the pot). Therefore –15V will be set on the inverting terminal of 04 and it ramps positively. This increases the gate voltage and the FET begins to draw more current through the transistor T1 and this current drops a voltage across the 200Ω resistor at its path. (The drain voltage is set by 02,but most of the current is taken from T1). The drop across the 200Ωis applied to the difference amplifier 03 and it produces a positive voltage at its output, proportional to the current through the GaAs FET. When this voltage reaches a value, it makes the ramp generator 04 to ramp in the opposite sense. Finally at steady state, the current charging the capacitor across 04 should be zero. This is possible only when

$$\frac{\text{Output of 03}}{100K} = \frac{\text{Setting of pot P2}}{500K}$$

$$\text{Output of 03} = \frac{15*100}{500} = 3V$$

which is equal to the drop across the 200Ω showing that 30mA is flowing through the 200Ω and hence through the GaAs FET.


NATIONAL RADIO ASTRONOMY OBSERVATORY
TITLE: DC BIAS REGULATOR
DSGN BY S.WEINREB DATE: 6/19/80
APPD BY: DR BY:
DWG. NO A2613 E16
REV: 9/81
CONSTANT CURRENT FET SUPPLY
SYSTEM USE, 3 STAGE, WITH REMOTE
GATE VOLTAGE MONITOR & GAIN ADJUST
ALL OP AMPS 1/4 TL074BCN
20K REMOTE GAIN TRIM
J2-A J2-H J2-J J2-K J2-C
+15
3RD STAGE ONLY -15
750K
.047
750K
.1μF
VG MON FP
2K
J2-D,E,F REMOTE GATE MONITOR
+15
.22
10K
GATE VOLTAGE J1-A,C,E
1N4099
.22
-15
499K
CW P2
10K
0-30mA ID ADJ
ID MON FP
0.1 V/mA
2K
100K
49.9K
49.9K
VD MON FP
2K
100K
10V/50mA
100K
T1 2N2219
+15
100
200
100K
CW P1
10K
0-6V VD ADJ
15K
+15
DRAIN J1-F,B,D
1.0
J1-H
FP
CONNECTOR PIN ALLOCATION
J1 — 7 PIN — TO FET
A VG1
B VD2
C VG2
D VD3
E VG3
F VD1
H GND
J2 — 9 PIN — PWR. & MONITOR
A +15
B GND
C -15
D VG1 MON.
E VG2 MON.
F VG3 MON.
H +15 GAIN
J ARM TRIM
K -15 POT

Appendix I

FHC40LG
Low Noise HEMT

T3

ABSOLUTE MAXIMUM RATING (Ambient Temperature Ta=25°C)

Item	Symbol	Condition	Rating	Unit
Drain-Source Voltage	V_{DS}		3.5	V
Gate-Source Voltage	V_{GS}		-3.0	V
Total Power Dissipation	P_{tot}	Note	290	mW
Storage Temperature	T_{stg}		-65 to +175	°C
Channel Temperature	T_{ch}		175	°C

Note: Mounted on Al_2O_3 board (30 x 30 x 0.65mm)

Fujitsu recommends the following conditions for the reliable operation of GaAs FETs:
1. The drain-source operating voltage (V_{DS}) should not exceed 2 volts.
2. The forward and reverse gate currents should not exceed 0.2 and -0.1 mA respectively with gate resistance of 4000Ω.

ELECTRICAL CHARACTERISTICS (Ambient Temperature Ta=25°C)

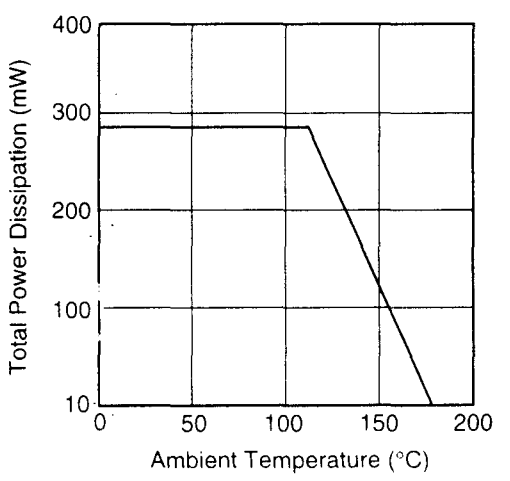
Item	Symbol	Condition	Limit			Unit
			Min.	Typ.	Max.	
Saturated Drain Current	I_{DSS}	V_{DS} = 2V, V_{GS} =0V	10	40	85	mA
Transconductance	g_m	V_{DS} = 2V, I_{DS} =10mA	45	65	-	mS
Pinch-off Voltage	V_p	V_{DS} = 2V, I_{DS} =1mA	-0.1	-1.0	-2.0	V
Gate Source Breakdown Voltage	V_{GSO}	I_{GS} = -10μA	-3.0	-	-	V
Noise Figure	NF	V_{DS} = 2V, I_{DS} = 10mA, f = 4GHz	-	0.30	0.40	dB
Associated Gain	G_{as}		14.0	15.5	-	dB

AVAILABLE CASE STYLES: LG

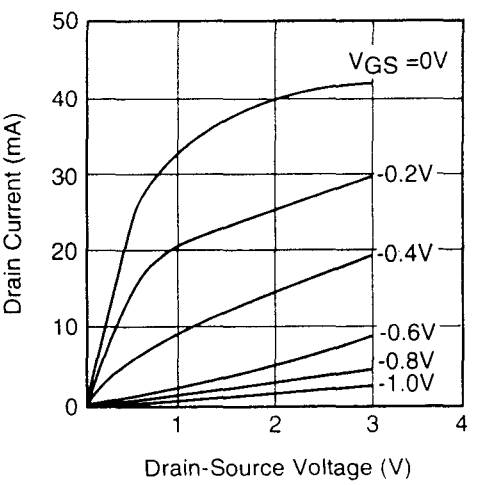
Note: RF parameters for LG devices are measured on a sample basis as follows:

Lot qty.			Sample qty.	Accept/Reject
1200	or	less	125	(0,1)
1201	to	3200	200	(0,1)
3201	to	10000	315	(1,2)
10001	or	over	500	(1,2)

POWER DERATING CURVE

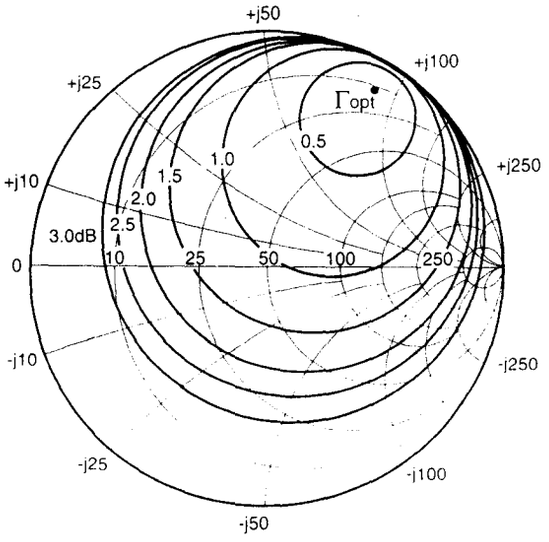


DRAIN CURRENT vs. DRAIN-SOURCE VOLTAGE



FUJITSU

TYPICAL NOISE FIGURE CIRCLE



f=4GHz
V_{DS}=2V
I_{DS}=10mA

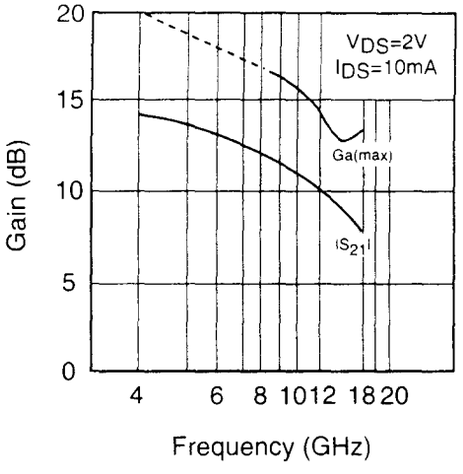
Γopt=0.87∠57°
Rn/50=0.18
NFmin=0.30dB

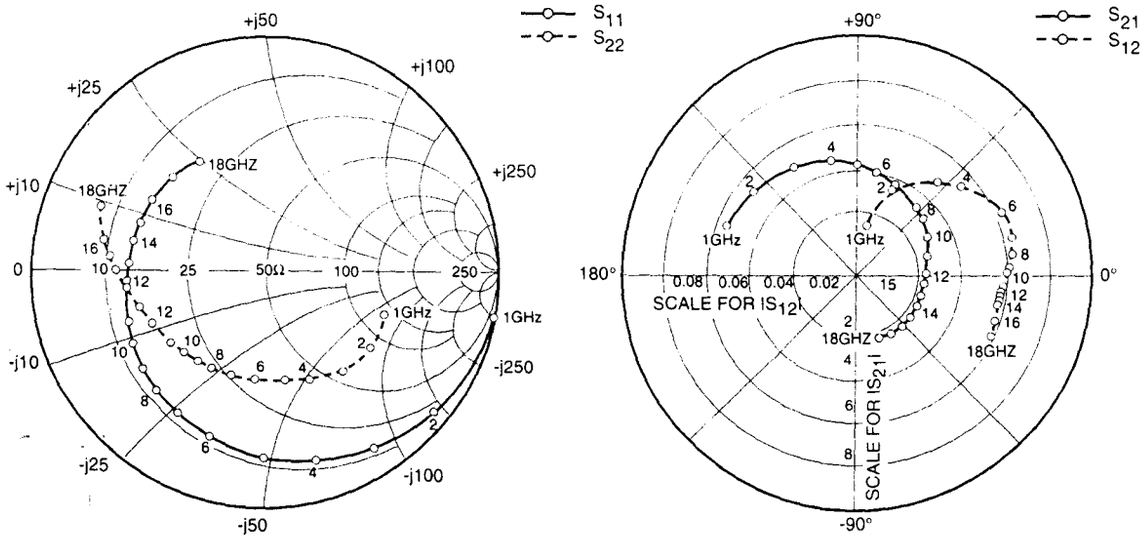
NOISE PARAMETERS

V_{DS}=2V, I_{DS}=10MA

Freq. (GHz)	Γopt (MAG)	Γopt (ANG)	NFmin (dB)	Rn/50
2	0.86	31.0	0.28	0.19
4	0.87	57.0	0.30	0.18
6	0.86	83.0	0.34	0.13
8	0.81	108.0	0.39	0.09
10	0.74	132.0	0.47	0.05
12	0.63	156.0	0.55	0.03
14	0.49	179.0	0.67	0.04
16	0.33	-158.0	0.81	0.07
18	0.13	-136.0	1.00	0.11

Ga(max) AND $|S_{21}|$ vs. FREQUENCY

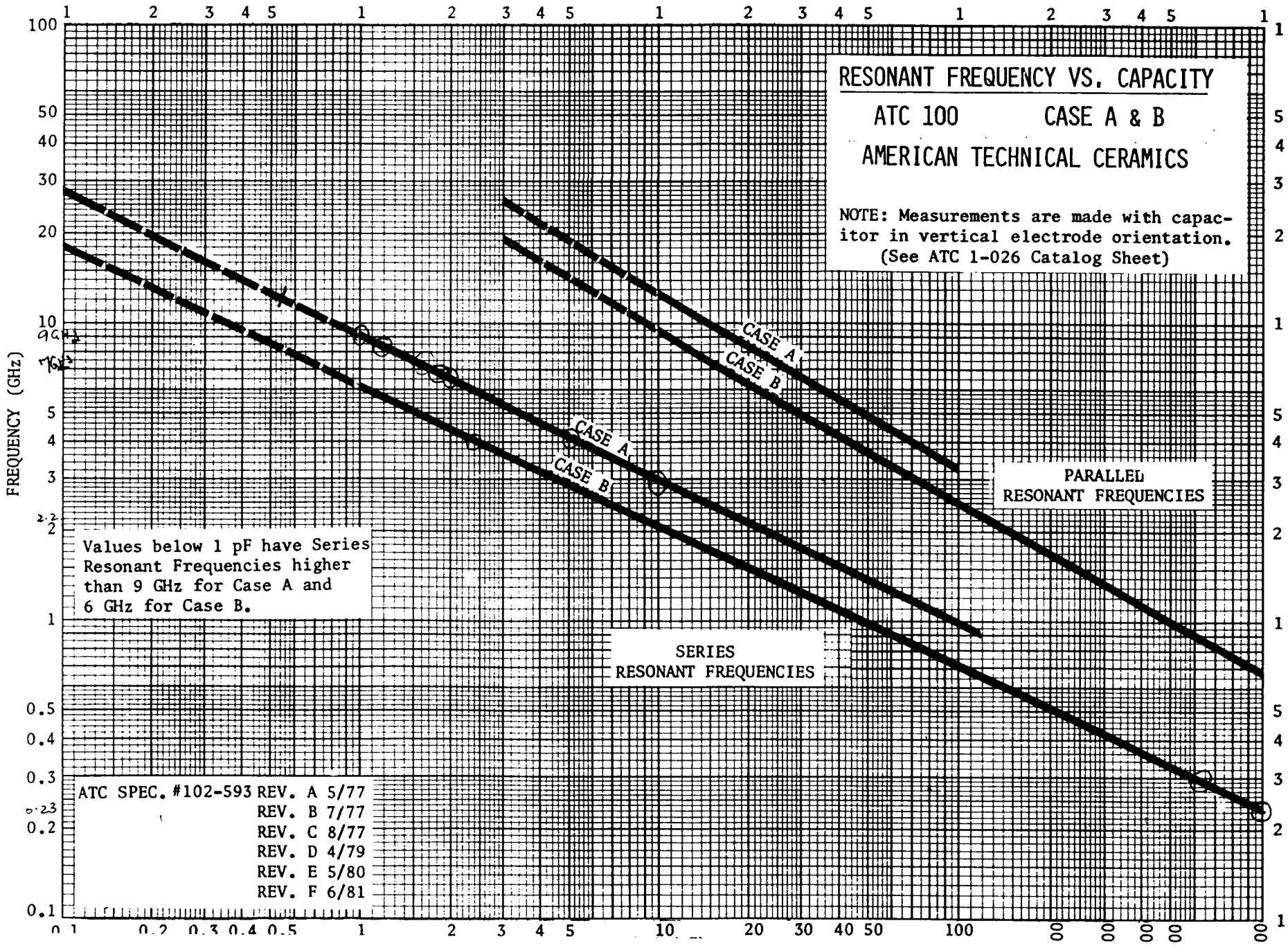




S-PARAMETERS

V_{DS} = 2V, I_{DS} = 10mA

FREQUENCY	S11		S21		S12		S22	
(GHZ)	MAG	ANG	MAG	ANG	MAG	ANG	MAG	ANG
1.0	0.980	-20.6	5.620	159.7	0.017	75.8	0.541	-17.8
2.0	0.942	-40.7	5.401	140.7	0.033	61.6	0.523	-35.0
3.0	0.887	-59.4	5.051	122.6	0.045	49.5	0.501	-51.2
4.0	0.838	-76.9	4.685	105.8	0.054	38.5	0.480	-66.6
5.0	0.786	-93.2	4.334	89.9	0.060	28.5	0.461	-81.3
6.0	0.742	-108.3	3.984	74.9	0.063	20.2	0.448	-95.4
7.0	0.705	-122.1	3.654	60.6	0.063	12.9	0.449	-108.9
8.0	0.672	-133.7	3.340	47.6	0.063	7.2	0.463	-120.3
9.0	0.651	-143.9	3.110	35.8	0.062	3.2	0.481	-130.1
10.0	0.633	-153.9	2.954	23.7	0.061	-0.2	0.498	-138.8
11.0	0.611	-164.1	2.786	11.8	0.059	-2.9	0.513	-147.6
12.0	0.595	-174.8	2.641	0.0	0.058	-5.1	0.535	-157.0
13.0	0.588	176.0	2.518	-11.6	0.057	-6.7	0.562	-165.3
14.0	0.579	167.6	2.412	-23.0	0.057	-7.9	0.597	-172.8
15.0	0.569	159.3	2.342	-34.6	0.057	-10.1	0.634	-179.7
16.0	0.555	150.5	2.290	-46.6	0.058	-12.9	0.667	173.6
17.0	0.536	140.3	2.272	-59.4	0.059	-17.0	0.697	166.4
18.0	0.525	129.9	2.233	-72.6	0.060	-22.4	0.727	158.8


RESONANT FREQUENCY VS. CAPACITY
ATC 100 CASE A & B
AMERICAN TECHNICAL CERAMICS
NOTE: Measurements are made with capacitor in vertical electrode orientation. (See ATC 1-026 Catalog Sheet)
FREQUENCY (GHz)
CASE A
CASE B
CASE A
CASE B
PARALLEL RESONANT FREQUENCIES
SERIES RESONANT FREQUENCIES
Values below 1 pF have Series Resonant Frequencies higher than 9 GHz for Case A and 6 GHz for Case B.
ATC SPEC. #102-593 REV. A 5/77
REV. B 7/77
REV. C 8/77
REV. D 4/79
REV. E 5/80
REV. F 6/81

Values of the function $\Phi(Z,A)$ for various values of $20 \log_{10}(\cosh A)$

$\Phi(Z,A)$									
	$20 \log_{10}(\cosh A)$								
Z	0	5	10	15	20	25	30	35	40
0.00	0.000000	0.000000	0.000000	0.000000	0.000000	0.000000	0.000000	0.000000	0.000000
0.05	0.025000	0.029593	0.036848	0.048140	0.065590	0.092539	0.134313	0.199460	0.301772
0.10	0.050000	0.059101	0.073629	0.096137	0.130902	0.184564	0.267698	0.397268	0.600625
0.15	0.075000	0.088681	0.110276	0.143848	0.195661	0.275567	0.399242	0.591802	0.893701
0.20	0.100000	0.118128	0.146721	0.191132	0.259597	0.365055	0.528062	0.781511	1.178306
0.25	0.125000	0.147479	0.182899	0.237850	0.322448	0.452552	0.653321	0.964936	1.451930
0.30	0.150000	0.176708	0.218746	0.283869	0.383962	0.537610	0.774237	1.140744	1.712272
0.35	0.175000	0.205794	0.254197	0.329059	0.443899	0.619809	0.890101	1.307751	1.957437
0.40	0.200000	0.234711	0.289191	0.373296	0.502035	0.698767	1.000282	1.464942	2.185803
0.45	0.225000	0.263438	0.323667	0.416460	0.558163	0.774142	1.104238	1.611187	2.396134
0.50	0.250000	0.291950	0.357568	0.458441	0.612094	0.845635	1.201523	1.746753	2.587582
0.55	0.275000	0.320226	0.390837	0.499134	0.663658	0.912994	1.291792	1.870306	2.659684
0.60	0.300000	0.3482442	0.423420	0.538444	0.712709	0.976019	1.374800	1.981918	2.912359
0.65	0.325000	0. 375982	0.455266	0.576284	0.759120	1.034555	1.450409	2.081555	3.015886
0.70	0.350000	0.403418	0.486328	0.612574	0.802790	1.088504	1.518582	2.169376	3.160875
0.75	0.375000	0.430533	0.516559	0.647248	0.843641	1.137814	1.579377	2.245710	3.258228
0.80	0.400000	0.457305	0.545918	0.680245	0.881619	1.182484	1.632947	2.311049	3.339098
0.85	0.425000	0.483716	0.574365	0.711518	0.916692	1.222564	1.679531	2.366019	3.404835
0.90	0.450000	0.509746	0.601865	0.741027	0.948855	1.258145	1.719443	2.411361	3.456938
0.95	0.475000	0.535377	0.628386	0.768745	0.978123	1.289363	1.753065	2.447905	3.497000
1.00	0.500000	0.560591	0.653899	0.794653	1.004533	1.316391	1.780835	2.476547	3.526658