PROJECT REPORT

2000-2001

COARSE FREQUENCY SETTING MODULE FOR 2000 TO 8000 MHz YIG TUNED OSCILLATOR

CARRIED OUT AT

RAMAN RESEARCH INSTITUTE

RADIO ASTRONOMY LAB

BANGALORE

SUBMITTED IN PARTIAL FULFILLMENT OF

Award of Degree

of

BACHELOR OF ENGINEERING

in

ELECTRICAL AND ELECTRONICS

BY THE BANGALORE UNIVERSITY, BANGALORE

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BANGALORE –560 054

CERTIFICATE

This is to certify that the project work entitled

" COARSE FREQUENCY SETTING MODULE FOR 2000 TO 8000 MHz YIG TUNED OSCILLATOR "

has been successfully carried out by

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in partial fulfillment of the dissertation project for the award of Bachelor of Engineering Degree in

Electrical and Electronics Engineering by the Bangalore University during the academic year 2000-2001

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Gowrugolla Gnana Pradeep

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COARSE FREQUENCY SETTING

MODULE

FOR

2000-8000 MHz

YIG TUNED OSCILLATOR

CONTENTS

Synopsis:

COARSE FREQUENCY SETTING MODULE FOR 2000-8000 MHz YIG TUNED OSCILLATOR

Introduction:

Frequency synthesizers and local oscillators are very important sub-systems in many sensitive radio and microwave frequency systems. Frequency synthesis is "the generation of a frequency or set of frequencies, which are exact multiples of reference frequency".

These frequency synthesizers and stable local oscillators are widely used in applications such as communication transmitters and receivers, where stability of the carrier is crucial. They also find use in "high sensitive-low noise" Radio Astronomy receiver systems as local oscillators to down convert incoming readiation to an intermediate frequency for further processing. YIG oscillators (Yttrium Iron Garnet) is commonly used in microwave receivers and spectrum analyzers.

Design

Our project aims at designing a module to set the frequency of a microwave oscillator, that produces high frequency waves in the range of (2-8) GHz band. The main objective of our project is:

The basic oscillator is a current controlled device. Setting the frequency with thumbwheel or PC, generates a constant current, to set the oscillator coarse frequency. The oscillator normally phase locked to a stable reference, is used in radio receivers as stable local oscillator signal for down converting the input frequency to an intermediate frequency.

The module has a port that can be connected to the parallel port of a PC to set the frequency without using the thumbwheel.

There could be errors from circuit like offset voltages or drift , which might occur during the generation and setting of coarse frequency. A "characterization" of the module has to be done to measure these various errors and reduce the drift in the desired frequency. (Drift occurs due to change in current, temperature and/or internal drift of the oscillator)

Conclusion:

The project aims at the design, development and fabrication of a module whose current output sets the frequency of the YIG oscillator that can generate (2-8) GHz frequencies. The oscillator we use here is an YIG oscillator. The frequency setting resolution of the oscillator has been designed to be 10 MHz.

CHAPTER-I

YIG OSCILLATOR

RF and Microwave Frequency:

Radio frequency or Microwave frequency is a descriptive term used to identify the electromagnetic waves in the frequency spectrum ranging approximately from 1GHz to 30 GHz. This corresponds to wavelengths from 30cm to 1 cm. Sometimes higher frequencies extending up to 600 GHz are also called 'microwaves'. These waves present several interesting and unusual features not found in other portions of the electromagnetic frequency spectrum. These features make 'microwaves' uniquely suitable for several useful applications.

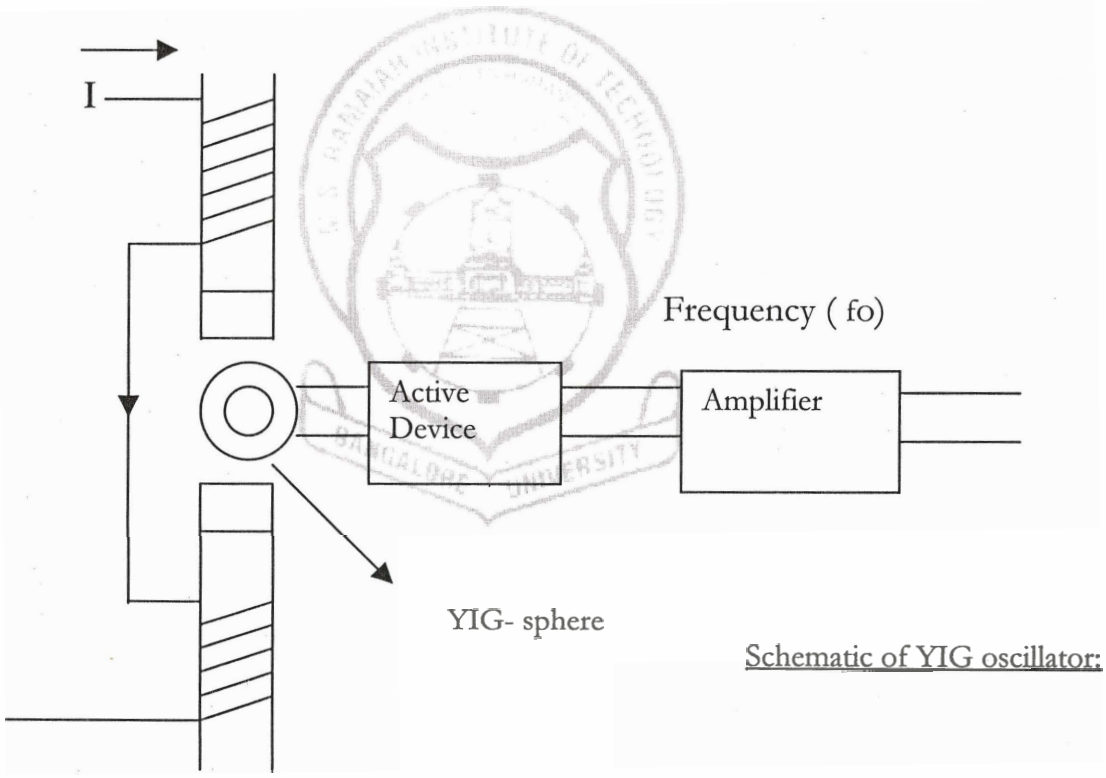
The main characteristic features of microwaves originate from the small size of wavelengths (1 cm to 30 cm) in relation to the sizes of components or devices commonly used. Since the wavelengths are small , the phase varies rapidly with distance , consequently the techniques of circuit analysis and design, of measurements and of power generation, and amplification at these frequencies are distinct from those at lower frequencies.

We are concerned only in the range of 2 GHz-8 GHz in our project. The oscillator we use has a frequency range of (2-8) GHz. The details about the Yttrium Iron Garnet (YIG) oscillator will be dealt with later in the report.

YIG OSCILLATOR:

Yittrium iron garnet ($Y_3Fe_5O_{12}$) is an insulating ferrimagnet with the lowest line width. This is the main reason for its use in radio receivers. Single crystal yttrium iron garnet (YIG) or gallium substituted YIG are magnetic insulators, which resonate at a microwave frequency when magnetized by a suitable direct magnetic field.

A unique feature of this resonance is that for a spherical YIG configuration, the resonant frequency is only related to the direct magnetic field and not to its dimensions. The basic ferromagnetic resonance phenomenon can be explained in terms of spinning electrons which create a net magnetic moment in each molecule of a YIG crystal. This electron precession may be used to couple two orthogonal circuits at a microwave signal frequency equal to that precession. This phenomenon suggests that voltage controlled tunable microwave filters using YIG resonators may be constructed .



Schematic of YIG oscillator:

Basic Working of the YIG Oscillator:

1. The crystal sphere is tuned by placing it in the air gap in between the electromagnets.
2. The crystal is placed in between the two electromagnets.
3. Current is passed through the magnets.
4. This current creates a magnetic field around the crystal.
5. The crystal gets energized and begins to resonate
6. This is principle of the working of the YIG Oscillator.

Hysterisis, Temperature,Linearity and Tuning Speed:

The YIG resonator depends on the direct magnetic field, hysteresis effects, tuning speed and temperature characteristics.

The area of the pole pieces is kept large compared to the cross sectional area of the YIG resonator to ensure that the resonator is magnetized by a uniform magnetic field. Parallelism of the pole pieces is also important. The choice of a re-entrant magnetic circuit shields the resonator from external stray magnetic fields.

The change in temperature changes the resonant frequency of the resonator. A YIG heater is to be used if the temperature of the resonator is to be maintained constant to get a stable frequency.

Gap dimension of the electromagnet should also be constant with ambient temperature.

- Eddy currents maybe minimized by increasing the resistivity of the current paths by-using high resistivity steels for the YIG housing and steel laminations for the core of the electromagnet.

In order to have a linear relationship between the coil current and the direct magnetic field in the gap between the pole pieces of the electromagnet it is necessary to ensure that the shell and the pole pieces do not exhibit saturation effects at the value of the current corresponding to the highest operating frequency of the YIG resonator.

' The YIG oscillator is therefore a current controlled oscillator. If the input current to the terminals of the oscillator is changed then correspondingly the frequency output of the oscillator also changes. This is the main function of the module being made by us in our

project. We are controlling the current input to the oscillator thereby setting the frequency of the oscillator'.

YIG Specifications:

Specifications	AV7236
1. Frequency Range Min	2-8 GHz
2. Power Output into 50 ohm Load, min at 25 C	20 mW/+13 dBm
3. Power Output Variation vs. Frequency, Max	6.0 dB
4. Operating Case Temperature Range	0 to 65 C
5. Frequency Drift over Operating Temp, max	1.5 MHz
6. Pulling Figure (12 dB Return Loss), Typical	0.01 MHz
7. Pushing Figure +15 VDC Supply, Typical	0.1 MHz/V
-5 VDC Supply, Typical	N/A
8. Magnetic Susceptibility @ 60 Hz, Typical	70 kHz/Gauss
9. 2nd Harmonic @25 C, Min	-12 dBc
10.3rd harmonic, @ 25 C, Min	–15 dBc
11. Spurious Output, Min	-60 dBc

Main Tuning Port Characteristics	
1. Sensitivity	20 ± 1 MHz/mA
2. 3 dB Bandwidth, Typical	5 kHz
3. Linearity, Typical	± 0.05%
4. Hysterisis, Typical	5 MHz
5.. Input impedance @ 1 kHz, Typical	10 Ω in series with 10 mH

FM Tuning Port Characteristics	
1. Sensitivity, Typical	310 kHz/mA
2. 3 dB Bandwidth, Typical	800 kHz
3. Deviation at 400 kHz Rate, Max	30 MHz
4. Input impedance @1 MHz, Typical	1 Ω in series with 1.7 μH

12. DC Circuit Power, Max	+15 V ±0.3 V @175 mA
13. YIG Heater Power:	
▫ Input Voltage Range	20 to 28 VDC
▫ Power @25 C, Max	1.5 Watts
▫ Power @ 0 C, Max	2.0 Watts
14. Weight, Max	10 oz
15. Case Style	A-45

Specifications :

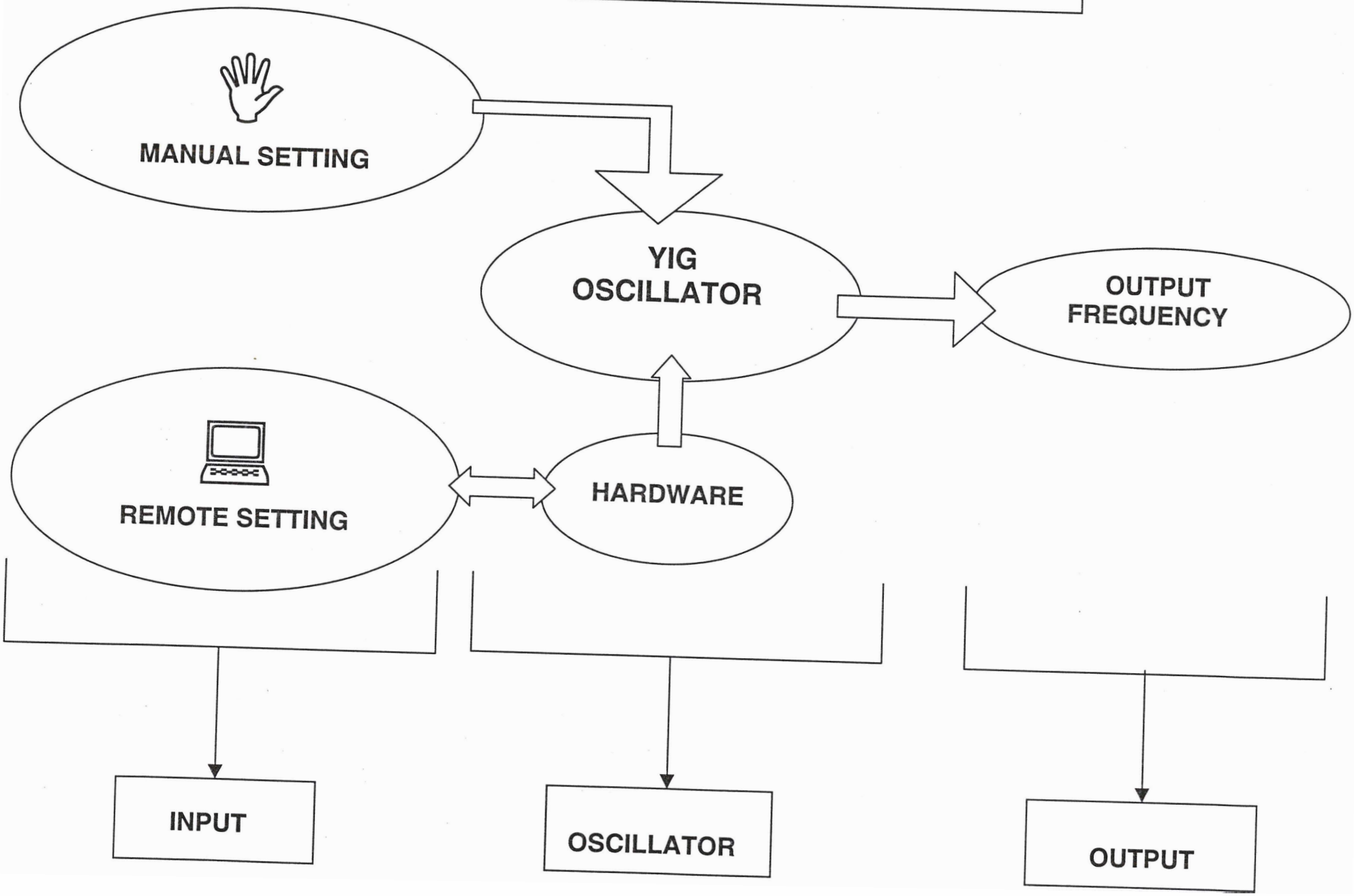
1) **Frequency Range (Min) :** The output frequency of the oscillations lie between (2-8)GHz.
2) **Power Output:** Output power expressed in mW or dBm.
3) **Operating Case temperature range:** Safe operating temperature range for the oscillator.
4) **Frequency Drift over Operating Temp., Max :** Gradual change in the frequency of the oscillations due to temperature or other changes in the circuit.
5) **Pulling Figure:** The total frequency change of an oscillation when the phase angle of the reflection co-efficient of the load impedance varies through 360^{0} , the absolute value of this reflection co-efficient being constant at 0.20.

6) **Pushing Figure**: A change in the resonant frequency of a circuit due to changes in the supply voltages.
7) **Magnetic Susceptibility**: The ratio of the magnetization of a material to the magnetic field strength; it is a tensor when these two quantities are not parallel; otherwise it is a simple number. Also known as susceptibility.
8) **Spurious Output**:: Frequencies in the output are called spurious output. Non harmonic outputs are also called spurious output.
9) **Tuning**: The process of adjusting the inductance or the capacitance or both in a tuned circuit; for e.g., in a radio, television or radar receiver or transmitter, so as to obtain optimum performance at selected frequency.
10) **Sensitivity**: The minimum input signal required to produce a specified output signal for a radio receiver or similar device.
11) **Linearity:** It is the amount by which a relationship between two quantities deviates from a straight line.
12) **Hysteresis**: An oscillator effect where in a given value of an operating parameter may result in multiple values of output power or frequency.
13) **Impedance Matching**: Maximum Power Transfer theorem i.e., only when the input impedance equals the load or output impedance, maximum power can be transferred from input to output.

CHAPTER-II

INTRODUCTION

BASIC BLOCK DIAGRAM



The basic block diagram is as shown in the previous page. There are three main parts in our project namely

1. INPUT
2. OSCILLATOR
3. OUTPUT

Considering each part of the block diagram individually :

1. **INPUT:**

   The input is of two types namely 'Manual' and 'Remote'.

   Manual input is setting the 'THUMBWHEEL'. This is like a push button and can go from values 0-9. The output of the thumbwheel is in Binary Coded Decimal (BCD) format. The BCD output of the thumbwheel has to be converted to current and then given as an input to the oscillator coarse frequency control port.

   The other input is from the PC. The output is taken through the parallel port and is given to the YIG oscillator through the same common circuit. Therefore these are the two schemes provided to set the YIG oscillator frequency.

2. **OSCILLATOR:**

   The oscillator being used is a YIG oscillator and depending on the frequency required, corresponding current is generated by the digital and analog circuit.

   The input current has to be maintained constant to get a stable output frequency.

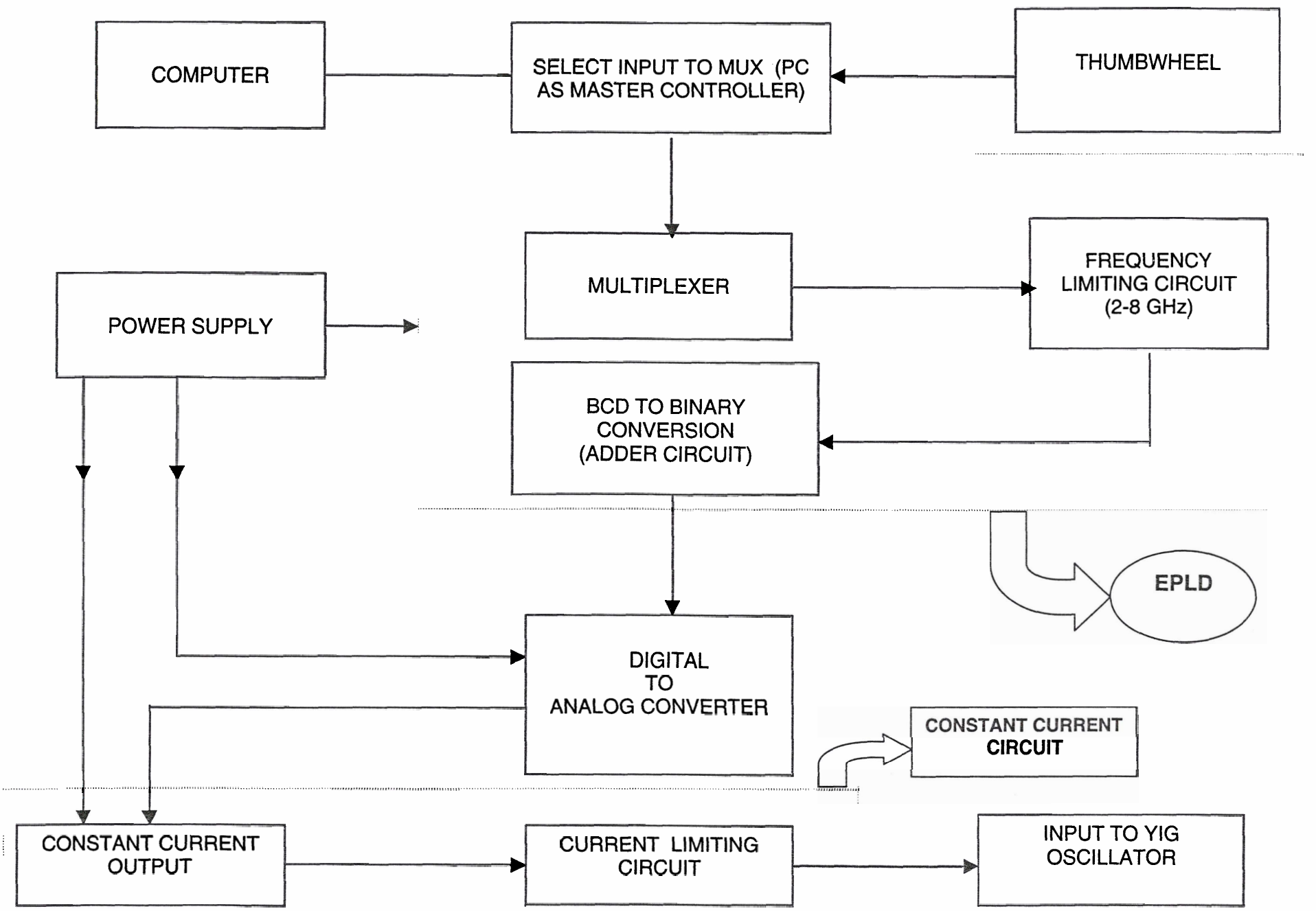
3. FREQUECY OUTPUT:

The output from the oscillator thus obtained can be measured by using a high frequency Spectrum Analyzer or a microwave Frequency Counter. The frequency obtained is compared with the frequency set and adjustments are made to get the correct frequency.

The hardware is an interface between the input and the oscillator and is required for acquisition of data. The data obtained is analysed for linearity , drift etc.

This is a brief overview of the project.

PROJECT BLOCK DIAGRAM



Input: (Computer and Thumbwheel)

This is one of the modes of input to set the YIG oscillator frequency and the other is the thumbwheel. Input can be given through either one of these modes. First of all, when the computer is off-line, the thumbwheel is the only mode of input. Using the three thumbwheels on the front panel the required frequency (x 10 MHz) can be set. The output of the thumbwheel is given to the next part of the circuit.

Thumbwheel:

The thumbwheel can be set in steps of one from 0-9. The output of the thumbwheel is in BCD format. There are 4 outputs from each thumbwheel. If 8 is set then the output from these 4 pins would be 1000. Therefore from the three thumbwheels there are twelve outputs.

Computer as an input:

Once the computer is turned on and the program is executed, there is an option for the user to select either the manual mode or the computer mode. The user can change on to the manual mode while working on the PC. The PC is interfaced using General purpose interface bus (GPIB) through which the output frequency is measured using Spectrum Analyzer and voltage/current is measured using digital multimeter.

Selection Control:

Multiplexer part is used to chose between the inputs . The thumbwheel output and the parallel port output are connected to the multiplexer. Depending on the mode of input required , the user can either set the frequency of the oscillator using the PC or the thumbwheel. We have designed a logic circuit which uses the MSB data from the parallel port output, to select either the thumbwheel or the PC. The number of input lines from the thumbwheel or the PC is twelve lines.

Choosing the number of input lines:

From the YIG oscillator specifications we note that, its frequency range is from 2-8 GHz We choose a step size of 10 MHz. So the total number of settings that can be obtained from 2-8GHz is 600 with the chosen step size of 10 MHz.

We note that for 600 steps, the minimum number of input bits should be 10 because $2^{10} = 1024$. So 1024 frequencies can be set using 10 lines.

The input from the thumbwheel and the PC is in BCD format which cannot be used directly but has to be converted to binary format because the input to the DAC is in binary.

So, in the first step,

- Input is chosen from either the thumbwheel or PC.
- Input is of 12 bits.
- It is in BCD format.
- Data from the thumbwheel is given through the EPLD.

  Data from the computer is given through the Parallel Port to the EPLD

Multiplexer:

This is used to choose between the PC and the thumbwheel. The 4 MSBs from the parallel port output are chosen and is logically connected to get a particular output depending on the required mode of input.

When the PC is off, the module is under manual control. When the PC is turned on, the module is still under manual control. Once the program required for using the PC to set the frequency is executed, a choice is given to the user to choose between the Manual and the Remote access. Depending on the choice of the user, a particular bit pattern is sent and since

the four MSBs are connected logically, the output of this logic circuit decides the required mode.

The output of the Mux is given to the next block, which is the Frequency Limiting logic circuit.

In the second step:

- Manual or the remote input is chosen by the mux.
- MSBs of the PC input is used for selection process

  Depending on the selection, thumbwheel or PC input is given to the next block i.e. the frequency limiting circuit.
- input is of 12 bits.

Frequency Limiting logic Circuit:

This is another logic circuit, which has been made to remove the mistakes that might occur during the setting of the frequency. When a frequency has to be set from the panel using the thumbwheel, the user might enter a value that may not be in the frequency range of the oscillator. The incorrect frequency set might result in a current outside the current range specified for the oscillatotor. From the specifications of the YIG we see that 20 MHz frequency requires a current of 1 mA. Therefore for a frequency of 2 GHz, the current required is 100 mA and for 8 GHz, current required is 400 mA.

So, while setting the frequency the user might enter between 0 GHz to 9999 GHz, which is outside the frequency range specified for the oscillator. This frequency has a current value outside its range.

In order to avoid this kind of mistake, the logic circuit designed limits the frequency between the 2GHz-8GHz.. The logic circuit forces the set frequency between the range of the osicllator.

Therefore in the third step:

Frequency is controlled and limited within 2-8GHz.

any value less than 2 GHz is set to 2 GHz.

- any value greater than 8 GHz if set to 8 GHz
- the number of input lines and output lines are 12

BCD-BINARY CONVERSION (ADDER CIRCUIT):

The input from the Frequency limiting circuit is now in the range of 2 – 8 GHz and is a 12-bit number in BCD format . The input to the DAC is required to be a 10 bit binary number.

The main purpose of this BCD-Binary converter circuit is to convert the 12- bit BCD number to a 10-bit binary number. This is given as the input to the DAC.

The adder circuit consists of 5 full adders. The IC used is a 7483 chip. Each IC has 4 full adders. The circuit is connected in such a manner so as to get a Binary output with 10 digits. Each binary number represents a particular value of current. The binary number given to the DAC is converted to current and this current is further processed and given to the YIG oscillator.

In the fourth step:

The BCD number is converted to Binary format.

The 12 input lines is reduced to 10 output lines

the BCD number is converted to Binary form which can be used by the DAC

The main logic circuits used above are

1) Selection control
2) Multiplexing part
3) Frequency limiting logic circuit
4) Adder Circuit

All the above digital circuits have to be used for the required frequency setting. All the above circuits need a large number of ICs.In order to improvise on this circuit, we have something know as an Erasable Programmable Logic Device (EPLD). This is a programmable chip where in the entire digital circuit can be programmed on to it to perform the same function. This reduces the space and the number of ICs by a large amount. This is very useful even though it is costlier than the ICs, but is a trend to use this in digital electronics..This EPLD is explained in detail in the later chapters. The circuit that has been programmed in the EPLD is as shown in the figure. It is noted that using the gates alone, the number of Ics that is required for the digital circuit is twenty three. This number is quite large and hence the use of EPLD reduces the number of ICs and simplifies the circuit.

Digital to Analog Converter:

The adder circuit gives out a 10 bit binary number. This binary number is given as input to the DAC. Each combination of the 10 bit binary number is converted to its equivalent current value. The DAC used here is a "MULTIPLYING DAC".

It takes in a 10 bit binary number and gives out current proportional to the binary bits.

The current from the DAC is constant but of very small value. This current has to amplified and used as input for the YIG oscillator. This is done by the constant current circuit .

In the fifth step:

- binary input is taken by the DAC.
- The binary value is converted to its equivalent analog. (current)
- This current is given to the amplifier and constant current circuit.

Constant Current Circuit:

The output of the DAC is current and this current is used as the input for the YIG oscillator. The current is made constant and is amplified by the analog circuit designed. The current should be constant because any change in the current will change the frequency, as the sensitivity of the oscillator is high. As seen in the specifications, for every 1mA change in current the frequency changes by 20 MHz. So, the current should not change, but should be constant.

Transistors are used for amplification. In order to see that the current does not exceed the permissible values, current limiting circuit is also made. A fuse is used to prevent large currents from affecting the oscillator and spoiling the other components.

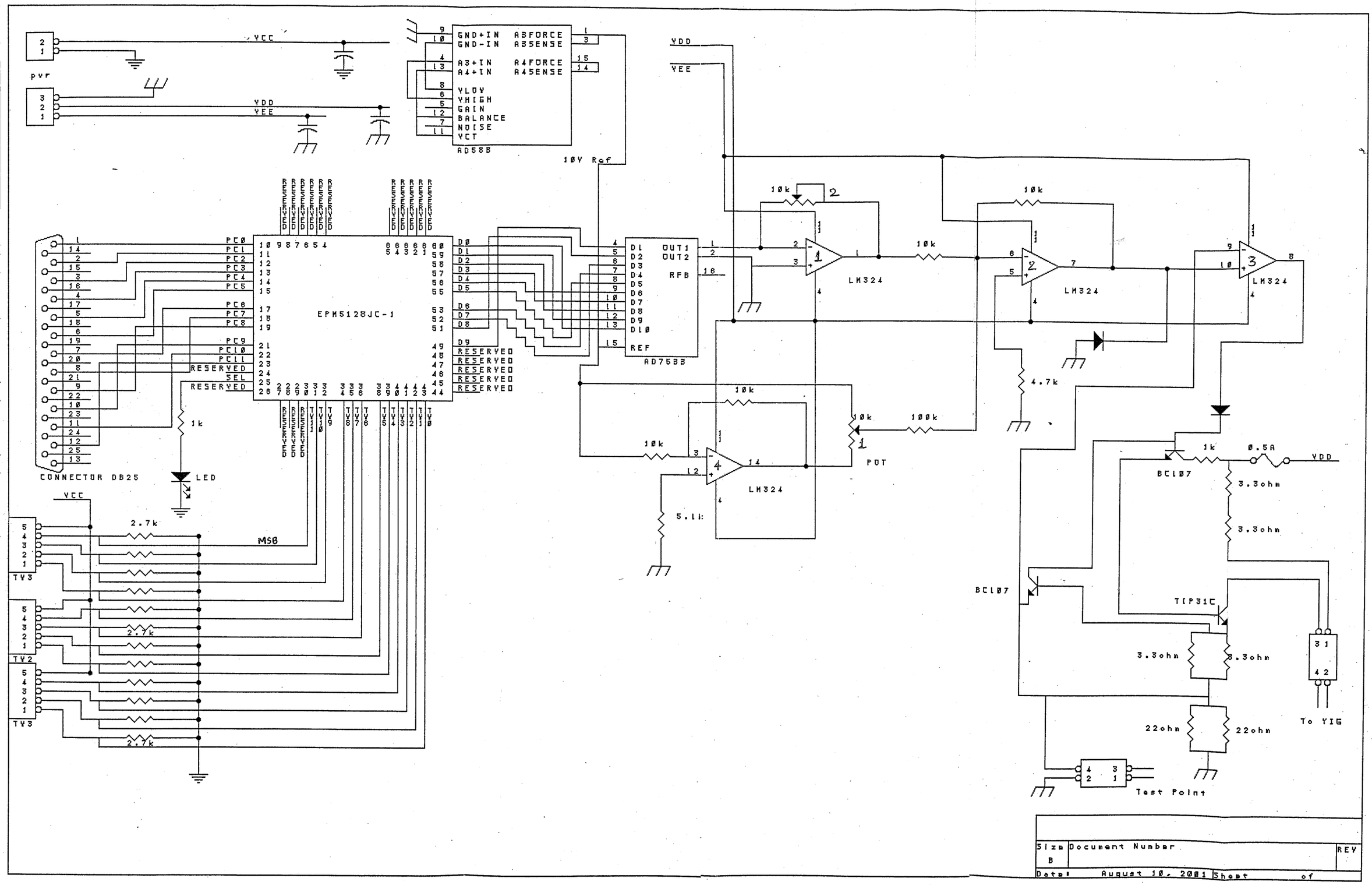
This circuit uses 4 op-amps for controlling and regulation purposes.

In the sixth step:

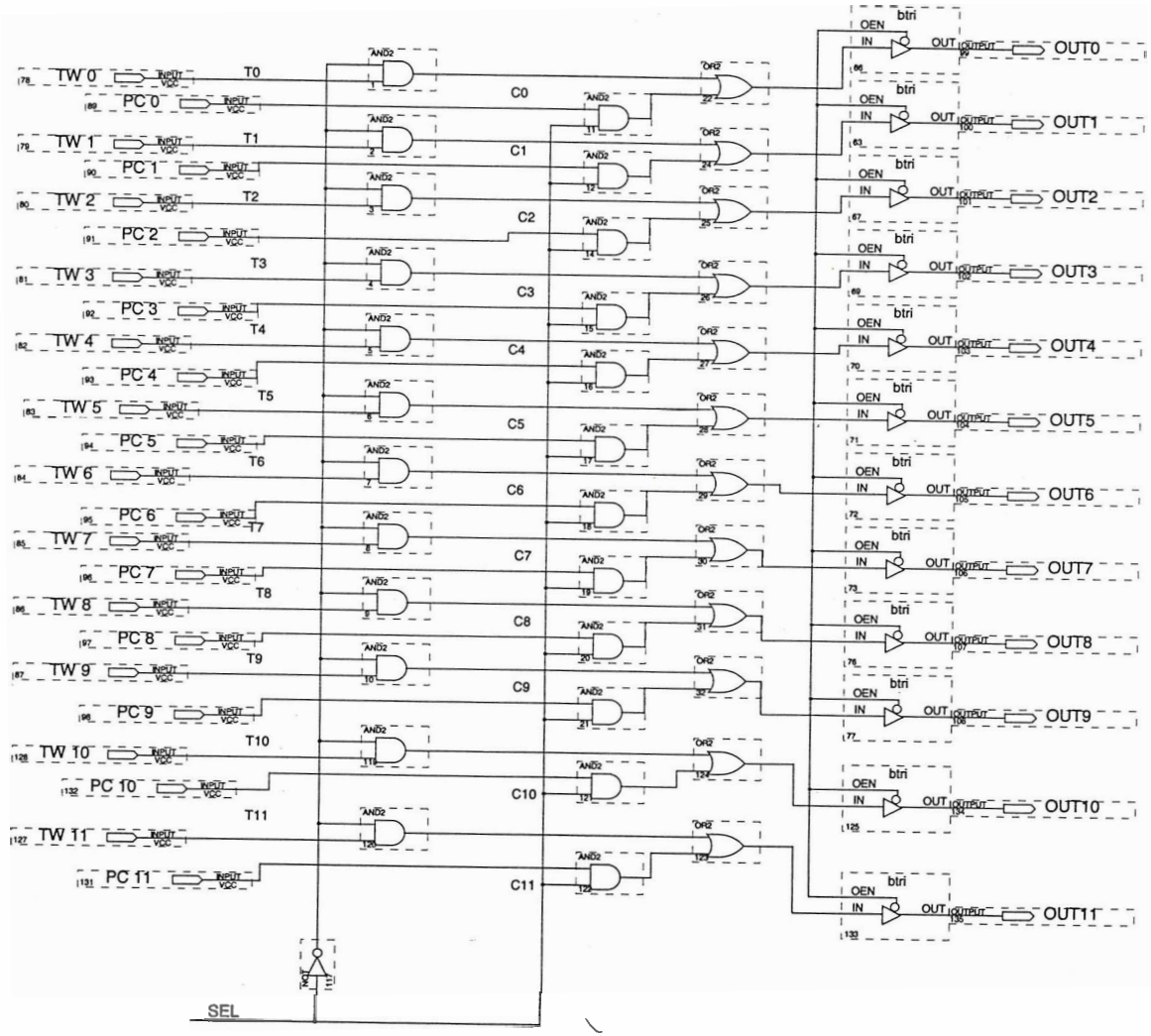
- Current output of the DAC is used as the input for the oscillator.
- This current is amplified and made constant.
- current limiting circuit and the constant current circuit together forms the "Constant Current Circuit".
- The output of this constant current circuit drives the YIG oscillator.

CHAPTER-III

PROJECT CIRCUIT DIAGRAM


VCC
PWR
VDD
VEE
AD588
GND+IN
GND-IN
A3+IN
A4+IN
VLOW
VHIGH
GAIN
BALANCE
NOISE
VCT
A3FORCE
A3SENSE
A4FORCE
A4SENSE
10V Ref
EPM5128JC-1
PC0
PC1
PC2
PC3
PC4
PC5
PC6
PC7
PC8
PC9
PC10
PC11
RESERVED
SEL
CONNECTOR DB25
1k
LED
AD7533
D1
D2
D3
D4
D5
D6
D7
D8
D9
D10
OUT1
OUT2
RFB
REF
10k
100k
POT
LM324
5.11k
4.7k
BC107
0.5A
3.3ohm
TIP31C
22ohm
To YIG
Test Point
2.7k
MSB
TV3
TV2
Size
B
Document Number
REV
Date: August 10, 2001
Sheet
of

24 INPUT-12 OUTPUT MULTIPLEXER : FIG (2 a) :



SELECTION OF PC / THUMBWHEEL :

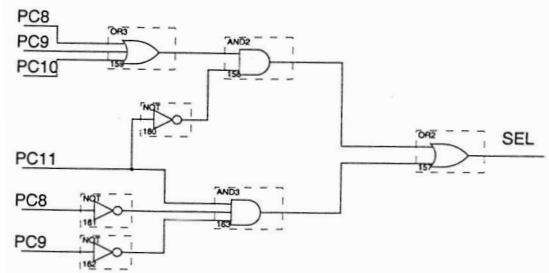


FIG (2 b):

FREQUENCY LIMITING LOGIC CIRCUIT: FIG (3 a)

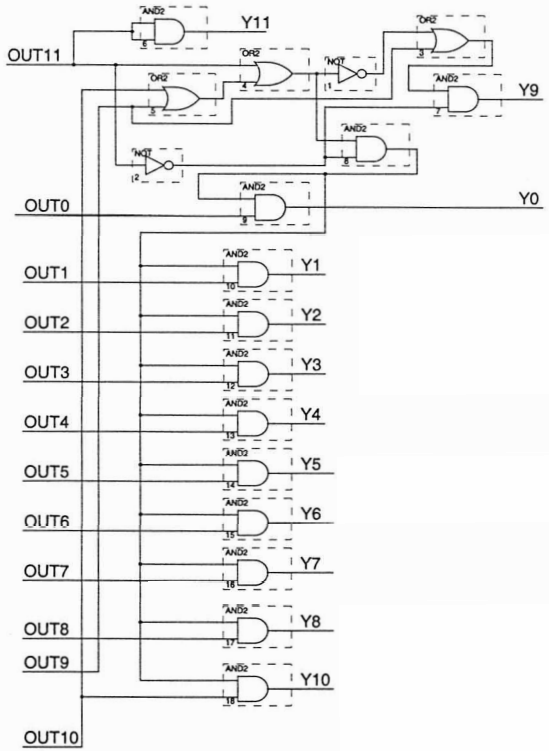
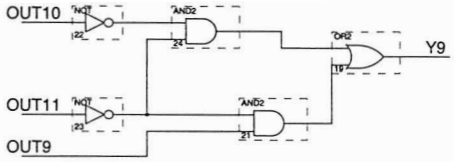
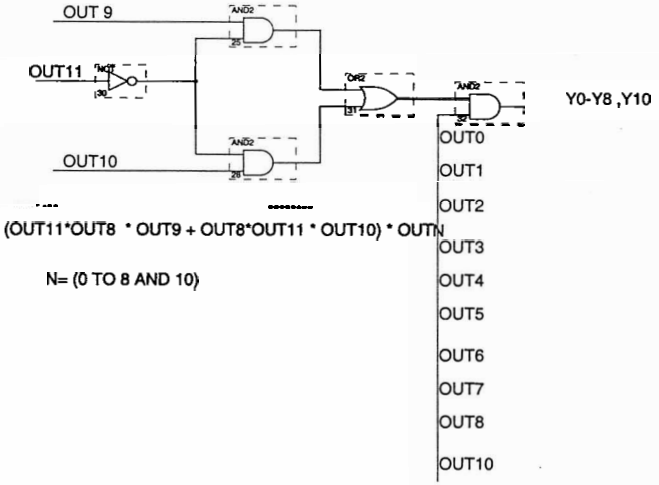


FIG (3 b):



Y9 = (OUT11 * OUT10) +(OUT11*OUT9)

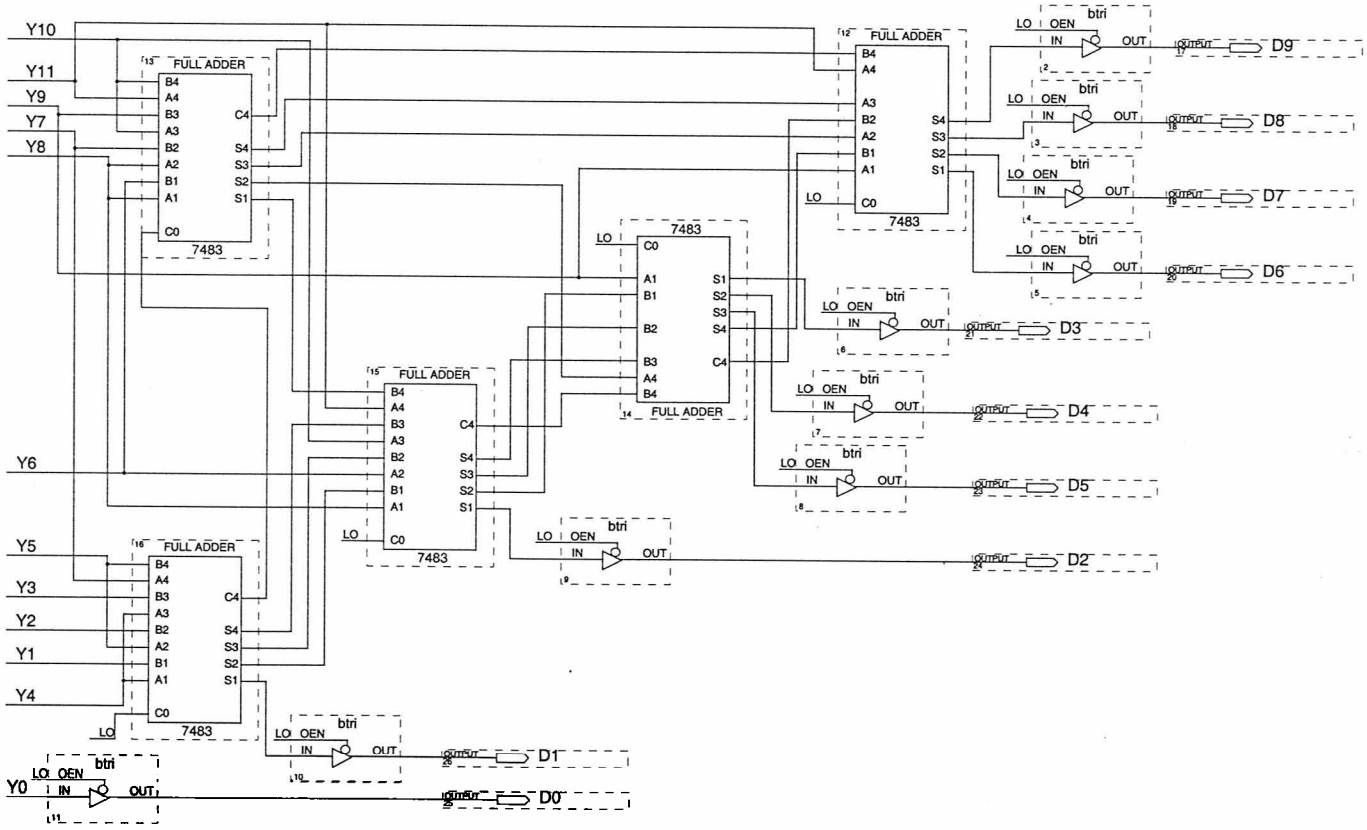
FIG (3 c):



YN = (OUT11*OUT8 * OUT9 + OUT8*OUT11 * OUT10) * OUTN

N= (0 TO 8 AND 10)

BCD TO BINARY CONVERTER FIG (4)



Circuit design :

The circuit that has been designed is a module for constant current frequency tuning. A user enters the required frequency using Thumbwheel or PC. This data is modified to generate constant current ,using which the YIG based oscillator can be tuned.

Thumbwheel:

The thumbwheel is a device that is used to set a particular number. The output of the thumbwheel is the BCD of the number selected . The thumbwheel can be set from 0-9 in steps of one, the output of thumbwheel is given to the multiplexer (enclosed in EPLD).

Multiplexer: (refer to fig (2a))

There are two methods of setting the frequency. One is the "Manual Control" (Thumbwheel) and the other method is the "Remote control"(PC control).
Mux (multiplexer) is a logical circuit that selects one of the 2^n inputs and passes it on to a single output, where n is the number of select lines. But the requirement in our project is to select a set of 12 inputs out of the 24 inputs and all the selected 12 inputs has to be passed on to the 12 output lines using only 1 select line.

The logical circuit as shown in Fig (1) does the same, one of the inputs to the first block of twelve AND gates ,is from the thumbwheel (TW0, TW1, TW2, …. TW11). The next block of twelve AND gates receive one of the inputs from the PC parallel port. A single select line SEL is connected to a NOT gate, the output is given as one of the inputs to all the twelve, two input AND gates. For the second block of twelve AND gates, one of the inputs is taken from the SEL pin directly, the other input is from the PC parallel port. The output of these twenty-four AND gates (2 Blocks) are OR-ed and taken as output.

Case 1: Here, if SEL is logic zero, then one of the inputs to the second block of twelve AND gates is zero.(An AND gate is active-high i.e., the output is high only if all the inputs to the AND gate is high and LOW if any one of the input is LOW.)

These gates receive the second input from the computer parallel port. Hence, this set is not activated, whereas the first block of AND gates, one of the inputs is SEL i.e., for SEL zero input is one and hence the output of this set of AND gates depends on the second input i.e., from the thumbwheel. As the output of these blocks i.e., twenty-four AND gates are OR-ed and output of the second block being zero for SEL = 0, the output of the first block of AND gates is the output of the OR gate.

Case 2: When SEL = 1

Output of the PC parallel port is the output of the OR gate . The logic is as explained above.

SELECTION OF PC/THUMBWHEEL: (Refer to (fig2b)

$Y_{11}Y_{10}$ \ Y_9Y_8	00	01	11	10
00	0	1	1	1
01	1	1	1	1
11	0	0	0	0
10	1	1	0	0

$$\overline{Y_{11}}\,Y_8 + \overline{Y_{11}}\,Y_9 + \overline{Y_{11}}\,Y_{10} + Y_{11}\,\overline{Y_{10}}\;\overline{Y_9} + \overline{Y_{11}}\,(Y_8 + Y_9 + Y_{10}) + Y_{11}\,\overline{Y_{10}}\;\overline{Y_9}$$

To make the PC as master, once we turn on the PC and enter the data the SEL output should be high. And as explained in Case 2: the PC is activated and hence the required frequency can be set by entering the data through the computer and the manual mode of data entry is disabled. If the PC hangs , all the bits of the output port are high and under such conditions the output of the Fig(3), that is low as explained in Case 1 the control shifts to Manual mode. The output of the SEL is low when the PC is off i.e., the inputs PC8-PC11 are all low and so the input control is still manual. The output of this circuit is low only if all the four bits are high or all the four inputs are low. For any other combination the output is a logical high.

(2-8) GHz Frequency Limiter : (refer to figure(3a))

Now, we know that in a thumbwheel the data entered ranges from 0000 to 9999, that represents 0000 MHz to 9999 MHz., but our range of interest is from 2000 MHz to 8000 MHz., i.e., from 2000 to 8000 on the thumbwheel. Hence a logical circuit is required such that for any value entered by the user out of this range, the circuit has to give an output of 2000, for a value entered less that 2000 and the output forced to 8000 for any input less than 8000 and for any value entered within this range, has to be passed on without any change.

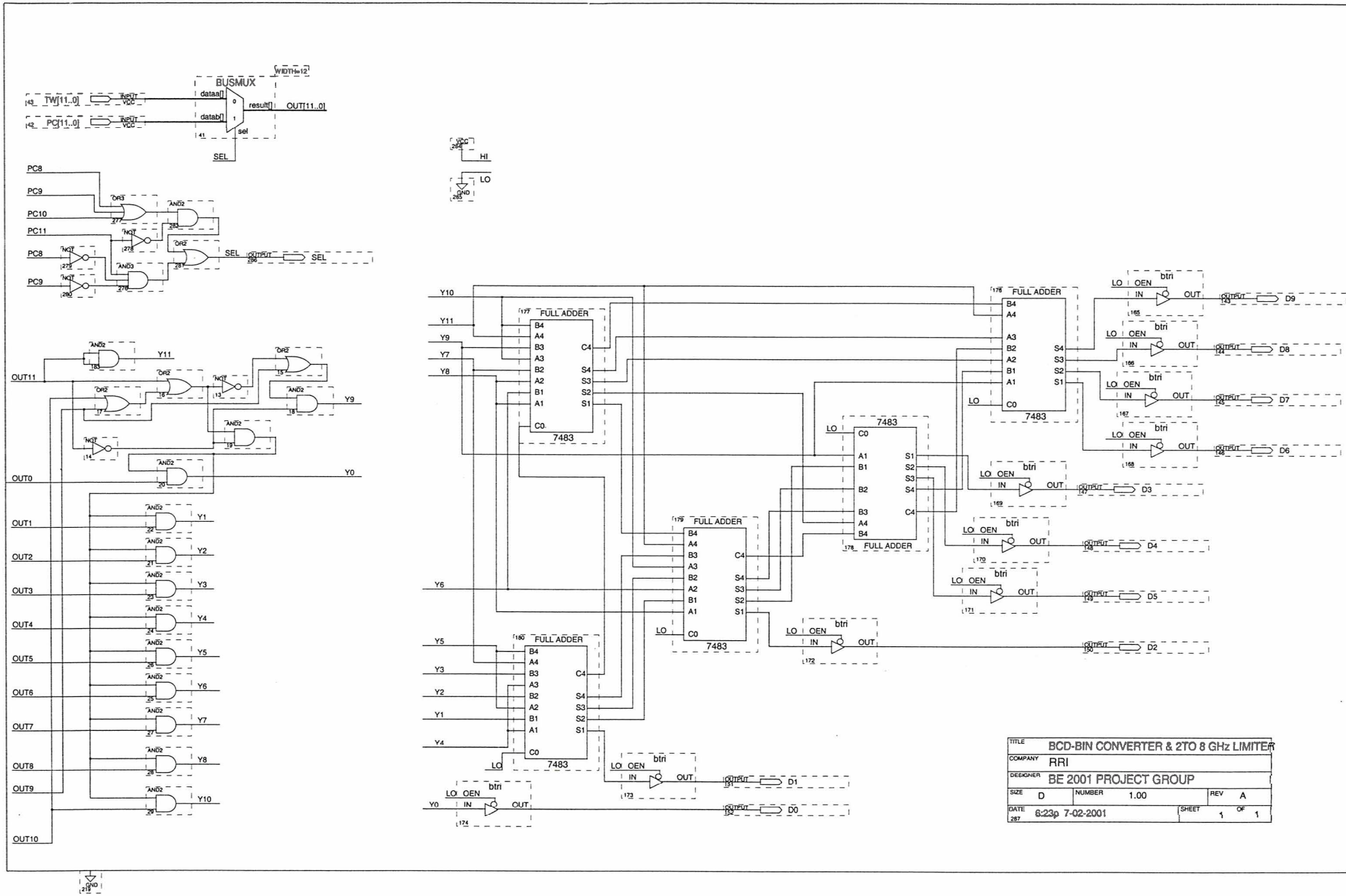
Truth Table for 2 GHz to 8 GHz limiter circuit

Out_{11}	Out_{10}	Out_9	Out_8		Y_{11}	Y_{10}	Y_9	Y_8		Y_7 to Y_0
0	0	0	0		0	0	1	0		0
0	0	0	1		0	0	1	0		0
0	0	1	0		0	0	1	0		OUT_7 to OUT_0
0	0	1	1		0	0	1	1		"
0	1	0	0		0	1	0	0		"
0	1	0	1		0	1	0	1		"
0	1	1	0		0	1	1	0		"
0	1	1	1		0	1	1	1		"
1	0	0	0		1	0	0	0		"
1	0	0	1		1	0	0	0		"

Y / Y_{11} Y_{10}	0	1
00	1	1
01	0	1
11	0	0
10	0	0

$$Y_9 = (\overline{OUT_{11}}\,\overline{OUT_{10}}) + (OUT_{11}\,\overline{OUT_9})$$

Refer to Fig 3 b


BUSMUX
WIDTH=12
TW[11..0]
PC[11..0]
INPUT
VCC
data[]
datab[]
sel
result[]
OUT[11..0]
SEL
PC8
PC9
PC10
PC11
OR3
AND2
NOT
OR2
AND3
OUTPUT
VCC
HI
GND
LO
OUT11
OUT0
OUT1
OUT2
OUT3
OUT4
OUT5
OUT6
OUT7
OUT8
OUT9
OUT10
Y11
Y9
Y0
Y1
Y2
Y3
Y4
Y5
Y6
Y7
Y8
Y10
FULL ADDER
7483
B4
A4
B3
A3
B2
A2
B1
A1
C0
S4
S3
S2
S1
C4
btri
LO OEN
IN
OUT
D9
D8
D7
D6
D5
D4
D3
D2
D1
D0
TITLE
BCD-BIN CONVERTER & 2TO 8 GHz LIMITER
COMPANY
RRI
DESIGNER
BE 2001 PROJECT GROUP
SIZE
D
NUMBER
1.00
REV
A
DATE
6:23p 7-02-2001
SHEET
1
OF
1

$OUT_{11}\,OUT_{10}$ \ $OUT_9\,OUT_8$	00	01	11	10
00	0	0	1	0
01	0	1	1	0
11	0	0	0	0
10	0	0	0	0

$$Y_n = (\overline{OUT_{11}}\,OUT_8\,OUT_9 + OUT_8\,\overline{OUT_{11}}\,OUT_{10})(OUT_n)$$

Where , n = 0 to 8 and 10.

Refer to fig 3.c.

The BCD output Y_0 to Y_{11} is given to a BCD-Binary converter circuit. This circuit involves twenty full adders and the output of this is given to the DAC. The main function of this circuit is that it converts the twelve input BCD to a ten bit binary output.
All the logic circuits starting from the multiplexer to the BCD to Binary converter are included in the EPLD.

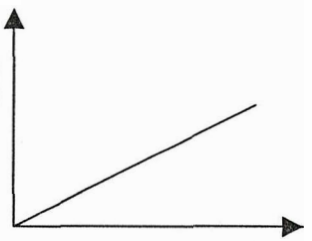
Multiplying DAC :

The reference voltage may be a fixed value internal to the device .In a multiplying DAC ,it is applied externally as a second input the output can be viewed as a product of the reference voltage and a fraction determined by the N-bit digital input x..

For a 10-bit DAC the minimum step size is $Vref/2^{10}$ or approximately 0.1% of the full scale. The output of the DAC is digitally controlled fraction of the reference voltage so that device plays the role of digital potentiometer.

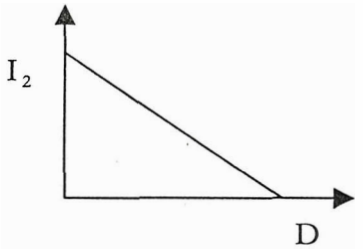
The digital to analog converter used here is AD7533. This is a 10 bit multiplying DAC. It consists of highly stable thin film R-2R Ladder and 10 CMOS switches on a monolithic chip. The simplified digital to analog circuit is shown in the figure. An inverted R-2R ladder structure is used i.e., the binary weighted currents are switched between the Iout1 and Iout2 bus lines. Thus the sum of currents in both the lines remains constant independent of the switch state. **For a 10V reference input, the current in switch 1 is 0.5 mA.** The current to switch 2 is 0.25 mA. and so on.

The current I_1 increases with increase in bits.



$0 < D < 1023/1024$

The current I_2 decreases with increase in bits



The binary output from the EPLD is given as input to the DAC. This input varies from 200 in binary to 800 in equivalent binary. The output current of the DAC is

DAC Input	$I_1(D)$	$I_2(1-D)$
200	1.955 mA	8.045 mA
800	7.82 mA	2.179 mA

for

$I_{ref} = 1$ mA

$V_{ref} = +10.00$ V

As calculated the current input to the YIG is 0.1A for 2 GHz to 0.4 A for 8 GHz. (from the specification for the YIG oscillator 20 MHz/1 mA)

The current output in line I1 for an input of 200 is 1.955 mA, which has to be amplified to 0.1 A, and for an input of 800 the current output of DAC is 7.820 mA and this has to be amplified to 0.4 A.

If I_2 is selected then 8.045 mA has to be scaled to 0.1 A. to obtain an output frequency of 2000 MHz and 2.179 mA has to be scaled to 0.4 A. for an output frequency of 8000 MHz. We see that the output current I_2, of DAC decreases with an increase in input bit pattern, where as, the required current to drive the oscillator increases with increase in required frequency i.e., for 2000 MHz the current required is 0.1 A and for 8000 MHz the current required is 0.4 A. Hence the output current has to be subtracted from the constant value of current. The difference between the currents increases with increase in bit pattern and hence the required output can be obtained.

Here, we have selected I_1 and this current is converted into voltage. The first op-amp circuit is a current to voltage converter. The voltage at point 1 is $V_1 = -I_1R_1$.

Hence the output voltage is proportional to R_1 if I_1 is kept constant.

The current flowing in line I_1 flows from 2 to 1 through the resistor R_1.

$$V_2=V_3=0$$

$$V_2-V_1=I_1R_1$$

$$V_1 = -I_1R_1$$

The voltage at V_1 is negative and is equal to I_1R_1. This voltage is then inverted to get a positive voltage. This inversion is done using op-amp (2). Hence, the voltage

$$-V_7 = 10k/10k * V_1$$

$$= -I_1R_1$$

$$V_7 = I_1R_1$$

This voltage has to be converted to current to give an input to the oscillator. Hence, we shall use the voltage dependent current source or the constant current source.

$$I_{out} = V_{in} / R$$

Therefore, the output of the current to voltage converter, being a negative voltage is further inverted and given as input to the third op-amp.

By, the virtual ground property of the op-amp, the voltage at point (9) is same as that at point(10). This voltage is given to point (4). Therefore, current through

$$I_c = (V_a - 0)/R = V_a/R$$

$$I_{out} = I_c = V_a/R$$

The maximum current that will flow is 0.4 A. Therefore, the resistor selected has to be of proper wattage. Here, the two 22 ohm resistors are 4 Watts , high precision resistors.

For a current range of 0.1 A – 0.4 A the voltage across this parallel combination or voltage at V_a

Should be 0.1 * 11 = 1 .10 V to 0.4 * 11 = 4 .40 V

Therefore, V_a must vary from +1.10 V to +4.4 0V.

The voltage at V_7 = +1.10 V for frequency setting of 2000 MHz.

= +4.40 V for frequency setting of 8000 MHz

Similarly, at point (6) , the input is –1.10 V to –4.40 V.

The current output of the DAC varies from 0.195 mA to 0.781 mA. Therefore, to calculate the feedback resistor in op-amp (1)

Voltage output(V)	Input Current (mA)	Feedback resistance R_b (kΩ)
1.1	0.195	5.641
4.4	0.781	5.632

Therefore, let R_b = 5.6 kΩ. Hence, R_b, has to be 5.6 kΩ.

The circuit must be provided with gain control and offset control. To provide gain control, the feedback resistor can be replaced by a potentiometer of 10 kΩ.

To provide offset op-amp (2) can be used as a summer circuit and sum amplitude of voltage can be either added or subtracted from the output of op-amp (1) and hence an offset of ± 1V can be given to the circuit. A 10-kΩ pot is used to vary between +10 V and –10 V.

A gain of $1/10^{th}$ has to be provided so that offset varies between +1 V to –1 V.

Op-amp (2) was used as an inverter with only the input from op-amp (1) but now it is used as summer.

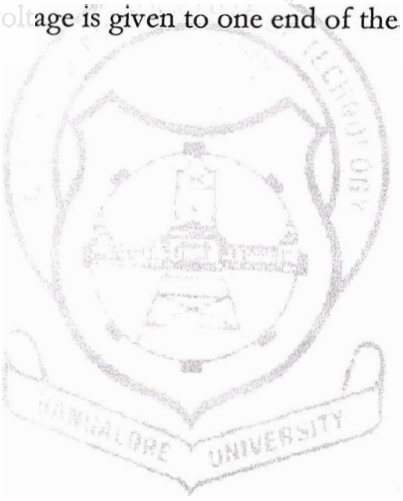
The output of op-amp (2) is $V_7 = V_1 * R_{f2}/R_6 + V_{pot} * R_{f2} / R_p$

Therefore, let R_{f2} = 10 kΩ and R_6 = 10 kΩ. Then R_p = 100 kΩ.

Therefore, $V_7 = V_1 * 1 + V_{pot} * 1/10$

The reference voltage to the DAC i.e., +10.00 V is generated using AD588. This IC generates a reference voltage of +10.00 V, when powered with +15 V & -15 V supply

For offset, the same +10.00 V reference is used and to generate –10.00 V, the input is given to point (13) of op-amp (4) and the output of op-amp (4) at point (14) is $-V_{in}$ and the output is therefore –10.00 V. This voltage is given to one end of the 10-kΩ pot and the other end is given to +10.00 V.



CHAPTER-IV

ERASABLE PROGRAMMABLE LOGIC DEVICE (EPLD)

ERASABLE PROGRAMMABLE LOGIC DEVICE (EPLD)

Altera Erasable Programmable Logic Devices

Except for very high-speed programmable logic, the general trend has been toward CMOS implementation, with its much higher levels of circuit integration and lower power demands than bipolar technologies. PALs were initially based on the same "program once" technology as bipolar PROMs. Altera pioneered the development of erasable programmable logic devices (EPLDs) based on CMOS erasable ROM technology. The EPLD can be erased simply by exposing it to ultraviolet (UV) light and then reprogrammed at a later time. Altera EPLDs are equivalent to 100 to 1000 conventional two-input gates, depending on the model selected.

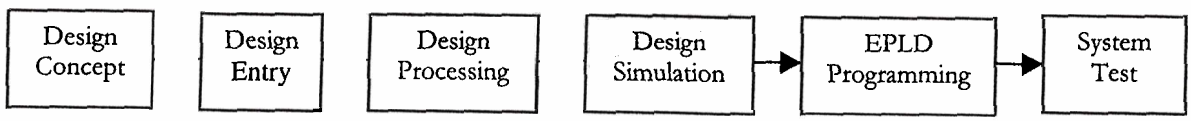
- These are devices that allow engineers to electrically program standard, off-the-shelf logic elements to meet the specific needs of their applications.
- These devices can be programmed depending on the circuitry required for their applications.
- The key to this capability is re-programmable CMOS technology, which is used to create Erasable Programmable Logic Devices (EPLD's)
- Types of EPLD's:
    - ❖ General Purpose EPLD's:
      Classic, MAX 5000 and MAX 7000 EPLD
    - ❖ Function- specific EPLD's:
    - ❖ **Mask – Programmed Logic** Devices (MPLD's)
- EPLD's can be used to integrate complete printed circuit board of TTL, PAL and FPGA devices into a single package.
- The EPLD's are all programmed using MAX+ PLUS BASELINE software made by Altera.
- EPLD's are available in windowed (erasable) ceramic packages or one-time programmable (OTP) plastic versions.

- Proprietary logic functions can be designed and fabricated in-house, eliminating the long engineering lead times, high tooling costs, complex procurement logistics and dedicated inventory problems associated with custom

"APPLICATION SPECIFIC INTEGRATED CIRCUIT (ASIC) "devices such as gate arrays and standard cells.

Altera, is the company that makes these EPLD's. Altera software products are developed together with the EPLD architectures, so that features are placed where they are most appropriate in either software or hardware.

EPLD Design Methodology:



Design Entry: Several types namely hierarchical schematic capture, Altera Hardware Description Language (AHDL), Boolean equation, state machine, truth table, waveforms, micro-coded assembly language. These methods can be freely combined to create a single EPLD design.

Design Compilers: They perform minimization and logic synthesis, design fitting (automatic place and route) and generate programming data.

Design Verification: This is done through Functional simulation, timing simulation and delay prediction for speed critical paths.

Hardware for programming EPLD's is offered by Altera and a variety of third-party vendors.

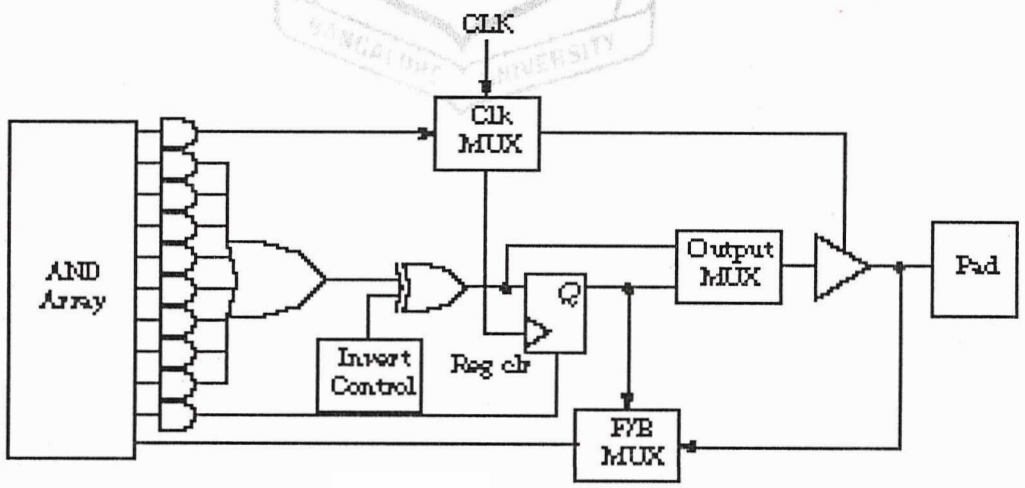
Software interfaces to other design tools are provided by Altera and third party translators and via industry standard net lists.

Altera approach to logic design eliminates the necessity of mastering the inner complexities of EPLD architectures. The user can work with familiar design entry tools and the Altera software automatically translates the design into the format required to fit the EPLD architecture.

Altera general purpose EPLD's provide dedicated input pins, user configurable I/O pins and clock options and flip-flop that ensure maximum flexibility for integrating random logic function.

Macrocell Architecture:

EPLD Macrocell Architecture The basic element of the EPLD is the macro-cell, containing an eight-product-term AND-OR array and several programmable multiplexers. Multiplexers are particularly easy to implement in MOS technology, so it is no surprise that they are pervasive in CMOS-based programmable logic.



Altera macrocell schematic.

Figure gives a block diagram/schematic view of the macrocell's contents. Its elements include a programmable AND array, a multiple fan-in OR gate to compute the logic function with programmable output polarity (via the XOR gate), a tri-state buffer driving an I/O pin, a programmable sequential logic block, and a programmable feedback section. Depending on the component, an EPLD may contain from 8 (EP300 series) to 48 (EP1800 series) such macrocells, each of which can be independently programmed.

Let's look at each of the programmable elements of the macrocell. As you will see, it offers more flexibility than any of the PAL architectures we have seen so far.
The macrocell's AND array is crossed with the true and complement of the EPLD's dedicated input and clock pin signals and the internal feedbacks from each of the component's outputs. Cross-points are implemented by EPROM connections that are initially connected. Unwanted connections are broken by "blowing" the appropriate EPROM bits.
The multiplexers allow the feedback, output, and clock sections to be independently programmed. The MUX selection lines are controlled by their own EPROM bits. Under MUX control, the combinational function can bypass the flip-flop on the way to the output. Thus you can program any output to be either combinational or registered.

Similarly, macrocell feedback into the AND arrays can come from the registered output or from the external pin. You can program many of the pins to be either output or input.

Altera MAX Architecture: The major problem with all AND-OR structures is the difficulty of sharing product terms among macrocells. In a conventional PAL, you cannot share the same product term across -different OR gates. The term must be repeated for each output. This can lower the efficiency of the PAL, reducing the number of equivalent discrete gates it can replace.

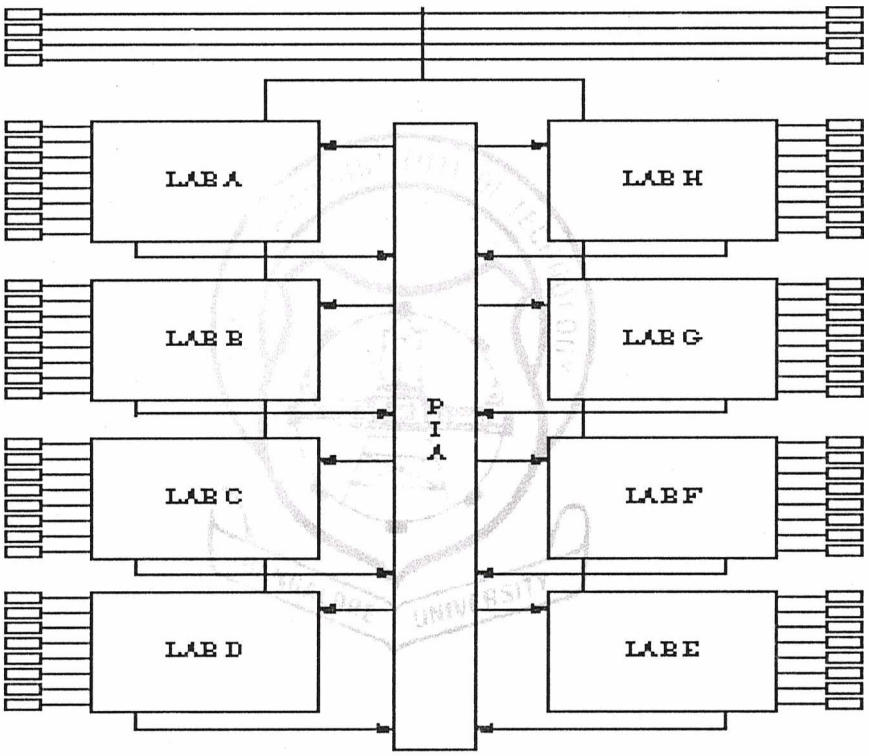
As programmable logic devices become even more highly integrated, the architectures must evolve to provide more area for global routing of signals. It must be possible to share terms

and outputs between macrocells more easily. Altera has addressed these problems in their *multiple array matrix* (MAX) family of parts. We describe the structure of MAX components in this subsection.

Macrocells, similar in structure to Figure 10.25, are grouped into Logic Array Blocks (LABs). Associated with each LAB is a group of additional product terms, usable by any of the macrocells within the LAB. These Expander Product Terms make it possible to implement a function with up to 35 product terms inside a single macrocell. This compares to only eight terms per function in most PAL families.

In addition, a Programmable Interconnect Array (PIA) can route the LAB's macrocell outputs globally throughout the device. Some lower-density devices also use the PIA to route the product term expanders.

Figure below shows the generic architecture of a MAX component, the EPM5128. The device has eight dedicated inputs (including the clock), 64 programmable I/O pins, eight LABs, 16 macrocells per LAB (128 macrocells total-not all macrocells are connected to an output pin), and 32 product term expanders per LAB (256 total). The dedicated input pins come in along the top and are distributed to each of the eight LABs. The PIA routes global signals. All on-chip signals have a connection path to the PIA. Only the signals needed by a particular LAB are connected to it under EPROM programming.



Altera EPM5128 block diagram

Once you reach devices as complex as the advanced MAX family, you would be unlikely to try to generate the personality map by hand. Altera provides an extensive tool set for mapping logic schematics onto the primitives supported by their EPLD structures.

MAX 5000 EPLD's:

These EPLD's are suitable for register intensive random logic and TTL and PAL integration. The EPLD being used in our project is a MAX 5000 series of type **EPM5128JC-1**

General Information on EPM5128JC-1:

- EPLD: EPM5128
- Package: J Type
- Temperature: C
- Speed Grade: -1
- t_{PD1}(ns): 25
- f_{max} (MHz): 62.5
- I_{cc3}(mA): 250 (active)
- I_{cc1}(mA): 225 (Standby)
- Macrocells: 128 (Registers)
- Dedicated I/P's: 8
- I/O pins: 52
- Number of pins: 68

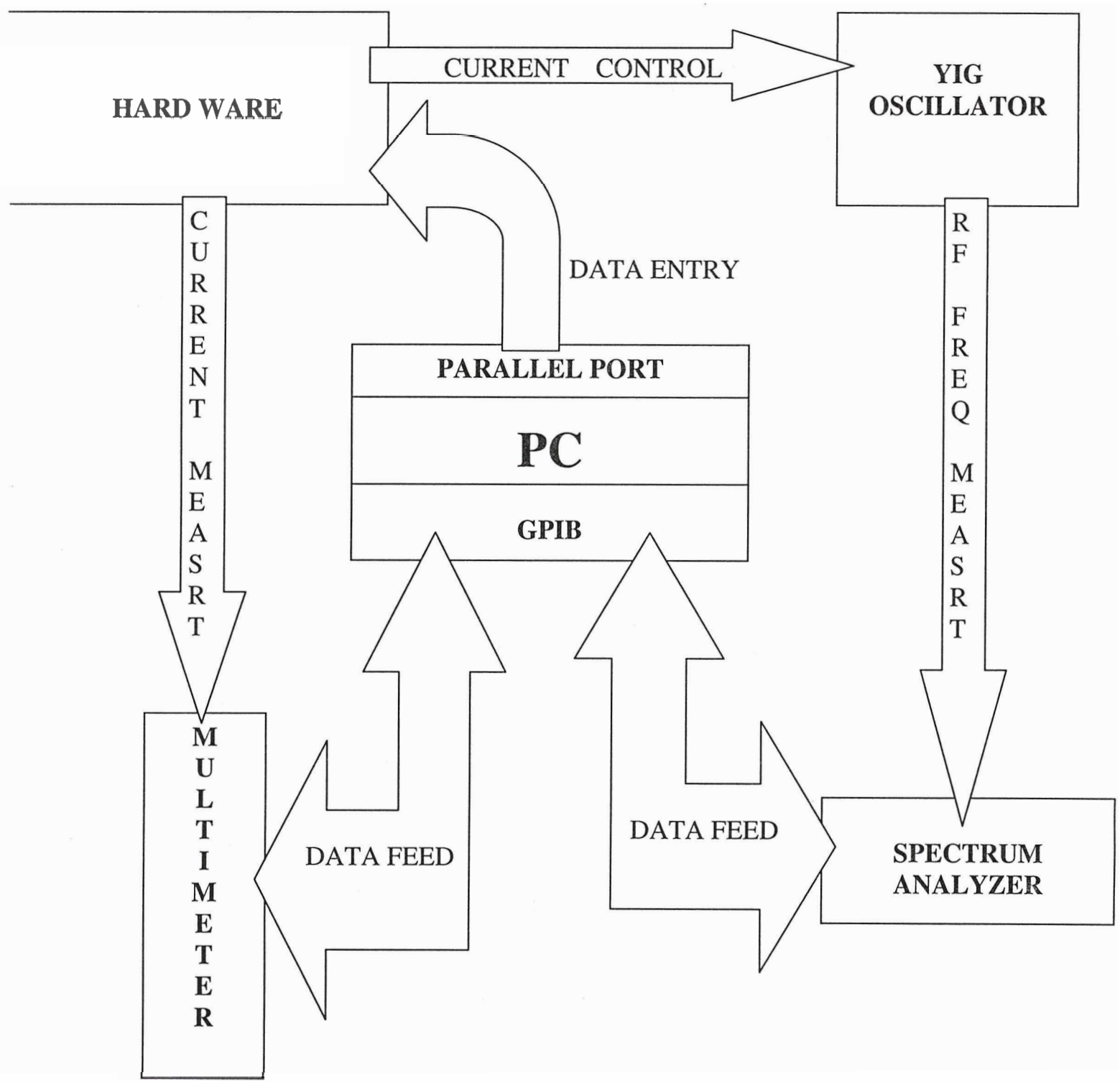
Features of EPM5128:

- High-density 128-macrocell general purpose MAX 5000 EPLD
- 256 shareable expander product terms that allow over 32 product terms in a single macrocell.
- High-speed multi LAB architecture.
- Programmable I/O architecture allowing up to 60 inputs or 52 outputs.
- Available in 68 pin windowed ceramic or plastic one-time programmable lead packages or re-programmable packages.
- It can replace over 60 TTL, MSI and SSI components and integrate multiple 20-24 pin low density PLD's.

CHAPTER-V

INTERFACING WITH PARALLEL PORT

BLOCK DIAGRAM OF INTERFACING



INTERFACING THE STANDARD PARALLEL PORT

Introduction to Parallel Ports :

The Parallel Port is the most commonly used port for interfacing home made projects. This port will allow the input of up to 9 bits or the output of 12 bits at any one given time, thus requiring minimal external circuitry to implement many simpler tasks. The port is composed of 4 control lines, 5 status lines and 8 data lines. It's found commonly on the back of your PC as a D-Type 25 Pin female connector.

Hardware Properties :

Below is a table of the "Pin Outs" of the D-Type 25 Pin connector. The D-Type 25 pin connector is the most common connector found on the Parallel Port of the computer.

Pin No (D-Type 25)	SPP Signal	Direction In/out	Register	Hardware Inverted	Pins of Interest
1	nStrobe	In/Out	Control	Yes	☜
2	Data 0	Out	Data		☜
3	Data 1	Out	Data		☜
4	Data 2	Out	Data		☜
5	Data 3	Out	Data		☜
6	Data 4	Out	Data		☜
7	Data 5	Out	Data		☜
8	Data 6	Out	Data		☜
9	Data 7	Out	Data		☜
10	nAck	In	Status		
11	Busy	In	Status	Yes	

12	Paper-Out / Paper-End	In	Status		
13	Select	In	Status		
14	nAuto-Linefeed	In/Out	Control	Yes	
15	nError / nFault	In	Status		
16	nInitialize	In/Out	Control		
17	nSelect-Printer / nSelect-In	In/Out	Control	Yes	
18 - 25	Ground	Gnd			

Table 1. Pin Assignments of the D-Type 25 pin Parallel Port Connector.

Port Addresses :

The Parallel Port has three commonly used base addresses. These are listed in table 2, below. The 3BCh base address was originally introduced used for Parallel Ports on early Video Cards.LPT1 is normally assigned base address 378h, while LPT2 is assigned 278h. However this may not always be the case as explained later. 378h & 278h have always been commonly used for Parallel Ports. The lower case h denotes that it is in hexadecimal. These addresses may change from machine to machine

Address	Notes:
3BCh - 3BFh	Used for Parallel Ports which were incorporated on to Video Cards
378h - 37Fh	Usual Address For LPT 1
278h - 27Fh	Usual Address For LPT 2

Table 2 Port Addresses

When the computer is first turned on, BIOS (Basic Input/Output System) will determine the number of ports you have and assign device labels LPT1, LPT2 & LPT3 to them. BIOS first

looks at address 3BCh. If a Parallel Port is found here, it is assigned as LPT1, and then it searches at location 378h. If a Parallel card is found there, it is assigned the next free device label. This would be LPT1 if a card wasn't found at 3BCh or LPT2 if a card was found at 3BCh. The last port of call is 278h and follows the same procedure than the other two ports. Therefore it is possible to have a LPT2, which is at 378h and not at the expected address 278h.

What can make this even confusing is that some manufacturers of Parallel Port Cards have jumpers, which allow you to set your Port to LPT1, LPT2, LPT3. Now what address is LPT1? - On the majority of cards LPT1 is 378h, and LPT2, 278h, but some will use 3BCh as LPT1, 378h as LPT1 and 278h as LPT2. *Life wasn't meant to be easy.*

Software Registers - Standard Parallel Port (SPP)

	Name	Read/Write	Bit No.	Properties
Base + 0	Data Port	Write (Note-1)	Bit 7	Data 7
			Bit 6	Data 6
			Bit 5	Data 5
			Bit 4	Data 4
			Bit 3	Data 3
			Bit 2	Data 2
			Bit 1	Data 1
			Bit 0	Data 0

Table 4 Data Port

Note 1: If the Port is Bi-Directional then Read and Write Operations can be performed on the Data Register.

The base address, usually called the Data Port or Data Register is simply used for outputting data on the Parallel Port's data lines (Pins 2-9). This register is normally a write only port. However if your port is bi-directional, you can receive data on this address.

Offset	Name	Read/Write	Bit No.	Properties
Base + 1	Status Port	Read Only	Bit 7	Busy
			Bit 6	Ack
			Bit 5	Paper Out
			Bit 4	Select In
			Bit 3	Error
			Bit 2	IRQ (Not)
			Bit 1	Reserved
			Bit 0	Reserved

Table 5 Status Port

The Status Port (base address + 1) is a read only port. Any data written to this port will be ignored. The Status Port is made up of 5 input lines (Pins 10,11,12,13 & 15), an IRQ status register and two reserved bits. Please note that Bit 7 (Busy) is an active low input. E.g. if bit 7 happens to show logic 0, this means that there is +5v at pin 11. Likewise with Bit 2. (nIRQ) If this bit shows a '1' then an interrupt has **not** occurred.

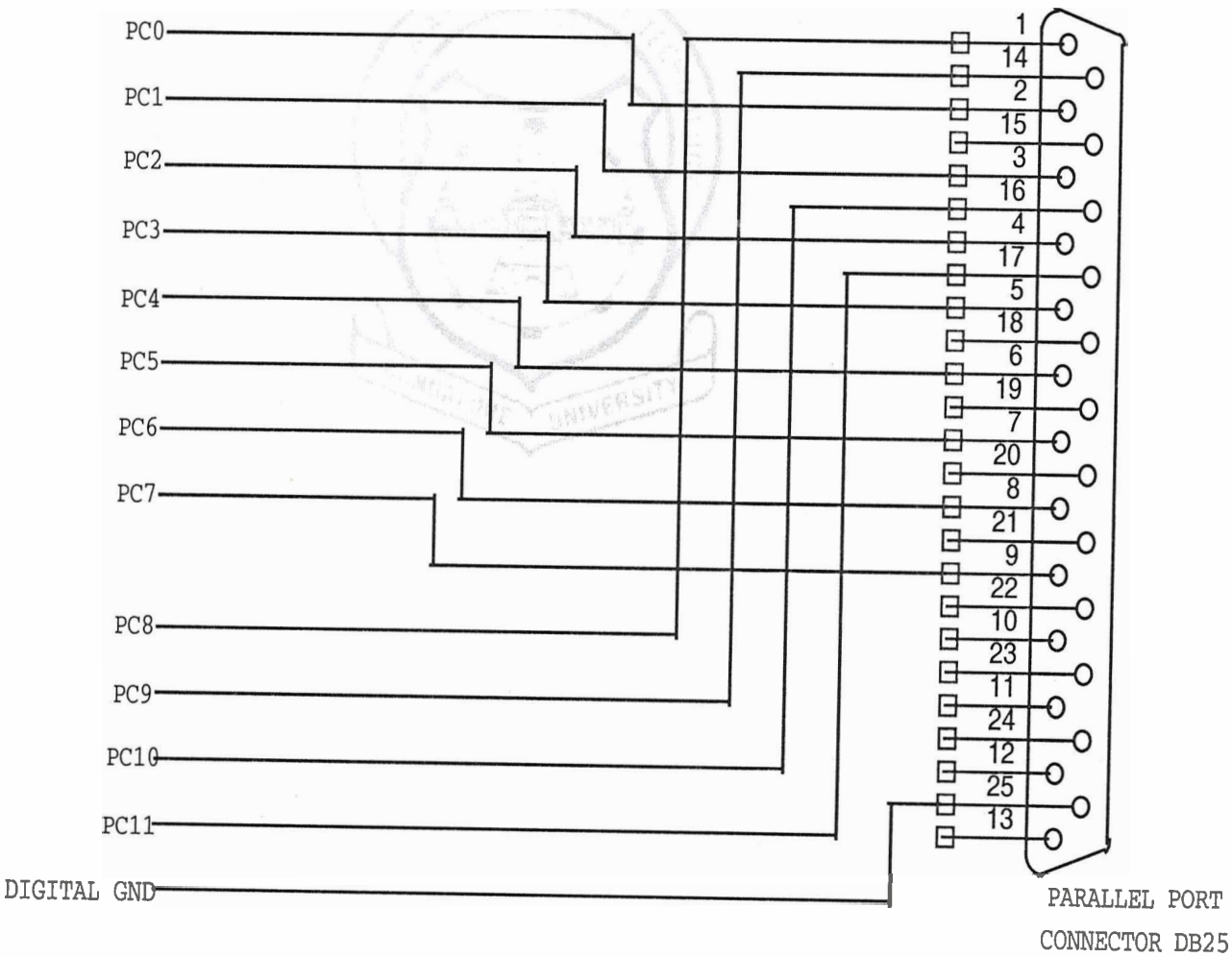
Offset	Name	Read/Write	Bit No.	Properties
Base + 2	Control Port	Read/Write	Bit 7	Unused
			Bit 6	Unused
			Bit 5	Enable Bi-Directional Port
			Bit 4	Enable IRQ Via Ack Line
			Bit 3	Select Printer
			Bit 2	Initialize Printer (Reset)
			Bit 1	Auto Linefeed
			Bit 0	Strobe

Table 6 Control Port

The Control Port (base address + 2) was intended as a write only port. When a printer is attached to the Parallel Port, four "controls" are used. These are Strobe, Auto Linefeed, Initialize and Select Printer, all of which are inverted except Initialize.

SIGNALS FROM PARALLEL PORT TO EPLD;

The figure below shows us the signals from parallel port to EPLD. Pin numbers 2 to 7 constitute PC0 to PC7 of EPLD while pin numbers 1,14,16 and 17 constitute PC8 to PC11 of EPLD. Pin number 25(as pin numbers 18 to 25 is at logic ground w.r.t. parallel port) of parallel port is connected to digital ground of the EPLD. So we see that a total of 12 pins or data lines(i.e. the maximum number of data that can be sent from a parallel port at any given time) are being used as output lines from the parallel port to the hardware i.e. to the EPLD of the circuit to be precise.


PC0
PC1
PC2
PC3
PC4
PC5
PC6
PC7
PC8
PC9
PC10
PC11
DIGITAL GND
1
14
2
15
3
16
4
17
5
18
6
19
7
20
8
21
9
22
10
23
11
24
12
25
13
PARALLEL PORT
CONNECTOR DB25

POINTS OF INTEREST W.R.T. PARALLEL PORT:

As we can see from the pin configuration of the standard Parallel Port ,pin numbers 2 to 9 constitute the dedicated data lines i.e. D0 to D7 while pin numbers 1,14,16 and 17 are control lines which are used as output lines i.e. D8 to D11.Thus the maximum number of 12 output lines are being used to output data from the parallel port.

As the output from the thumbwheel is BCD which is sent as input to the EPLD Also we can see that in order to access pins 2 to 9 i.e. D0 to D7 we have to refer to the base address of the parallel port which is usually 0x278 or 0x378, in the computer which we have used the base address is 0x278. In order to access pins 1,14,16 and 17 we have to refer to its address which is (base address + 2) in Hexadecimal i.e. 0x27a. Next we see that the dedicated output lines D0 to D7 are sent out of the parallel port without being inverted while among the other four output lines , D8,D9 and D11 are sent out of parallel port after inversion and output line D10 is sent out of parallel port without any inversion.

The output of the parallel port is the binary equivalent of any decimal number, for eg. consider the following command in Borland C language ....

Outport (0x278,12);

The above command would output the binary equivalent of the decimal number 12 i.e. 00001100 to pins 2 to 9 (or D0 to D7 with pin 2 being the LSB and pin 9 being MSB). Now consider the following command in C language...

Outport (0x27a, 12);

Outport (0x27a, 1);

The first of the above commands would output the binary equivalent of the decimal number 12 but since the output from the pins 1,14 and 17 are inverted , the output from the

parallel port would be 0111 at pins 17,16,14 and 1 respectively. While the output of the parallel port for the second command would be 1010 at pins 17,16,14 and 1 respectively.

The Borland C compiler allows the usage of a variable to output the binary equivalent of the decimal number entered into the PC while on the other hand the compiler does not allow the usage of a variable to output the Hexadecimal of the decimal number entered into the PC. Consider for example the following C commands...

```
Int k;
k=11;
Outport (0x278,k); /* would output 00001011 */
Outport (0x278,0x11);/*would output 00010001 */
Outport (0x278,0xk);/*error */
```

As we would be dealing with numbers from 0 to 9 only, the Hexadecimal equivalent of any decimal number from 0 to 9 is same as the BCD equivalent of any decimal number.

As the input from the thumbwheel to the EPLD is the BCD of the decimal number entered on the thumbwheel, we decided to output the BCD of any decimal number entered on the PC from the parallel port to EPLD.

DATA ENTRY FROM THE PC:

We now have the task of sending the BCD equivalent of a decimal number entered into the PC. From the above section we know our limitations of the parallel port and that of the Borland C compiler.

The following are steps to be taken in writing the required C code:

1. Suppose the entered frequency value is 2324 MHz then the last digit namely 4 in this case has to be eliminated .
2. Now that we are left with 232 our next step is to separate 2 and 32 from 232 and store them in separate variables, say k=2 and l=32. This is done because the four control lines which are used as data lines can output the binary values of decimal numbers 0 to 15 only. That is to say the binary value of 'k' would be sent to the four data lines and on the other hand the binary value of 'm' would be sent to the eight dedicated data lines .
3. Next consider the following tables.

Table 1:

Entered decimal number	Binary output at pins								BCD output								Decimal number to be output whose binary equivalent maps with the required BCD of the entered decimal number
	9	8	7	6	5	4	3	2									
00	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
12	0	0	0	0	1	1	0	0	0	0	0	1	0	0	1	0	18
55	0	0	1	1	0	1	1	1	0	1	0	1	0	1	0	1	85
99	0	1	1	0	0	0	1	1	1	0	0	1	1	0	0	1	153

Table 2:

Entered decimal number	Output at pins				Decimal number to be output whose binary equivalent maps with the required BCD of the entered decimal number
	17	16	14	1	
0	1	0	1	1	11
1	1	0	1	0	10
2	1	0	0	1	9
3	1	0	0	0	8
4	1	1	1	1	15
5	1	1	1	0	14
6	1	1	0	1	13
7	1	1	0	0	12
8	0	0	1	1	3
9	0	0	1	0	2

From Table 1 we can see that if the entered decimal number is 'k' then the decimal number to be output whose binary equivalent maps with the required BCD of the entered decimal number takes the form (k*16+k%10),say i=(k*16+k%10).Therefore, 'i' has to be output to the parallel port.

From Table 2 we can see that if the entered decimal number is 'm' and if 'm' lies between 4 and 7 then the decimal number to be output whose binary equivalent maps with the required BCD of the entered decimal number takes the form (19-m), say j=(19-m). Therefore, 'j ' has to be output to the parallel port if 'm' lies between 4 and 7.Now if the entered decimal number 'm' is any of the following 0,1,2,3,8 and 9 then the decimal number to be output whose binary equivalent maps with the required BCD of

the entered decimal number takes the form (11-m), say x=(19-m). Therefore, 'x ' has to be output to the parallel port if 'm' is any of the following 0,1,2,3,8 and 9.

Thus we see that if we output 'i' to parallel port base address 0x278 and if we output 'm' to address 0x27a we get the binary output which maps to the required BCD of the entered decimal number i.e. $(232)_{10}=(001000110010)_{BCD}$. The corresponding C commands are:

```
Outport(0x278,i);/*outputs 00110010 */
Outport(0x27a,m);/* outputs 0010 */
```

Necessity of Parallel Port

Apart from the parallel port we have the serial port, which also very widely used. For our application the DAC should receive all the ten inputs at the same time for proper operation of the DAC. In case of the serial port, data is output serially only through one pin, which should not be given to the DAC directly. We can still use the serial port by using shift registers in the serial-in parallel-out mode of operation, by doing so we can give all the ten inputs to the DAC at the same time. On the other hand, the parallel port can be made to give out a maximum of twelve outputs, all at the same time. Thus, in order to avoid unnecessary circuit designing the parallel port is used instead of the serial port.

CHAPTER-VI

DATA ACQUISITION USING GENERAL PURPOSE INTERFACE BUS (GPIB)

GENERAL PURPOSE INTERFACING BUS (G.P.I.B)

The G.P.I.B. is a link or an interface system, through which interconnected electronic devices communicate.

The original G.P.I.B. was designed by Hewlett-Packard (where it is called as H.P.I.B) to connect and control programmable instruments manufactured by H.P. The G.P.I.B. because of its high data transfer rate quickly gained popularity in other applications such as inter-computer communication and peripheral control. It was later accepted as the industry standard IEEE-488.The versatility of the system prompted the name General Purpose Interfacing Bus. The G.P.I.B and H.P.I.B. are the two brand versions of the same IEEE-488 standard.

The G.P.I.B. is a carefully designed defined general-purpose digital interface system. It minimizes the electrical/mechanical hardware and functional compatibility problems between the devices, yet has sufficient flexibility to accommodate a wide and growing range of products. As such G.P.I.B. is an interfacing concept and a design technique. You can take advantage of these concepts to define, design, build and use your own measurement system for maximum cost effectiveness. It's more than an interface; it's a design philosophy.

Overview:

* The Hewlett-Packard Interface Bus (HPIB) is a strictly-defined general-purpose computer interface system, in effect an external computer bus that allows interconnection of instruments and other devices to a controlling computer. General specifications of HPIB include:

- A bus configuration will consist of a single Active Controller (though on occasions several controllers may reside on the same bus and "pass control" among each other)

and one or more devices that can be instructed to "talk" or "listen" as instructed by the controller.

- Fifteen devices may be connected to one continuous bus.
- Total transmission path lengths over the interconnecting cables does not exceed 20 meters or 2 meters per device, whichever is less (when not using a bus extension technique).
- Data rate across the interface does not exceed 1 megabyte per second. (This data rate is rarely achieved in practice.)

Key Specifications Of IEEE 488.1 :

- Interconnected devices: Up to 15 maximum on one contiguous bus.
- Interconnection path: Star or linear (or mixed) bus network, up to 20 meters total transmission path length.
- Signal lines: 16 active lines, consisting of 8 data lines and 8 communications management lines.
- Message transfer scheme: Byte-serial, bit-parallel, asynchronous data transfer using an interlocking 3-wire handshake.
- Maximum data rate: 1 megabyte per second over limited distances, 250 to 500 kilobytes per second typical maximum over a full transmission path. The actual data rate is determined by the devices on the bus.

- Address capability: Primary addresses, 31 Talk and 31 Listen; secondary addresses, 961 Talk and 961 Listen. There can be a maximum of 1 Talker and up to 14 Listeners at a time on a single bus.
- Pass control: In systems with more than one controller, only one can be active at a time. The currently active controller can pass control to one of the others. A non-active controller may request control. Only the controller designated as System Controller can demand control.
- Interface Circuits: Driver and receiver circuits are TTL and Schottky compatible.

HPIB Functions & Capabilities:

* The operation of the HPIB can be compared to that of a committee. A committee chairman controls which member talks and implies that the others should listen. IEEE 488.1 has one device that controls, deciding who talks and who listens (under normal circumstances the controlling device will be one half of the conversation, but it doesn't have to be). Every IEEE 488.1 device must be capable of performing one or more of the following interface functions:

- **Listener**: A device capable of receiving data over the interface when addressed to Listen by the Active Controller. Examples of such devices are printers, programmable power supplies, or any other programmable instrument. There can be up to 14 Listeners on the HPIB at one time; usually the Active Controller will be a Talker while a single device is a Listener.
- **Talker**: A device capable of transmitting data over the interface when addressed to Talk by the Active Controller. Examples of such devices are voltmeters, data-

acquisition systems, or any other programmable instrument. There can be only one addressed Talker on the HPIB at one time. Usually the Active ontroller will be a Listener while a device is a Talker.

- **Controller:** A device capable of specifying the Talker and Listeners for a data or command transfer. Note that the Active Controller will be configured as Listener or Talker to support its end of the transfer. There can be only one addressed controller on the interface at one time; in multiple controller systems active control may be passed between controllers, but only one can be a master "System Controller".

GPIB Lines:

The GPIB consists of 24 lines, which are shared by all instruments connected to the bus. 16 lines are used for signals, while 8 lines are for ground. The signal lines are divided into these groups:

- Eight data lines
- Five interface management lines
- Three handshake lines

The signal lines use a low-true (negative) logic convention with TTL levels. This means that a line is low (true or asserted) when it is a TTL low level, and a line is high (false or unasserted) when it is a TTL high level. The pin assignment scheme for a GPIB connector is shown below.

The pins and signals associated with the GPIB connector are described below.

Table 3-1: GPIB Pin and Signal Assignments

Pin	Label	Signal Name	Pin	Label	Signal Name
1	DIO1	Data transfer	13	DIO5	Data transfer
2	DIO2	Data transfer	14	DIO6	Data transfer
3	DIO3	Data transfer	15	DIO7	Data transfer
4	DIO4	Data transfer	16	DIO8	Data transfer
5	EOI	End Or Identify	17	REN	Remote Enable
6	DAV	Data Valid	18	GND	DAV ground
7	NRFD	Not Ready For Data	19	GND	NRFD ground
8	NDAC	Not Data Accepted	20	GND	NDAC ground
9	IFC	Interface Clear	21	GND	IFC ground
10	SRQ	Service Request	22	GND	SRQ ground
11	ATN	Attention	23	GND	ATN ground
12	Shield	Chassis ground	24	GND	Signal ground

Data Lines:

The eight data lines, DIO1 through DIO8, are used for transferring data one byte at a time. DIO1 is the least significant bit, while DIO8 is the most significant bit. The transferred data can be an instrument command or a GPIB interface command.

Data formats are vendor-specific and can be text-based (ASCII) or binary. GPIB interface commands are defined by the IEEE 488 standard.

Interface Management Lines

The interface management lines control the flow of data across the GPIB interface, and are described below.

Table 3-2: GPIB Interface Management Lines

Line	Description
ATN	Used by the Controller to inform all devices on the GPIB that bytes are being sent. If the ATN line is high, the bytes are interpreted as an instrument command. If the ATN line is low, the bytes are interpreted as an interface message.
IFC	Used by the Controller to initialize the bus. If the IFC line is low, the Talker and Listeners are unaddressed, and the System Controller becomes the Controller-In-Charge.
REN	Used by the Controller to place instruments in remote or local program mode. If REN is low, all Listeners are placed in remote mode, and you cannot change their settings from the front panel. If REN is high, all Listeners are placed in local mode.
SRQ	Used by Talkers to asynchronously request service from the Controller. If SRQ is low, then one or more Talkers require service (for example, an error such as invalid command was received). You issue a serial poll to determine which Talker requested service. The poll automatically sets the SRQ line high.
EOI	If the ATN line is high, the EOI line is used by Talkers to identify the end of a byte stream such as an instrument command. If the ATN line is low, the EOI line is used by the Controller to perform a parallel poll (not supported by the toolbox).

Handshake Lines:

The three handshake lines, DAV, NRFD, and NDAC, are used to transfer bytes over the data lines from the Talker to one or more addressed Listeners.

Before data is transferred, all three lines must be in the proper state. The active Talker controls the DAV line and the Listener(s) control the NRFD and NDAC lines. The handshake process allows for error-free data transmission. The handshake lines are described below.

Table 3-3: GPIB Handshake Lines

Line	Description
DAV	Used by the Talker to indicate that a byte can be read by the Listeners.
	Indicates whether the Listener is ready to receive the byte.
NDAC	Indicates whether the Listener has accepted the byte.

The handshaking process follows these steps:

1. Initially, the Talker holds the DAV line high indicating no data is available, while the Listeners holds the NRFD line high and the NDAC line low indicating it is ready for data and no data is accepted, respectively.

2. When the Talker puts data on the bus, it sets the DAV line low, which indicates that the data is valid.

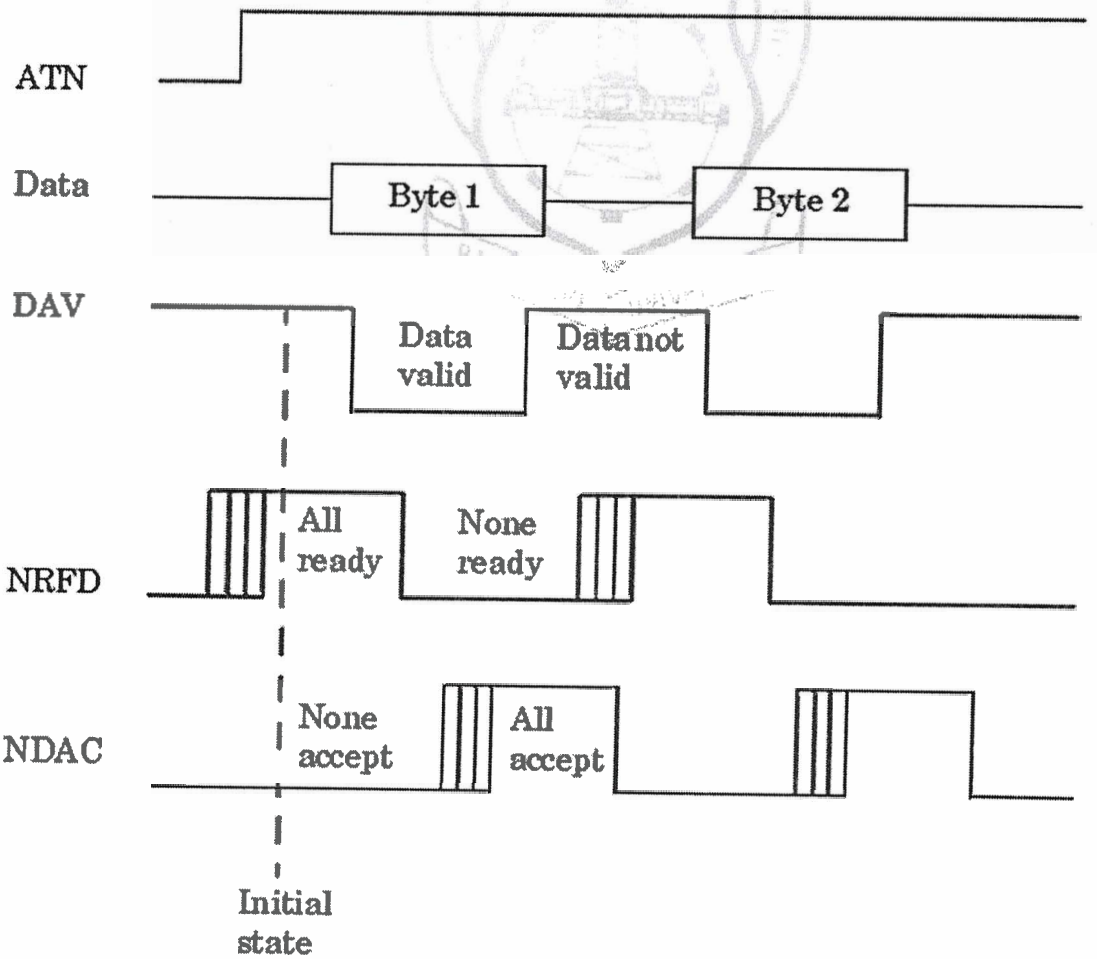
3. The Listeners set the NRFD line low, which indicates that they are not ready to accept new data.

4. The Listeners set the NDAC line high, which indicates that the data is accepted.

5. When all Listeners indicate that they have accepted the data, the Talker asserts the DAV line indicating that the data is no longer valid. The next byte of data can now be transmitted.

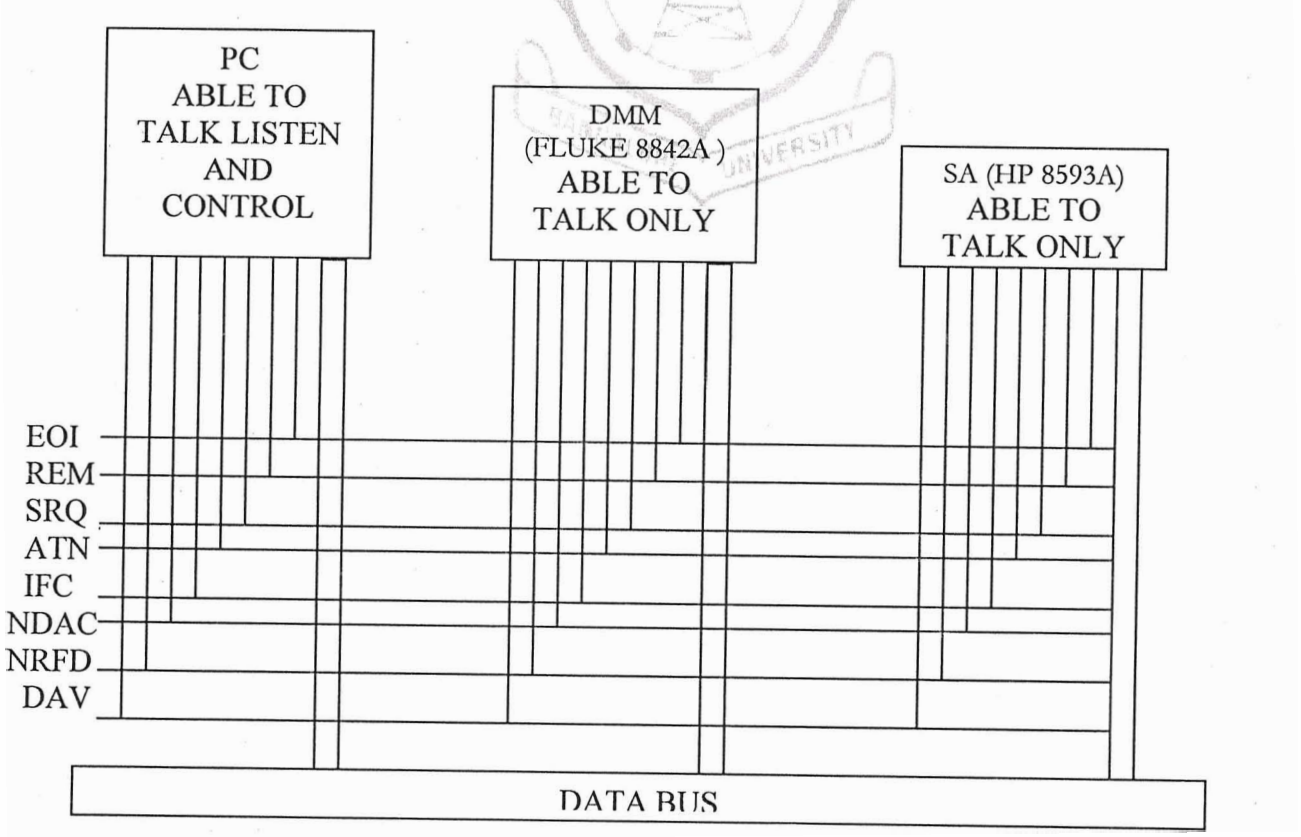
6. The Listeners hold the NRFD line high indicating they are ready to receive data again, and the NDAC line is held low indicating no data is accepted.

The handshaking waveform are shown below.



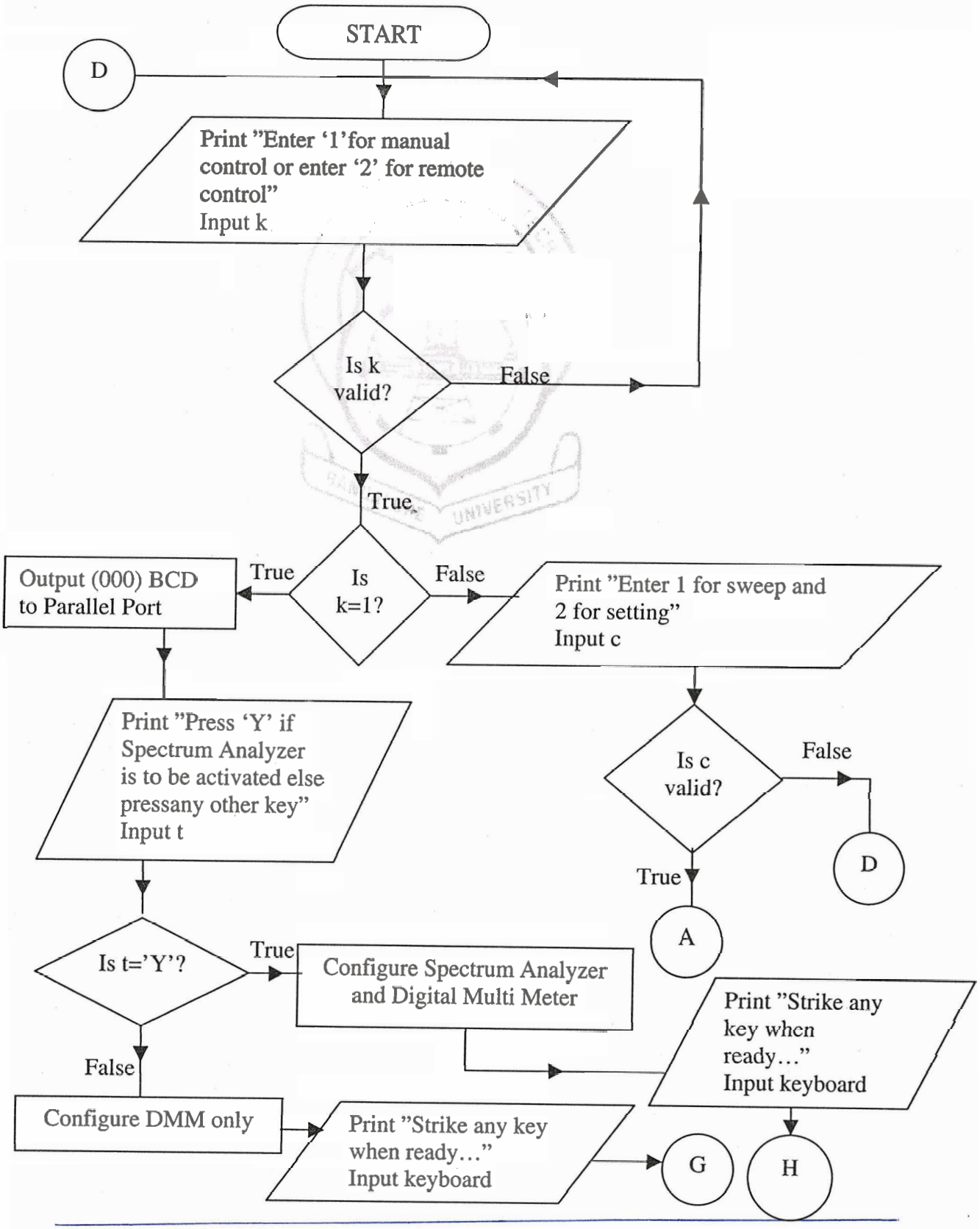
GPIB Set Up

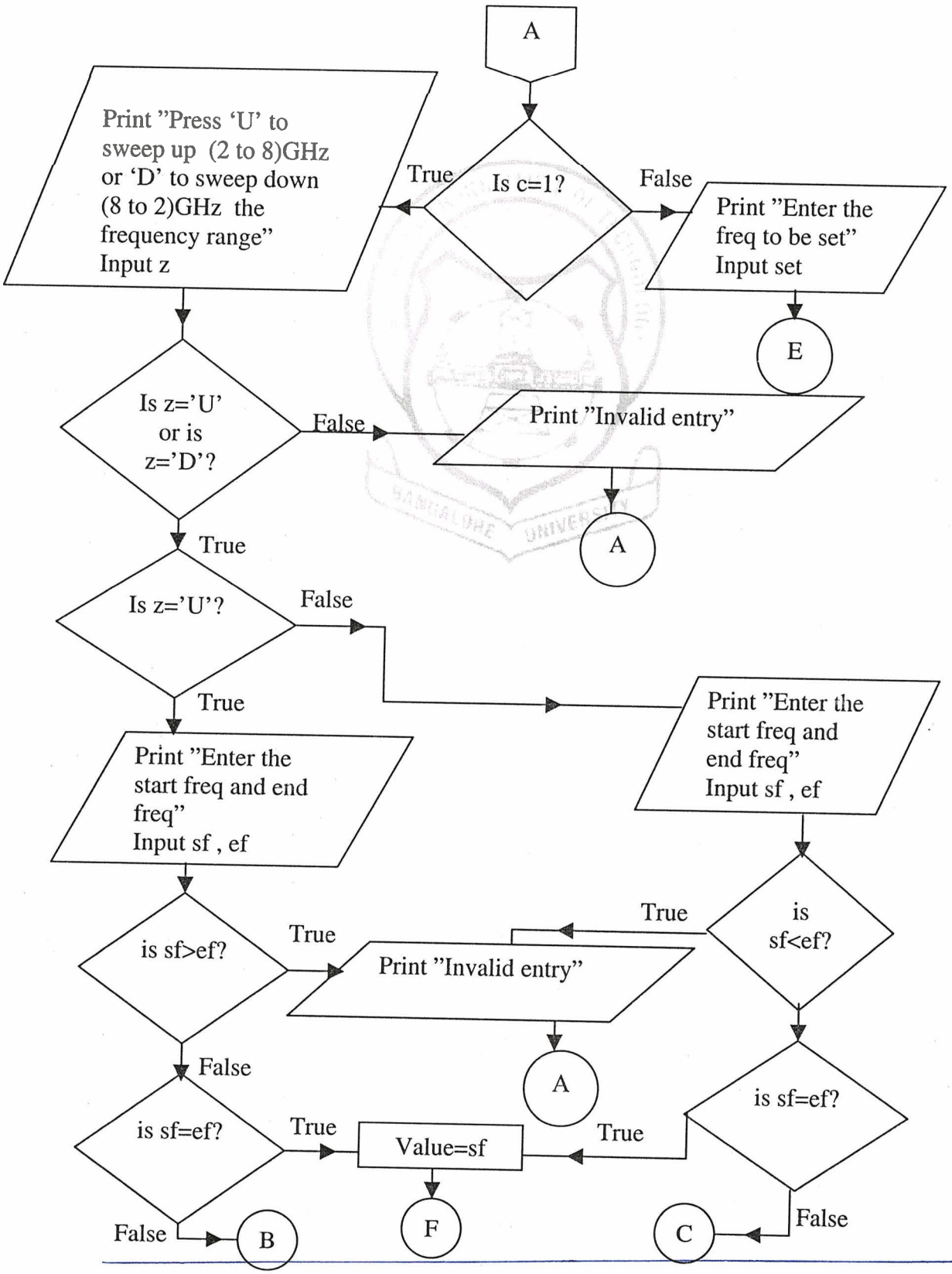
The figure below shows us the GPIB set up which is used in the project . As the digital multi meter and the spectrum analyzer measure the voltage across the reference resistor and the output frequency, power respectively they are categorized as " TALK " instruments. On the other hand the PC which configures the digital multi meter and the spectrum analyzer and also acts as the storage place for the values being measured it is categorized as "CONTROLLER".

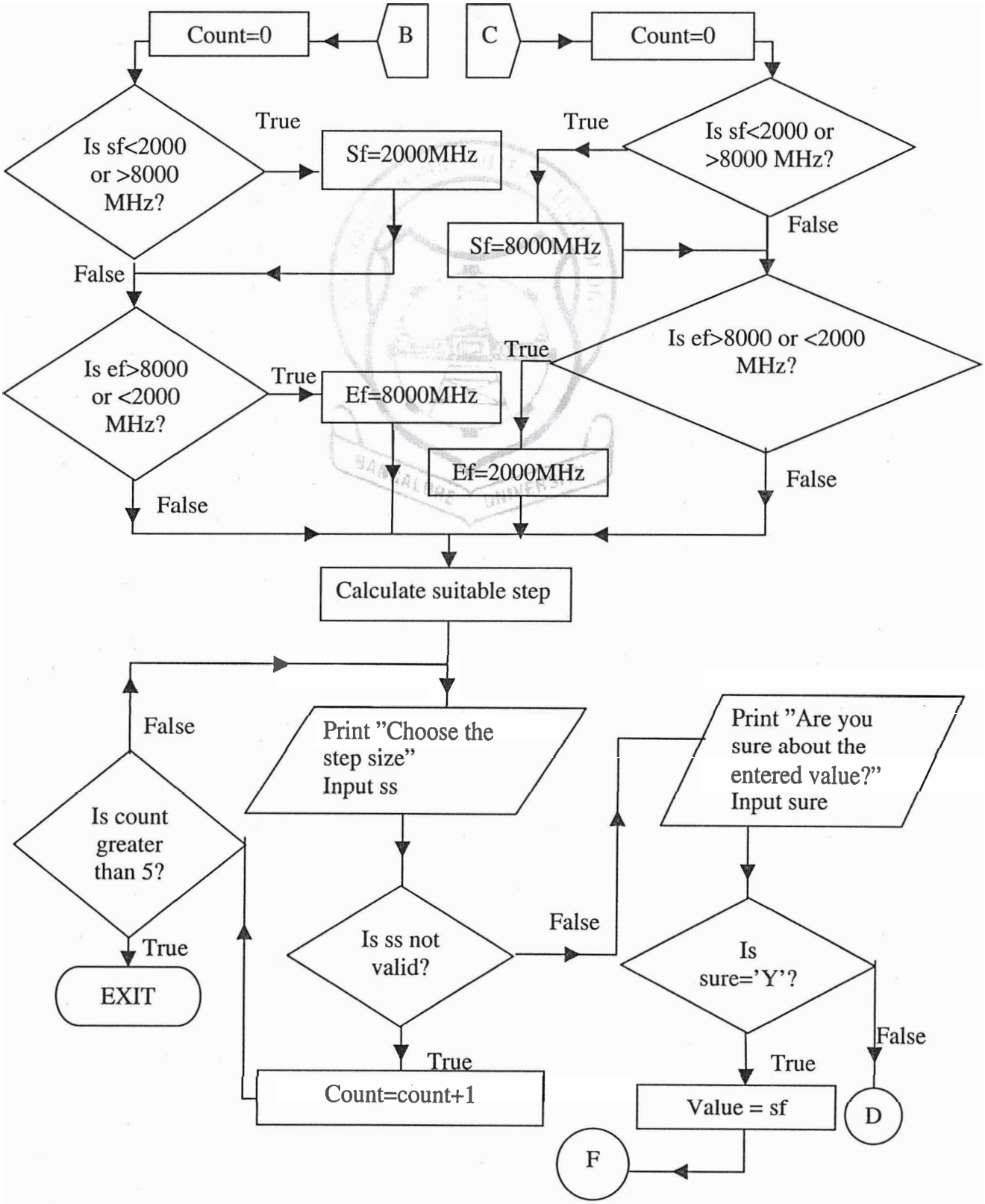


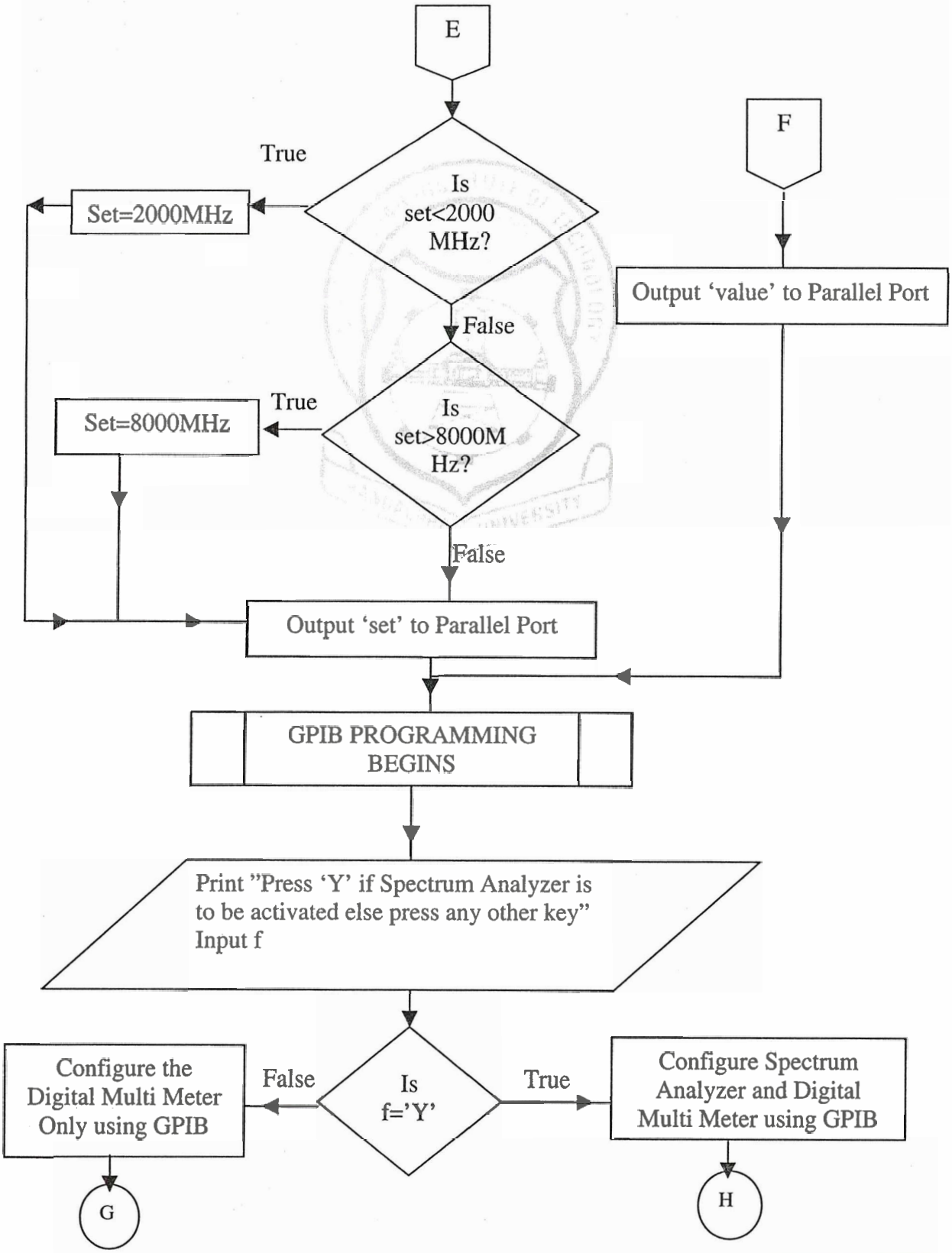
CHAPTER-VII

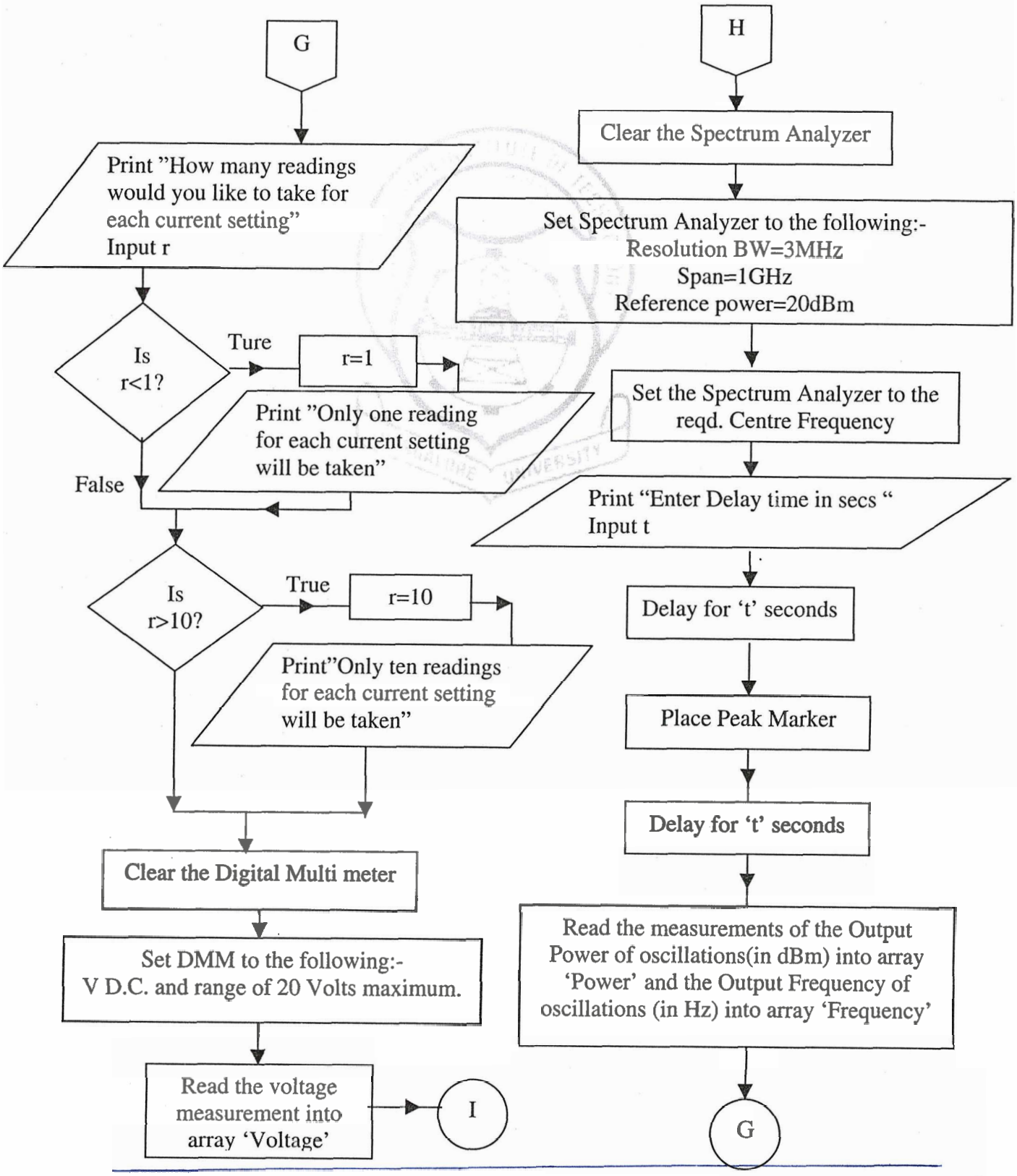
PROGRAMMING AND FLOW CHARTS

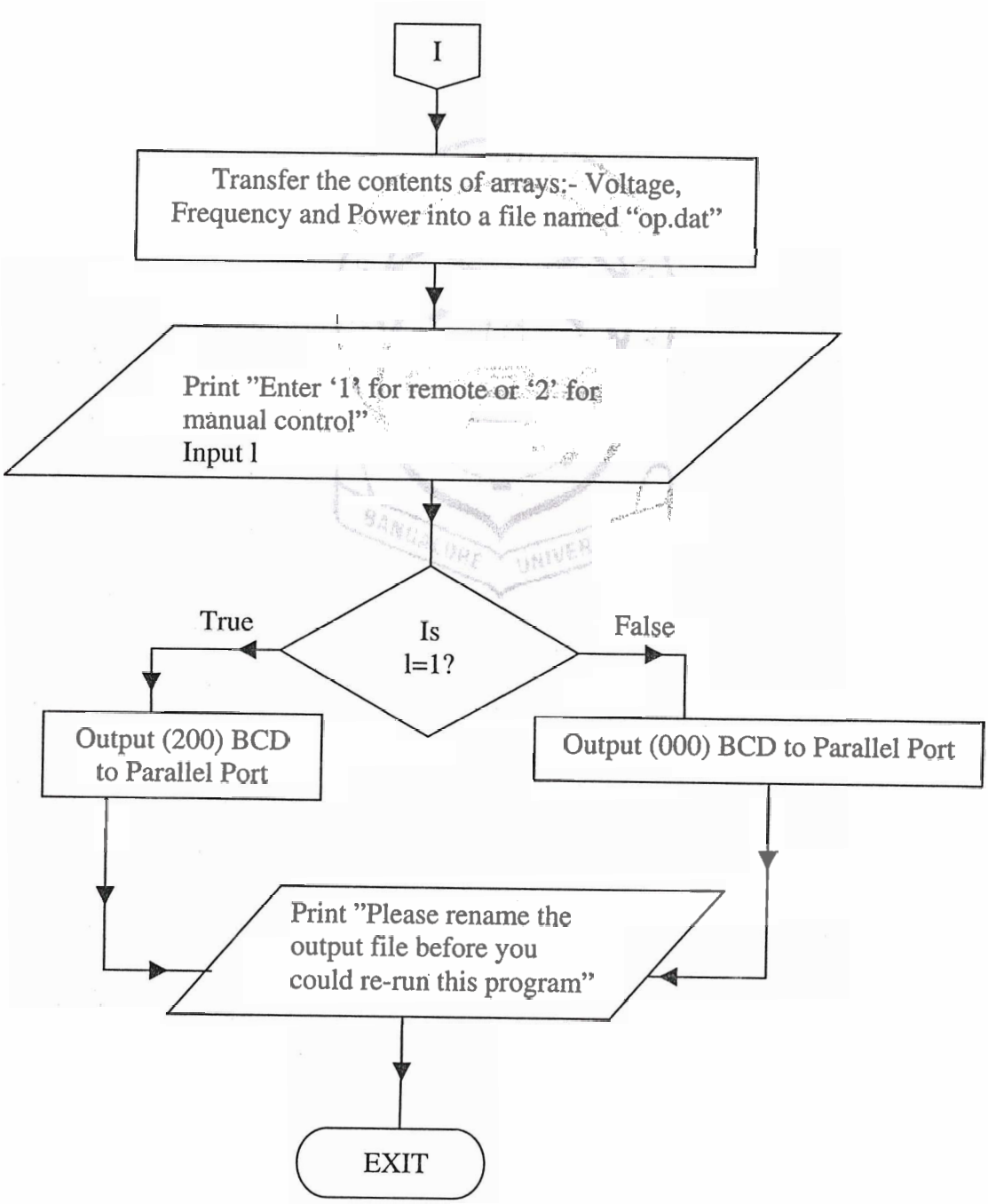

START
D
Print "Enter '1' for manual control or enter '2' for remote control"
Input k
Is k valid?
False
True
Is k=1?
True
False
Output (000) BCD to Parallel Port
Print "Enter 1 for sweep and 2 for setting"
Input c
Print "Press 'Y' if Spectrum Analyzer is to be activated else pressany other key"
Input t
Is c valid?
False
D
True
A
Is t='Y'?
True
Configure Spectrum Analyzer and Digital Multi Meter
Print "Strike any key when ready..."
Input keyboard
False
Configure DMM only
Print "Strike any key when ready..."
Input keyboard
G
H


A
Is c=1?
True
False
Print "Press 'U' to sweep up (2 to 8)GHz or 'D' to sweep down (8 to 2)GHz the frequency range" Input z
Print "Enter the freq to be set" Input set
E
Is z='U' or is z='D'?
False
Print "Invalid entry"
A
True
Is z='U'?
False
True
Print "Enter the start freq and end freq" Input sf , ef
Print "Enter the start freq and end freq" Input sf , ef
is sf>ef?
True
Print "Invalid entry"
True
is sf<ef?
False
A
is sf=ef?
True
Value=sf
True
is sf=ef?
False
B
F
C
False


Count=0
B
C
Count=0
Is sf<2000 or >8000 MHz?
True
Sf=2000MHz
True
Is sf<2000 or >8000 MHz?
False
Sf=8000MHz
False
Is ef>8000 or <2000 MHz?
True
Ef=8000MHz
True
Is ef>8000 or <2000 MHz?
Ef=2000MHz
False
False
Calculate suitable step
False
Print "Choose the step size" Input ss
Print "Are you sure about the entered value?" Input sure
Is count greater than 5?
Is ss not valid?
False
Is sure='Y'?
True
EXIT
True
Count=count+1
True
Value = sf
False
D
F


E
F
True
Is set<2000 MHz?
Set=2000MHz
Output 'value' to Parallel Port
False
Is set>8000M Hz?
True
Set=8000MHz
False
Output 'set' to Parallel Port
GPIB PROGRAMMING BEGINS
Print "Press 'Y' if Spectrum Analyzer is to be activated else press any other key"
Input f
Is f='Y'
False
True
Configure the Digital Multi Meter Only using GPIB
Configure Spectrum Analyzer and Digital Multi Meter using GPIB
G
H


G
Print "How many readings would you like to take for each current setting"
Input r
Is r<1?
Ture
r=1
Print "Only one reading for each current setting will be taken"
False
Is r>10?
True
r=10
Print"Only ten readings for each current setting will be taken"
Clear the Digital Multi meter
Set DMM to the following:-
V D.C. and range of 20 Volts maximum.
Read the voltage measurement into array 'Voltage'
I
H
Clear the Spectrum Analyzer
Set Spectrum Analyzer to the following:-
Resolution BW=3MHz
Span=1GHz
Reference power=20dBm
Set the Spectrum Analyzer to the reqd. Centre Frequency
Print "Enter Delay time in secs "
Input t
Delay for 't' seconds
Place Peak Marker
Delay for 't' seconds
Read the measurements of the Output Power of oscillations(in dBm) into array 'Power' and the Output Frequency of oscillations (in Hz) into array 'Frequency'
G


I
Transfer the contents of arrays:- Voltage, Frequency and Power into a file named "op.dat"
Print "Enter '1' for remote or '2' for manual control"
Input l
Is l=1?
True
False
Output (200) BCD to Parallel Port
Output (000) BCD to Parallel Port
Print "Please rename the output file before you could re-run this program"
EXIT

FUNCTIONS USED IN C PROGRAM

Below is the list of functions apart from the function main( ) used in the C code.

int check( );	/*TO CHECK IF ENTERED CHOICE IS CORRECT*/
int dataentry( );	/* DATA IS ENTERED IN THIS FUNCTION */
void limiter ( );	/* LIMITS THE DATA ENTERED IN BETWEEN THE FREQUENCY REGION 2 GHz TO 8GHz */
int stepsize ( );	/* CALCULATES THE STEPSIZE FOR THE ENTERED RANGE OF FREQUENCIES TO BE SWEPT */
int choice ( );	/* DISPLAYS A SET OF 5 VALUES OF STEPSIZE */
int assignss( );	/* ASSIGNS THE STEPSIZE CHOOSEN TO SUITABLE VARIABLE */
void configure ( );	/* CONFIGURES THE SPECTRUM ANALYZER AND DIGITAL MULTIMETER OR ONLY THE DIGITAL MULTIMETER AS PER THE USER'S REQUIREMENTS */
void sweepm( );	/* SWEEPS ACROSS THE SET RANGE OF FREQUENCIES */
void setm( );	/* SETS THE FREQUENCY AS CHOOSEN BY THE USER */
int flukeset ( );	/* INTERFACES WITH THE DIGITAL MULTIMETER AND SETS THE NUMBER OF READINGS THE MULTIMETER HAS TO TAKE */
void fluke ( );	/* INTERFACES WITH THE DIGITAL MULTIMETER AND STORES THE READINGS OF THE MULTIMETER INTO AN ARRAY NAMELY "VOLTAGE" */

```
void saa ();          /* INTERFACES WITH THE SPECTRUM ANALYZER
                      AND STORES THE READINGS OF THE MARKER
                      FREQUENCY AND MARKER AMPLITUDE INTO TWO
                      SEPARATE ARRAYS NAMELY "FREQUENCY" AND
                      "POWER" */

void store();         /* TRANSFERS THE CONTENTS OF THE THREE
                      ARRAYS INTO A FILE NAMED "OP.DAT" */

void fordelay ();     /* AS THE BUILT IN FUNCTION DELAY() IS NOT
                      COMPATABLE WITH GPIB PROGRAMMING, A FOR
                      LOOP IS USED AS A DELAY FUNCTION */
```

SAMPLE GPIB PROGRAM

Below is a sample GPIB program. Similar logic is used in writing the C code for the program developed in the project.

```
#include <stdio.h>
#include<ctype.h>
#include <dos.h>
#include"c:\at-gpibw\c\windecl.h"
#include <math.h>
#include <conio.h>


void main( )
{
int j,i,r,mm, sig=5;
char reading[30], read[30],str[30],str1[30],str2[30],read1[30];

float cf,db,csum,current[600],mf[600],mka[600],value,temp,temp1;

 /*READING VALUES FROM DMM */

mm=ibdev(0,1,0,T3s,1,0); /*Configuring the Digital Multi meter the Digital
                           Multi meter has a primary address=01 */

 printf("\nHow many readings would you like to take for each current
                           setting\n");
 scanf("%d",&r);
if (r<1)
{
 r=1;
 printf("\nOnly one reading for each current setting will be taken");
}
if(r>10)
{
r=10;
printf("\nOnly ten readings for each current setting will be taken");
```

```
}
ibclr(mm); /* Clears the device registers and all the previous settings */
ibwrt(mm,"F1\r\n",4L);  /* Sets the Digital Multi Meter to read D.C. Voltage */
ibwrt(mm,"R3\r\n",4L);  /* Sets the Digital Multi Meter to read a maximum
                           D.C. Voltage of 20 Volts */
csum=0;
for (j=1;j<=r;j++)
{
 ibrd(mm,reading,14L); /* Measures the voltage reading into character array
                          'reading' as the data measured by the digital multi
                          meter is sent to the PC in string format */
 reading[ibcnt]='\0'; /* Terminate the string with a 'NULL' pointer */
 printf("\nData read : %s     in round %d \n ",reading,j);
 csum+=atof(reading); /* the data read is converted into float data type by using
                         the Borland CPP compiler's built in function 'atof( )' */
}
current[i]=csum/(r); /* the average is calculated and stored in the array */


/* READING VALUES FROM THE SPECTRUM ANALYZER */
int sig;
sa=ibdev(0,18,0,T3s,1,0); /*Configuring the Spectrum Analyzer the Spectrum
                            Analyzer has a primary address=18 */
value1=(*value);
 printf("\n Enter the center frequency in MHz\n");
 scanf("%f",&value);
 strcpy(str1,"CF"); /* As the Spectrum Analyzer takes in commands only in
                       string format ,we have to do string manupulation  to set
                       the  center frequency of the spectrum analyzer */
 strcpy(str2,"MHZ");
 gcvt(value,sig,str); /* The built in function 'gcvt( )' converts float value to
                         corresponding string */
 strncat(str1,str,5);
 strncat(str1,str2,3);
 ibclr(sa); /* Clears the device registers and all the previous settings */
 ibwrt(sa,str1,9L); /* Sets the Spectrum Analyzer to the
                       entered center frequency*/
```

```
ibwrt(sa,"RL20DB",6L); /* Sets the Spectrum Analyzer to a
                          reference power of 20dB */
ibwrt(sa,"SP1GHz",6L); /* Sets the Spectrum Analyzer to a span of 1GHz */
fordelay(&time); /* Calls for a delay operation as the spectrum analyzer needs
                    some time to get set for measurements ( usually the delay
                    is around 4 to 5 seconds )*/
ibwrt(sa,"MKPK",4L); /* Sets the marker to the peak value of the signal */
fordelay(&time1); /* Calls for a delay operation as the spectrum analyzer needs
                     some time to get set for measurements */
ibwrt(sa,"MKA?\r\n",6L); /* Asks the spectrum analyzer to measure the
                            amplitude of the signal on which the
                            marker is on */
ibrd(sa,read1,5L); /* Reads in the measured amplitude in to string 'read1' */
ibwrt(sa,"MF?\r\n",5L); /* Asks the spectrum analyzer to measure the
                           frequency of the signal  on which the marker
                           is on */
ibrd(sa,read,8L); /* Reads in the measured frequency in to string 'read' */
temp=atof(read); /* Converts string format to corresponding float data type */
temp1=atof(read1); /* Converts string format to corresponding  float data
                      type*/

mf[i]=temp; /* Store the measured frequency value in an array */
mka[i]=temp1; /* Store the measured amplitude value into another array*/
printf("\n OUTPUT FREQUENCY: %d     OUTPUT POWER: %d
                                      \n",mf[i],mka[i]);
ibloc(mm); /* Places the digital multi meter  offline */
ibloc(sa); /* Places the spectrum analyzer offline */
}
```

CHAPTER-VIII

TESTS,MEASUREMENTS AND RESULTS

TEST RESULTS

Table 1 below are the values obtained of the output frequency(MHz) and the voltage across the reference resistor (volts). It also gives the values of the slope (volts/GHz), the average of the differences in voltages (volts) and the variations (volts) of the differences of voltages about the average of the differences in voltages.
(Refer graphs 1 and 2)

Table 1

Set Frequency (MHz)	Voltage Across Reference Resistor With YIG (Volts)	Difference in Voltages (Volts) V dn (Vn+1 – Vn)	Mean Frequency (MHz) (Fn+1 + Fn)/2	Slope (volts/ GHz)	Deviation in slope (mean slope =0.5515) Volts/GHz (Mean slope – slope)
2000	1.06	0.553	2500	0.553	0.0015
3000	1.613	0.5506	3500	0.5506	-0.0009
4000	2.1636	0.5508	4500	0.5508	-0.0007
5000	2.7144	0.5516	5500	0.5516	0.0001
6000	3.266	0.5514	6500	0.5514	-0.0001
7000	3.8167	0.5518	7300	0.5518	-0.0003
7600	4.1478				

The table 2 below are the values obtained of the measured output frequency(MHz) and the set frequency (MHz) for a step size of 1000 MHz. (Refer graphs 3 and 4)

Table 2

Set frequency (MHz)	Measured Frequency (MHz)	Difference between set and measured frequencies (MHz)
2000	1990	10
3000	3013	-13
4000	4022	-22
5000	5030	-30
6000	6038	-38
7000	7032	-32
7600	7592	8

The table 3 below are the values obtained of the measured output frequency(MHz) and the set frequency (MHz) for a step size of 100 MHz. (Refer graphs 5 and 6)

Table 3

Set frequency (MHz)	Measured frequency (MHz)	Difference between set and the measured frequencies (MHz)
2500	2507	-7
2600	2608	-8
2700	2710	-3
2800	2810	-2
2900	2910	-10
3000	3012	-12
3100	3112	-12
3200	3213	-13
3300	3313	-13
3400	3414	-14
3500	3515	-14
3600	3615	-15

The table 4 below are the values obtained of the measured output frequency(MHz) and the set frequency (MHz) for a step size of 10 MHz. (Refer graphs 7 and 8)

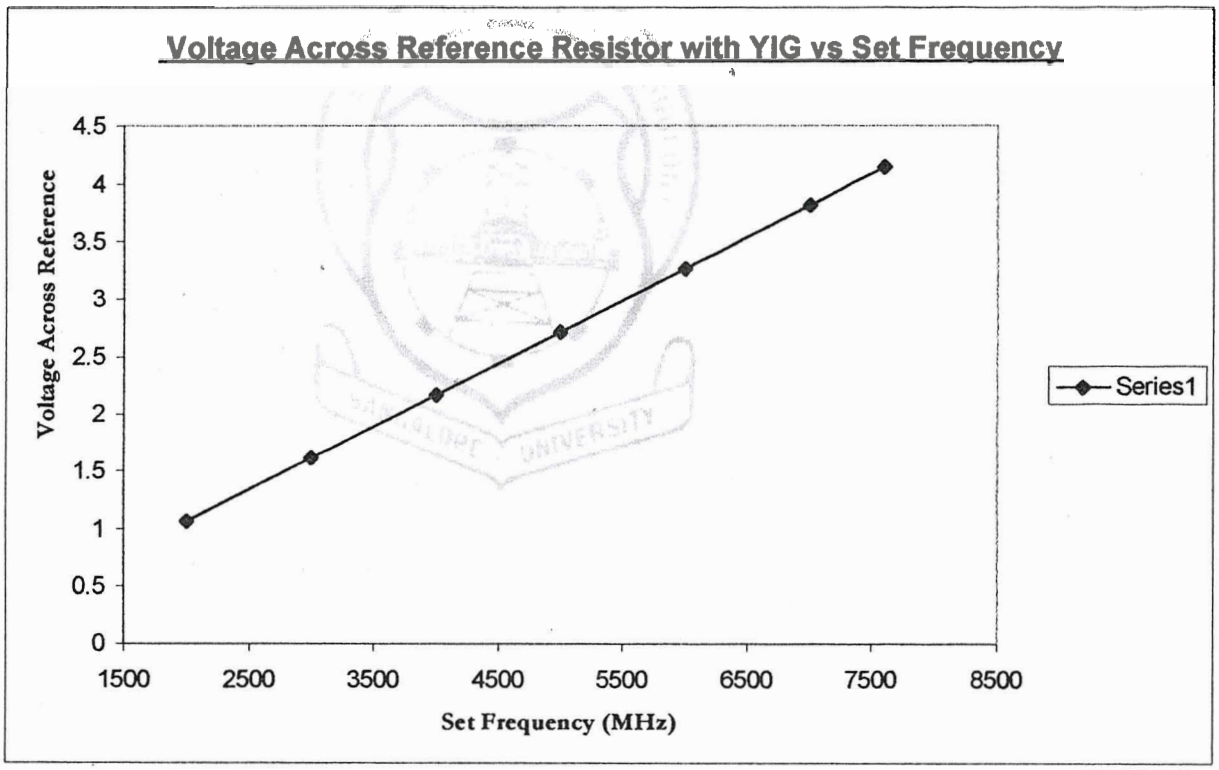
Table 4

Set frequency (MHz)	Measured frequency (MHz)	Difference in Set and measured frequencies (MHz)
2600	2607	-7
2610	2616	-6
2630	2638	-8
2640	2648	-8
2650	2657	-7
2660	2667	-7
2670	2677	-7
2680	2687	-7
2690	2697	-7

Table 5 below are the values obtained of the set frequency(MHz) and the voltage across the reference resistor (volts).

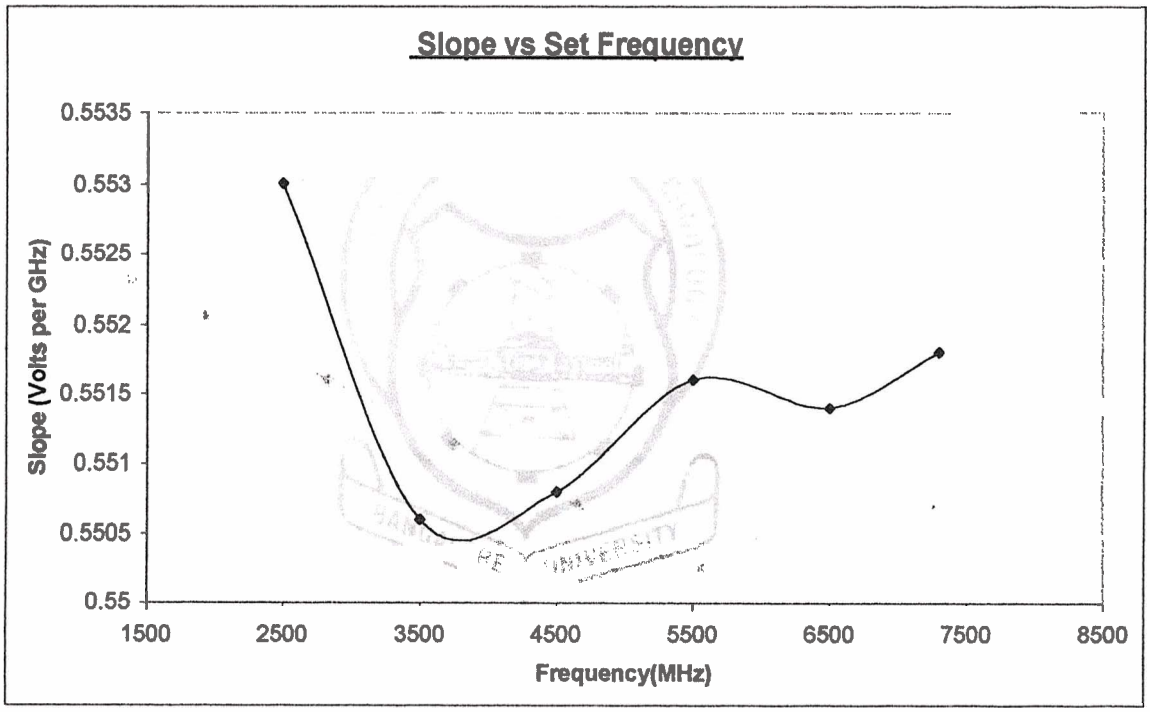
Table 5

Ste frequency(MHz)	Voltage across reference resistor (volts)
4800	2.7
4810	2.695
4820	2.7
4830	2.71
4840	2.71
4850	2.72
4860	2.725
4870	2.725
4880	2.735
4890	2.74
4900	2.74
4910	2.75
4920	2.76



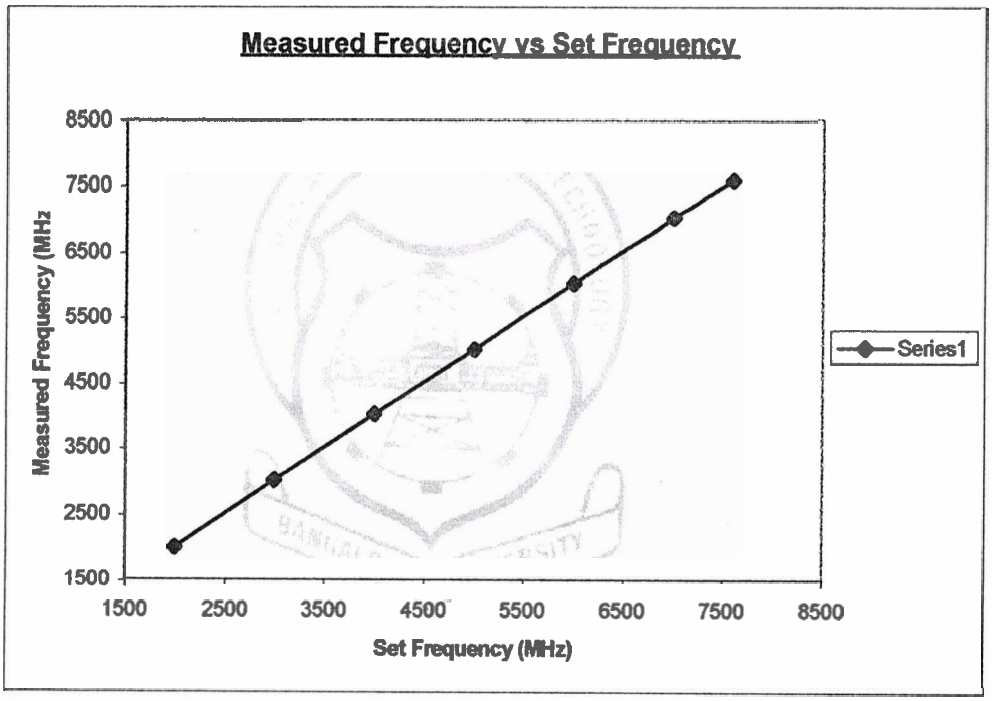
Graph 1

Graph 1 is a plot of voltage across the reference resistor as a function of set frequency with YIG having a step size of 1 GHz step size. From this graph we can conclude that the curve is as expected linear over the range of set range of frequencies having a nearly constant slope.



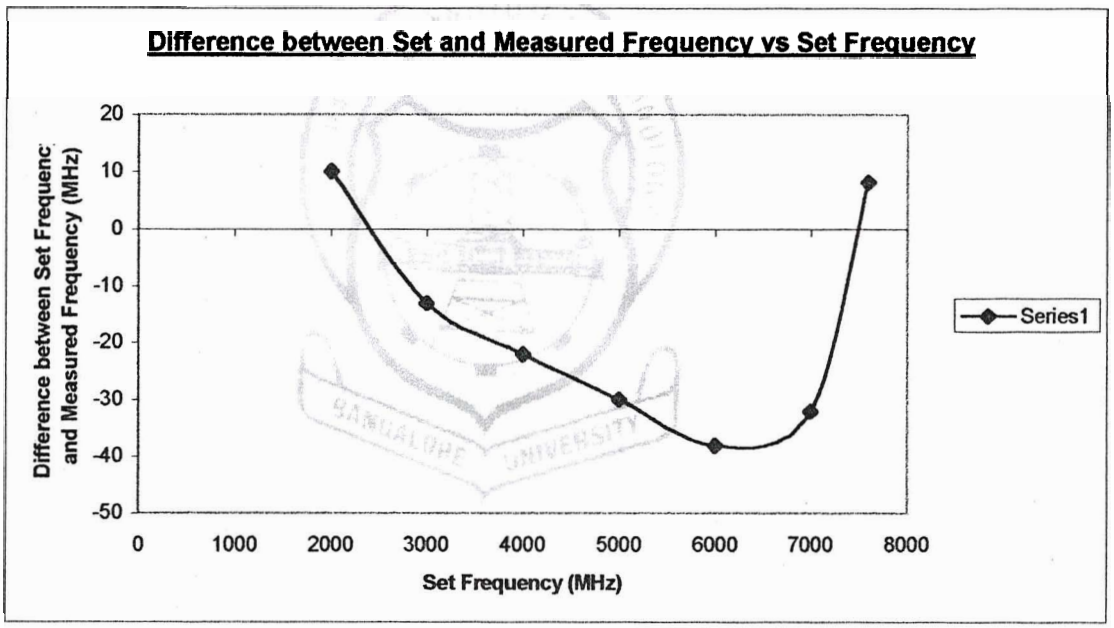
Graph 2

Graph 2 is a plot of the slope as a function of set frequency with a step size of 1 GHz. Ideally the curve should have been a parallel line along the x-axis with the ordinate value being the average value of 0.0015 volts. We see that the curve is nearly constant about the average value of 0.5515 volts/GHz. The maximum deviation from the average value is 0.0015 V which translates the average deviation from the set frequency about 1.5 MHz.



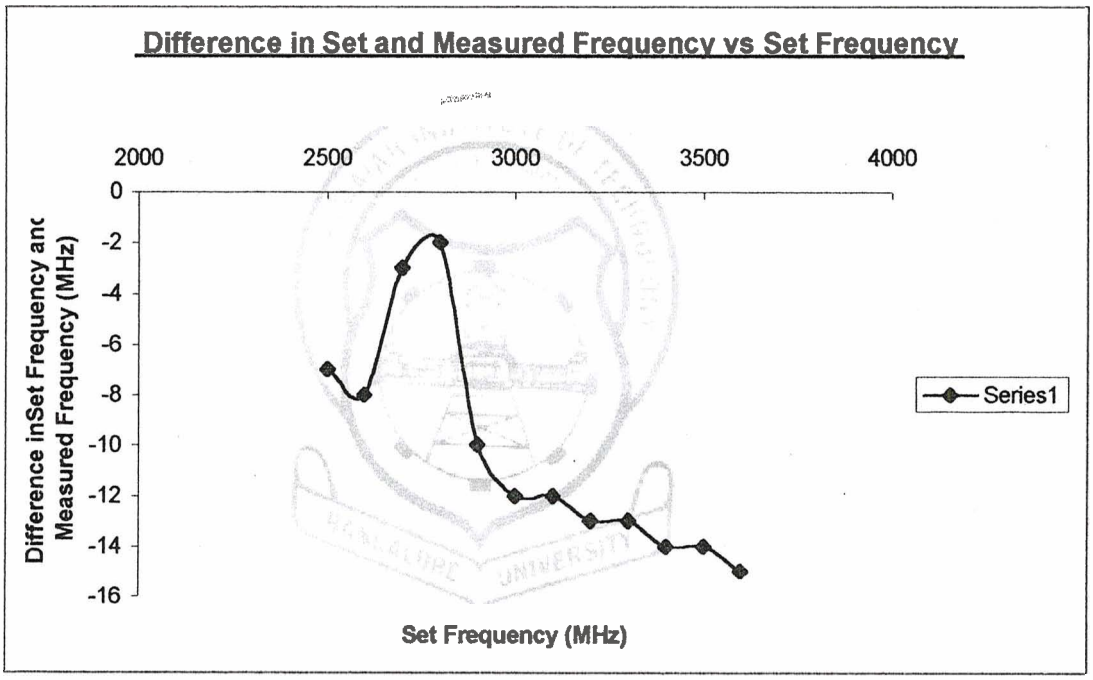
Graph 3

Graph 3 is a plot of measured frequency vs set frequency with 1 GHz step size. The curve should ideally be a straight line at an angle of 45 degrees. The obtained curve is very close to a straight line and at an angle of approximately 45 degrees having a nearly constant slope.



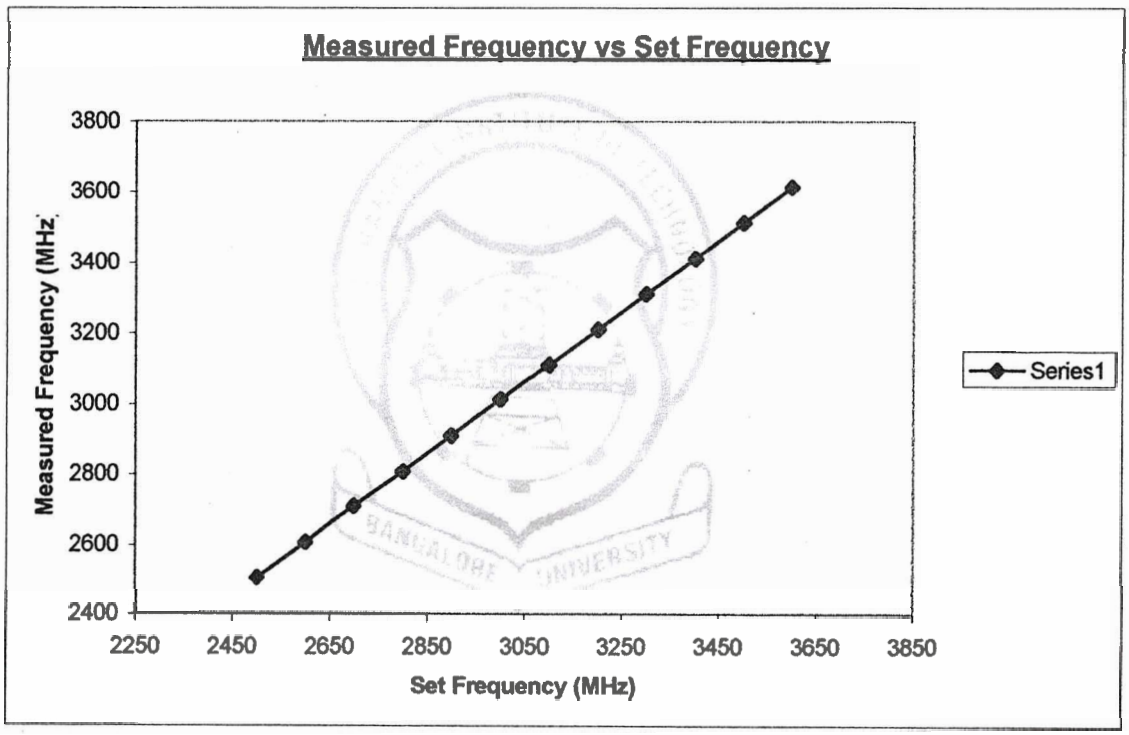
Graph 4

Graph 4 is a plot of deviation of measured frequency as a function of with 1 GHz step size. The expected curve is a straight line along the x-axis. The obtained curve has an average deviation of –16.71 MHz which can be reduced by adjusting the offset voltage. The average slope obtained is –2.98 % which can be reduced by adjusting the gain (decrease).



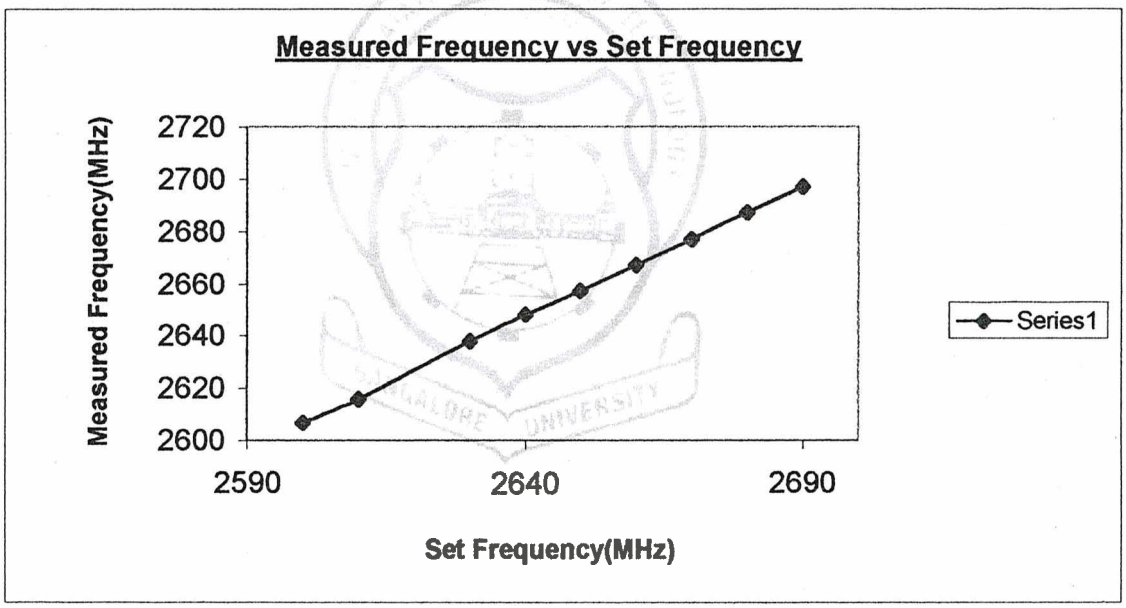
Graph 5

Graph 5 is a plot of deviation in the measured frequency as a function of set frequency over 1.1 GHz span from 2.5 to 3.6 GHz range with a step size of 100 MHz. The ideal curve should be a straight line along the x-axis. The obtained curve has an average deviation of –10.25 MHz which can be reduced by adjusting the offset voltage. Neglecting the third and fourth points the average slope obtained is -7.23 % which can be reduced by adjusting the gain (decrease).



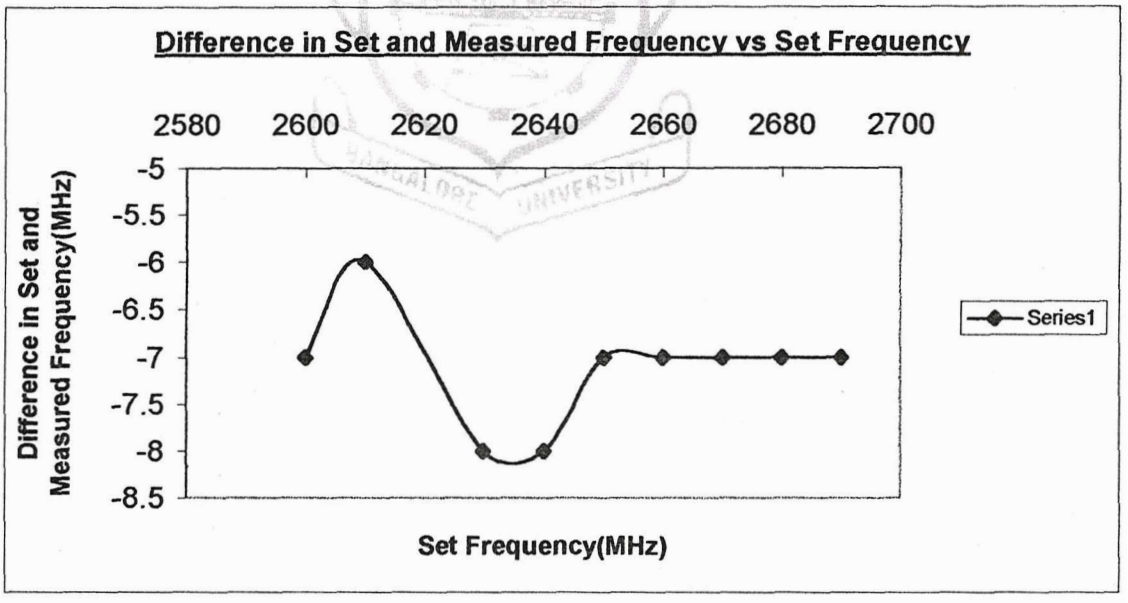
Graph 6

Graph 6 is a plot of set frequency vs the measured frequency with a step size of 100 MHz. the ideal curve should be a straight line at an angle of 45 degrees. The obtained curve is almost linear at an angle of approximately 45 degrees and having a nearly constant slope.



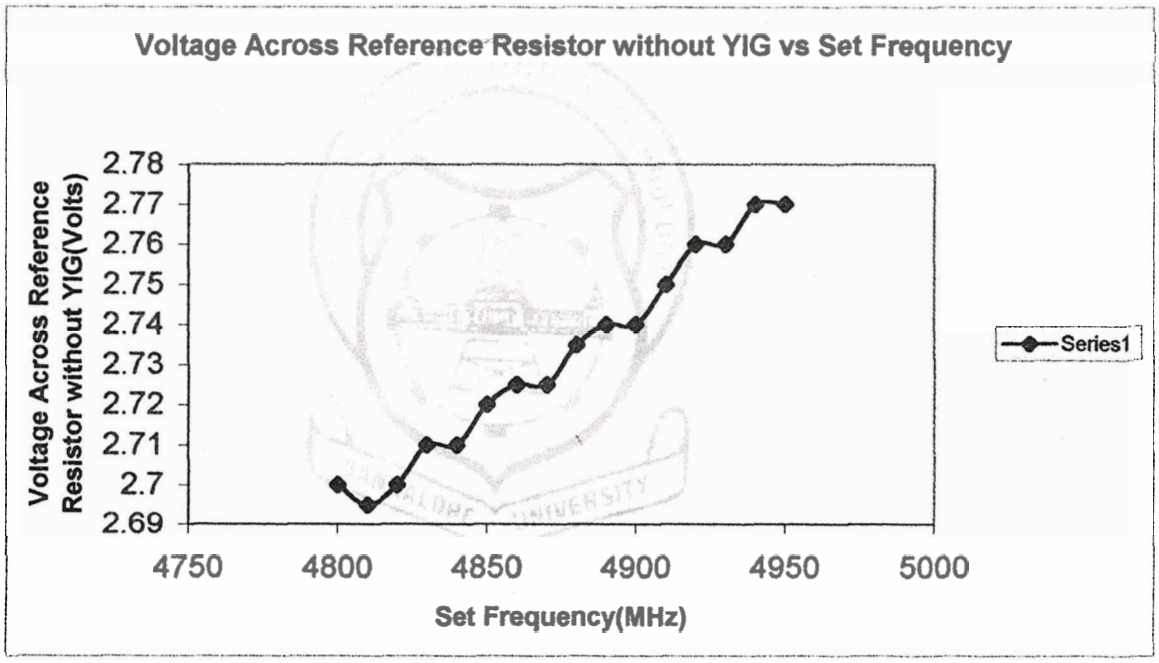
Graph 7

Graph 7 is a plot of measured frequency as a function of set frequency with a step size of 10 MHz. The ideal curve should be a straight line at an angle of 45 degrees. The obtained curve is close to being linear, at an angle of approximately 45 degrees and having a nearly constant slope.



Graph 8

Graph 8 is a plot of deviation in the measured frequency as a function of set frequency over 90 MHz span from 2600 to 2690 MHz range with a step size of 10 MHz. The ideal curve should be a straight line along the x-axis. The obtained curve has an average deviation of –7.11 MHz which can be reduced by adjusting the offset voltage. The average slope obtained is –7.9 % which can be reduced by adjusting the gain (decrease).



Graph 9

Graph 9 is a plot of Voltage across the reference resistor without the YIG (volts) as afunction of the set frequency (MHz). From the graph we can see that the input current to the YIG oscillator has variations. These variations is due to the increase in temperature of the circuit. If a fan is provided to the circuit then these variations freeze.

CHAPTER-IX

CONCLUSION

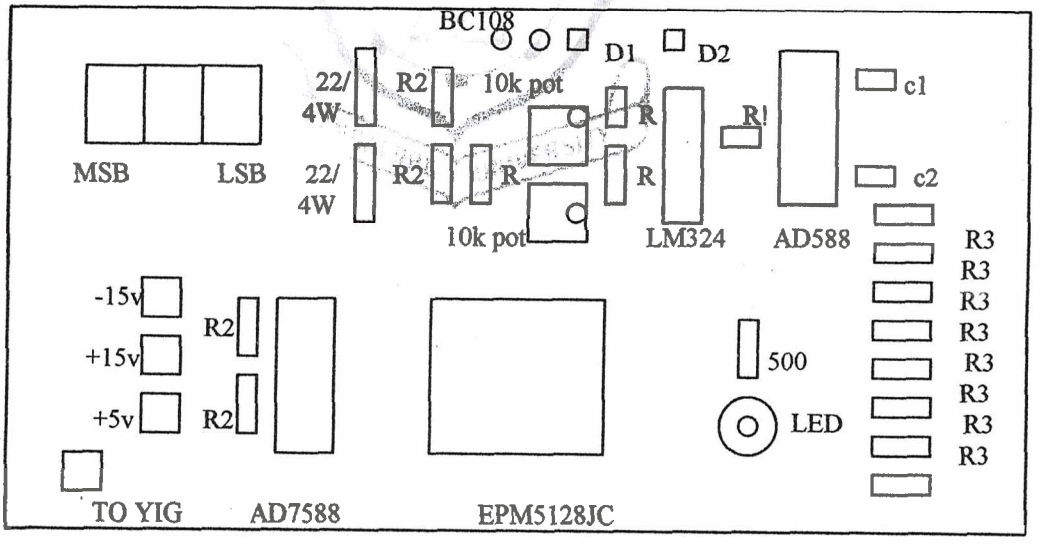
CONCLUSION

We have successfully completed the project as per the synopsis of the project. We have designed the module for coarse frequency setting of 2000 – 8000 MHz YIG tuned oscillator. The coarse frequency setting can also be achieved using PC.

From the graphs obtained we can clearly see that if we can adjust the gain and offset using potentiometers 2 and 1 respectively we can get the ideal graphs. The maximum drift of the output frequency from the set frequency is 0.27 % for a step size of 1000 MHz. The circuit without the YIG oscillator has variations in the input current to the YIG oscillator at high currents (about 350 mA and more). These variations is due to the increase in temperature of the circuit. If a fan is provided to the circuit then these variations freeze.

APPENDIX

GENERAL PURPOSE BOARD LAYOUT



EPM5128JC	→	EPLD	R1	→	100K
AD588	→	REFERENCE VOLTAGE	R2	→	3.3/2.5W
AD7533	→	DAC	R3	→	4.7k/0.25W
R	→	10K	R4	→	22/4W

COMPONENTS LIST:

ITEMS	QUANTITY
1. Thumbwheel	3
2. EPLD (EPM5128JC-1)	1
3. DAC (AD7533)	1
4. Reference IC (AD588)	1
5. Op-Amp (LM324)	1
6. Transistors:	
• BC108	2
• TIP31-C	1
7. Resistors (in ohm)	
• 3.3 (2 Watts) RCA	4
• 22 (4 Watts) RCA	2
• 500 (0.25 Watts)	1
• 1 k (0.25 Watts)	3
• 1.5 k (0.25 Watts)	1
• 2.7 k (0.25 Watts)	12
• 4.7 k (0.25 Watts)	1
• 5.1 k (0.25 Watts)	1
• 10 k (0.25 Watts)	4

• 10 k (pot)	2
• 100 k	1
8. Diodes (IN4148)	2
9. LED	5
10. Capacitors (Decoupling)	10
11. Fuse (0.5 mA)	1
12. Connector (25 pin)	1

Bibliography:

1. YIG FILTERS AND RESONATORS : HELSZAJN.J
2. DIGITAL FUNDAMENTALS : FLOYD
3. C PROGRAMMING : BALAGURUSWAMY
4. OP-AMP AND LINEAR CIRCUITS: RAMAKANTH GAYAKWAD
5. PRINCIPLES OF TRANSISTOR CIRCUITS: S.W. AMOS
6. BURR-BROWN ELECTRONIC SERIES:
   - DESIGNING WITH OP-AMPS
   - APPLICATIONS OF OP-AMPS
7. TRANSISTOR CIRCUIT APPROXIMATIONS: MALVINO
8. MANUALS: USER AND PROGRAMMING GUIDES
   - HP 8590 E-SERIES / L-SERIES SPECTRUM ANALYZER
   - GPIB NI-488.2 USER MANUAL FOR WINDOWS (NATIONAL INSTRUMENTS)
9. DATA BOOKS:
   - ANALOG DEVICES

     DATA CONVERSION PRODUCTS DATABOOK

     PMI

     LINEAR AND CONVERSION PRODUCTS DATABOOK

     RCA COMPONENTS DATA BOOK

CHAPTER-X

DATA SHEETS

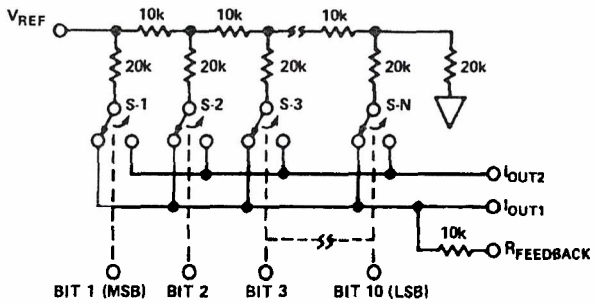
CMOS Low Cost 10-Bit Multiplying DAC

AD7533

FEATURES
Lowest Cost 10-Bit DAC
Low Cost AD7520 Replacement
Linearity: 1/2, 1 or 2LSB
Low Power Dissipation
Full Four-Quadrant Multiplying DAC
CMOS/TTL Direct Interface
Latch Free (Protection Schottky not Required)
End-Point Linearity

APPLICATIONS
Digitally Controlled Attenuators
Programmable Gain Amplifiers
Function Generation
Linear Automatic Gain Control

Functional Block Diagram



DIGITAL INPUTS (DTL/TTL/CMOS COMPATIBLE)

GENERAL DESCRIPTION

The AD7533 is a low cost 10-bit 4-quadrant multiplying DAC manufactured using an advanced thin-film-on-monolithic-CMOS wafer fabrication process.

Pin and function equivalent to the industry standard AD7520, the AD7533 is recommended as a lower cost alternative for old AD7520 sockets or new 10-bit DAC designs.

AD7533 application flexibility is demonstrated by its ability to interface to TTL or CMOS, operate on +5V to +15V power, and provide proper binary scaling for reference inputs of either positive or negative polarity.

Logic: A switch is closed to I_{OUT1} for its digital input in a "HIGH" state.

ORDERING GUIDE[1]

Model[2]	Temperature Range	Nonlinearity (% FSR max)	Package Option[3]
AD7533JN	−40°C to +85°C	±0.2	N-16
AD7533KN	−40°C to +85°C	±0.1	N-16
AD7533LN	−40°C to +85°C	±0.05	N-16
AD7533JP	−40°C to +85°C	±0.2	P-20A
AD7533KP	−40°C to +85°C	±0.1	P-20A
AD7533LP	−40°C to +85°C	±0.05	P-20A
AD7533JR	−40°C to +85°C	±0.2	R-16
AD7533KR	−40°C to +85°C	±0.1	R-16
AD7533LR	−40°C to +85°C	±0.05	R-16
AD7533AQ	−40°C to +85°C	±0.2	Q-16
AD7533BQ	−40°C to +85°C	±0.1	Q-16
AD7533CQ	−40°C to +85°C	±0.05	Q-16
AD7533SQ	−55°C to +125°C	±0.2	Q-16
AD7533TQ	−55°C to +125°C	±0.1	Q-16
AD7533UQ	−55°C to +125°C	±0.05	Q-16
AD7533SE	−55°C to +125°C	±0.2	E-20A
AD7533TE	−55°C to +125°C	±0.1	E-20A
AD7533UE	−55°C to +125°C	±0.05	E-20A

NOTES
[1]Analog Devices reserves the right to ship ceramic (package outline D-16) packages in lieu of cerdip (package outline Q-16) packages.
[2]To order MIL-STD-883, Class B processed parts, add /883B to part number. Contact your local sales office for military data sheet.
[3]E = Leadless Ceramic Chip Carrier; N = Plastic DIP; P = Plastic Leaded Chip Carrier; Q = Cerdip; R = SOIC.

REV. A

One Technology Way; P. O. Box 9106; Norwood, MA 02062-9106 U.S.A.
Tel: 617/329-4700 **Twx: 710/394-6577**
Telex: 174059 **Cables: ANALOG NORWOODMASS**

AD7533—SPECIFICATIONS (V_{DD} = +15V, V_{OUT1} = V_{OUT2} = 0V; V_{REF} = +10V unless otherwise noted)

PARAMETER	T_A = 25°C	T_A = Operating Range	Test Conditions
STATIC ACCURACY			
Resolution	10 Bits	10 Bits	
Relative Accuracy[1]			
AD7533JN, AD, SD, AQ, SQ	±0.2% FSR max	±0.2% FSR max	
AD7533KN, BD, TD, BQ, TQ	±0.1% FSR max	±0.1% FSR max	
AD7533LN, CD, UD, CQ, UQ	±0.05% FSR max	±0.05% FSR max	
Gain Error[2,3]	±1.4% FS max	±1.5% FS max	Digital Inputs = V_{INH}
Supply Rejection[4]			
$\Delta Gain/\Delta V_{DD}$	0.005%/%	0.008%/%	Digital Inputs = V_{INH}; V_{DD} = +14V to +17V
Output Leakage Current			
I_{OUT1}	±50nA max	±200nA max	Digital Inputs = V_{INL}; V_{REF} = ±10V
I_{OUT2}	±50nA max	±200nA max	Digital Inputs = V_{INH}; V_{REF} = ±10V
DYNAMIC ACCURACY			
Output Current Settling Time	600ns max[4]	800ns[5]	To 0.05% FSR; R_{LOAD} = 100Ω; Digital Inputs = V_{INH} to V_{INL} or V_{INL} to V_{INH}
Feedthrough Error	±0.05% FSR max[5]	±0.1% FSR max[5]	Digital Inputs = V_{INL}; V_{REF} = ±10V, 100kHz sine wave.
REFERENCE INPUT			
Input Resistance (Pin 15)	5kΩ min, 20kΩ max	5kΩ min, 20kΩ max[6]	
ANALOG OUTPUTS			
Output Capacitance			
C_{OUT1}	100pF max[5]	100pF max[5]	Digital Inputs = V_{INH}
C_{OUT2}	35pF max[5]	35pF max[5]	
C_{OUT1}	35pF max[5]	35pF max[5]	Digital Inputs = V_{INL}
C_{OUT2}	100pF max[5]	100pF max[5]	
DIGITAL INPUTS			
Input High Voltage			
V_{INH}	2.4V min	2.4V min	
Input Low Voltage			
V_{INL}	0.8V max	0.8V max	
Input Leakage Current			
I_{IN}	±1μA max	±1μA max	V_{IN} = 0V and V_{DD}
Input Capacitance			
C_{IN}	8pF max[5]	8pF max[5]	
POWER REQUIREMENTS			
V_{DD}	+15V ±10%	+15V ±10%	Rated Accuracy
V_{DD} Range[5]	+5V to +16V	+5V to +16V	Functionality with Degraded Performance
I_{DD}	2mA max	2mA max	Digital Inputs = V_{INL} or V_{INH}

NOTES
[1]"FSR" is Full-Scale Range.
[2]Full Scale (FS) = (V_{REF})
[3]Max gain change from T_A = +25°C to T_{min} or T_{max} is ±0.1% FSR.
[4]AC parameter, sample tested to ensure specification compliance.
[5]Guaranteed, not tested.
[6]Absolute temperature coefficient is approximately −300ppm/°C.
Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*

(T_A = +25°C unless otherwise noted)

V_{DD} to GND	−0.3V, +17V
R_{FB} to GND	±25V
V_{REF} to GND	±25V
Digital Input Voltage Range	−0.3V to V_{DD} +0.3V
OUT 1, OUT 2 to GND	−0.3V to V_{DD}
Power Dissipation (Any Package)	
To +75°C	450mW
Derates above +75°C by	6mW/°C
Operating Temperature Range	
Plastic (JN, KN, LN versions)	0 to +70°C
Hermetic (AD, BD, CD, AQ, BQ, CQ versions)	−25°C to +85°C
Hermetic (SD, TD, UD, SQ, TQ, UQ versions)	−55°C to +125°C
Storage Temperature	−65°C to +150°C
Lead Temperature (Soldering, 10sec)	+300°C

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

CAUTION:

ESD (Electro-Static-Discharge) sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subjected to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The foam should be discharged to the destination socket before devices are removed.

TERMINOLOGY

RELATIVE ACCURACY: Relative accuracy or end-point nonlinearity is a measure of the maximum deviation from a straight line passing through the endpoints of the DAC transfer function. It is measured after adjusting for ideal zero and full scale and is expressed in % of full-scale range or (sub) multiples of 1LSB.

RESOLUTION: Value of the LSB. For example, a unipolar converter with n bits has a resolution of (2^{-n}) (V_{REF}). A bipolar converter of n bits has a resolution fo $[2^{-(n-1)}]$ (V_{REF}). Resolution in no way implies linearity.

SETTLING TIME: Time required for the output function of the DAC to settle to within 1/2LSB for a given digital input stimulus, i.e., 0 to Full Scale.

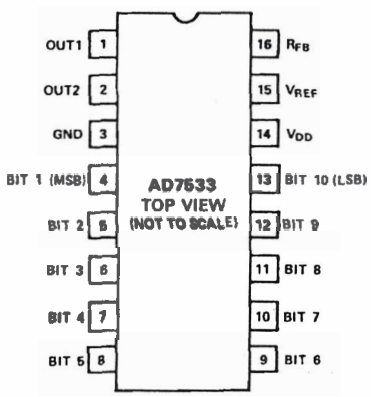
GAIN ERROR: Gain error is a measure of the output error between an ideal DAC and the actual device output. It is measured with all 1s in the DAC after offset error has been adjusted out and is expressed in Least Significant Bits. Gain error is adjustble to zero with an external potentiometer.

FEEDTHROUGH ERROR: Error caused by capacitive coupling from V_{REF} to output with all switches OFF.

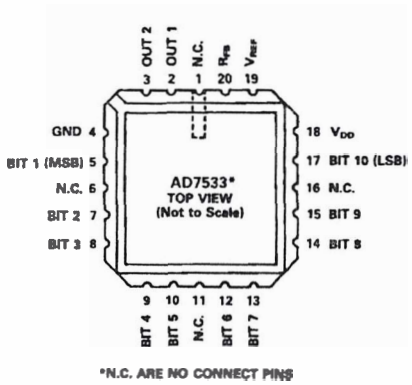
OUTPUT CAPACITANCE: Capacity from I_{OUT1} and I_{OUT2} terminals to ground.

OUTPUT LEAKAGE CURRENT: Current which appears on I_{OUT1} terminal with all digital inputs LOW or on I_{OUT2} terminal when all inputs are HIGH.

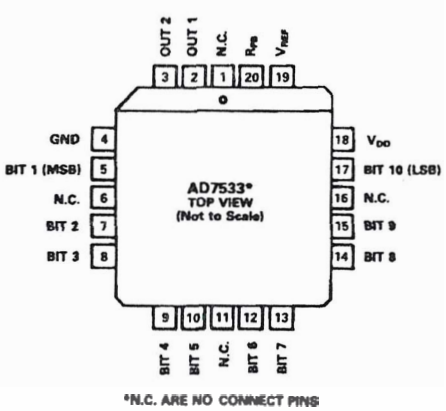
PIN CONFIGURATIONS



DIP



LCCC



PLCC

CIRCUIT DESCRIPTION

GENERAL CIRCUIT INFORMATION

The AD7533, a 10-bit multiplying D/A converter, consists of a highly stable thin film R-2R ladder and ten CMOS current switches on a monolithic chip. Most applications require the addition of only an output operational amplifier and a voltage or current reference.

The simplified D/A circuit is shown in Figure 1. An inverted R-2R ladder structure is used – that is, the binarily weighted currents are switched between the I_{OUT1} and I_{OUT2} bus lines, thus maintaining a constant current in each ladder leg independent of the switch state.

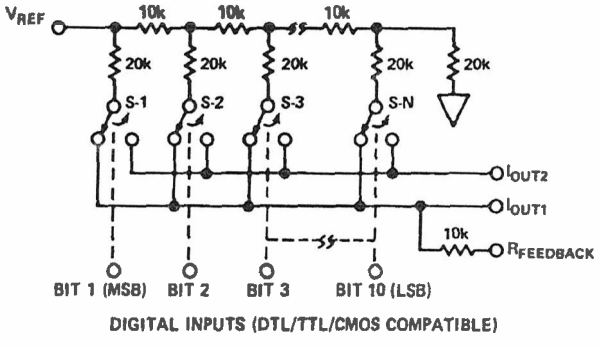


Figure 1. AD7533 Functional Diagram

One of the CMOS current switches is shown in Figure 2. The geometries of devices 1, 2 and 3 are optimized to make the digital control inputs DTL/TTL/CMOS compatible over the full military temperature range. The input stage drives two inverters (devices 4, 5, 6 and 7) which in turn drive the two output N channels. The "ON" resistances of the switches are binarily sealed so the voltage drop across each switch is the same. For example, switch 1 of Figure 2 was designed for an "ON" resistance of 20Ω, switch 2 for 40Ω, and so on. For a 10V reference input, the current through switch 1 is 0.5mA, the current through switch 2 is 0.25mA, and so on, thus maintaining a constant 10mV drop across each switch. It is essential that each switch voltage drop be equal if the binarily weighted current division property of the ladder is to be maintained.

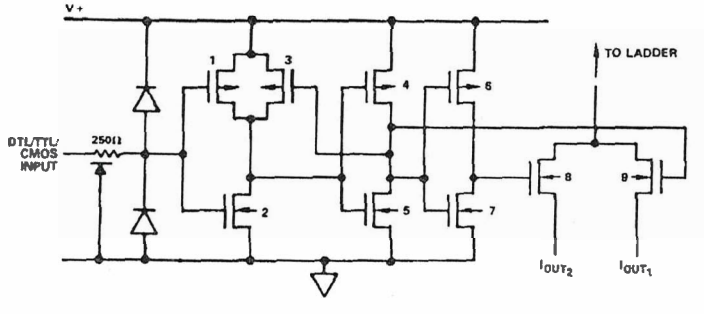


Figure 2. CMOS Switch

EQUIVALENT CIRCUIT ANALYSIS

The equivalent circuits for all digital inputs high and all digital inputs low are shown in Figures 3 and 4. In Figure 3 with all digital inputs low, the reference current is switched to I_{OUT2}. The current source $I_{LEAKAGE}$ is composed of surface and junction leakages to the substrate while the $\frac{I}{1024}$ current source represents a constant 1-bit current drain through the termination resistor on the R-2R ladder. The "ON" capacitance of the output N channel switch is 100pF, as shown on the I_{OUT2} terminal. The "OFF" switch capacitance is 35pF, as shown on the I_{OUT1} terminal. Analysis of the circuit for all digital inputs high, as shown in Figure 4, is similar to Figure 3; however, the "ON" switches are now on terminal I_{OUT1}, hence the 100pF at that terminal.

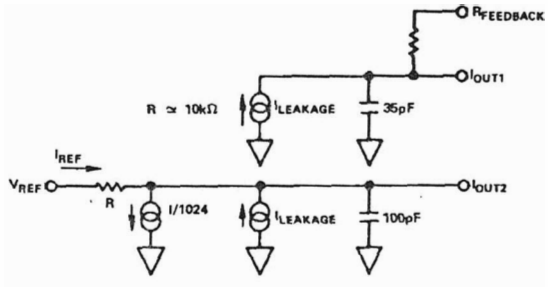


Figure 3. AD7533 Equivalent Circuit – All Digital Inputs Low

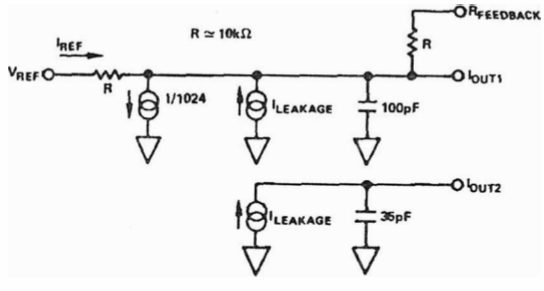


Figure 4. AD7533 Equivalent Circuit – All Digital Inputs High

OPERATION

UNIPOLAR BINARY OPERATION (2-QUADRANT MULTIPLICATION)

DIGITAL INPUT MSB LSB	ANALOG OUTPUT (V_{OUT} as shown in Figure 5)
1 1 1 1 1 1 1 1 1 1	$-V_{REF}\left(\frac{1023}{1024}\right)$
1 0 0 0 0 0 0 0 0 1	$-V_{REF}\left(\frac{513}{1024}\right)$
1 0 0 0 0 0 0 0 0 0	$-V_{REF}\left(\frac{512}{1024}\right)=\frac{V_{REF}}{2}$
0 1 1 1 1 1 1 1 1 1	$-V_{REF}\left(\frac{511}{1024}\right)$
0 0 0 0 0 0 0 0 0 1	$-V_{REF}\left(\frac{1}{1024}\right)$
0 0 0 0 0 0 0 0 0 0	$-V_{REF}\left(\frac{0}{1024}\right)=0$

NOTE:
1. Nominal LSB magnitude for the circuit of Figure 5 is given by $LSB = V_{REF}\left(\frac{1}{1024}\right)$

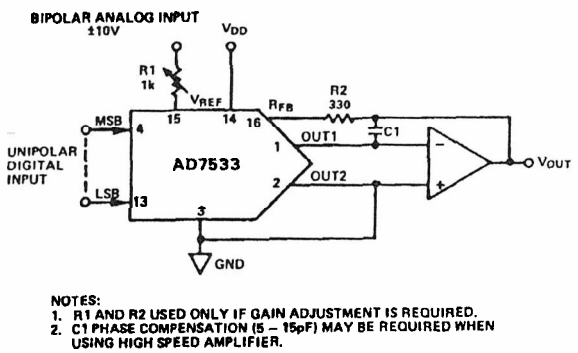
Table I. Unipolar Binary Code Table

BIPOLAR OPERATION (4-QUADRANT MULTIPLICATION)

DIGITAL INPUT MSB LSB	ANALOG OUTPUT (V_{OUT} as shown in Figure 6)
1 1 1 1 1 1 1 1 1 1	$+V_{REF}\left(\frac{511}{512}\right)$
1 0 0 0 0 0 0 0 0 1	$+V_{REF}\left(\frac{1}{512}\right)$
1 0 0 0 0 0 0 0 0 0	0
0 1 1 1 1 1 1 1 1 1	$-V_{REF}\left(\frac{1}{512}\right)$
0 0 0 0 0 0 0 0 0 1	$-V_{REF}\left(\frac{511}{512}\right)$
0 0 0 0 0 0 0 0 0 0	$-V_{REF}\left(\frac{512}{512}\right)$

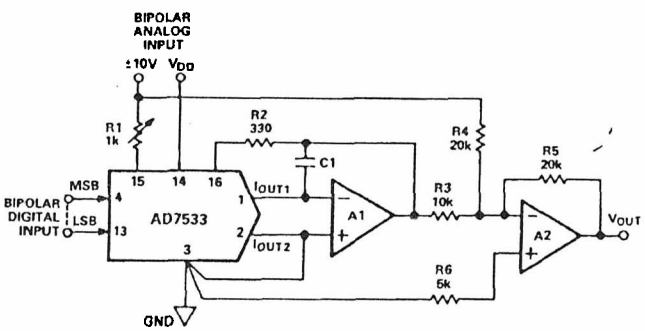
NOTE
1. Nominal LSB magnitude for the circuit of Figure 6 is given by $LSB = V_{REF}\left(\frac{1}{512}\right)$

Table II. Bipolar (Offset Binary) Code Table



NOTES:
1. R1 AND R2 USED ONLY IF GAIN ADJUSTMENT IS REQUIRED.
2. C1 PHASE COMPENSATION (5 – 15pF) MAY BE REQUIRED WHEN USING HIGH SPEED AMPLIFIER.

Figure 5. Unipolar Binary Operation (2-Quadrant Multiplication)

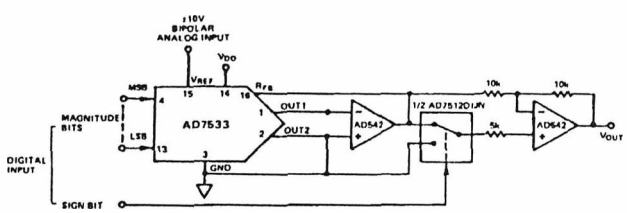


NOTES
1. R3, R4 AND R5 SELECTED FOR MATCHING AND TRACKING
2. R1, R2 USED ONLY IF GAIN ADJUSTMENT IS REQUIRED.
3. C1 PHASE COMPENSATION (5-15pF) MAY BE REQUIRED WHEN USING HIGH SPEED AMPLIFIERS

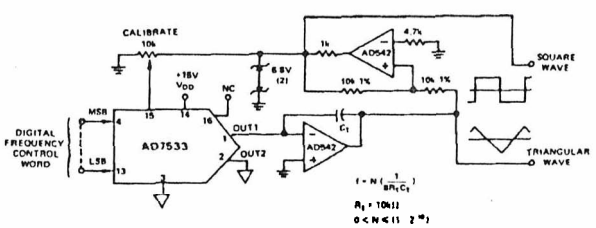
Figure 6. Bipolar Operation (4-Quadrant Multiplication)

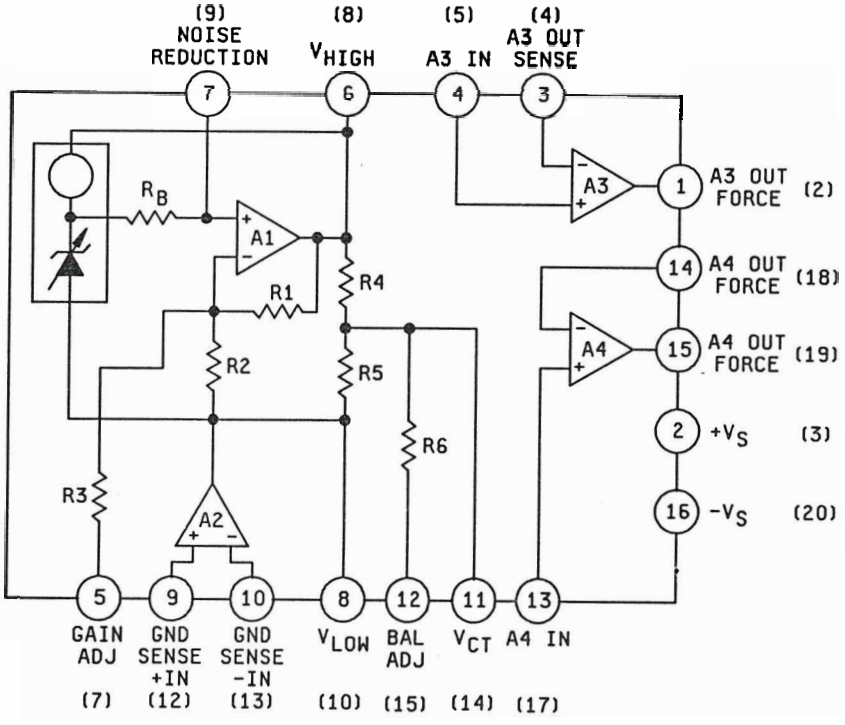
APPLICATIONS

10-BIT AND SIGN MULTIPLYING DAC



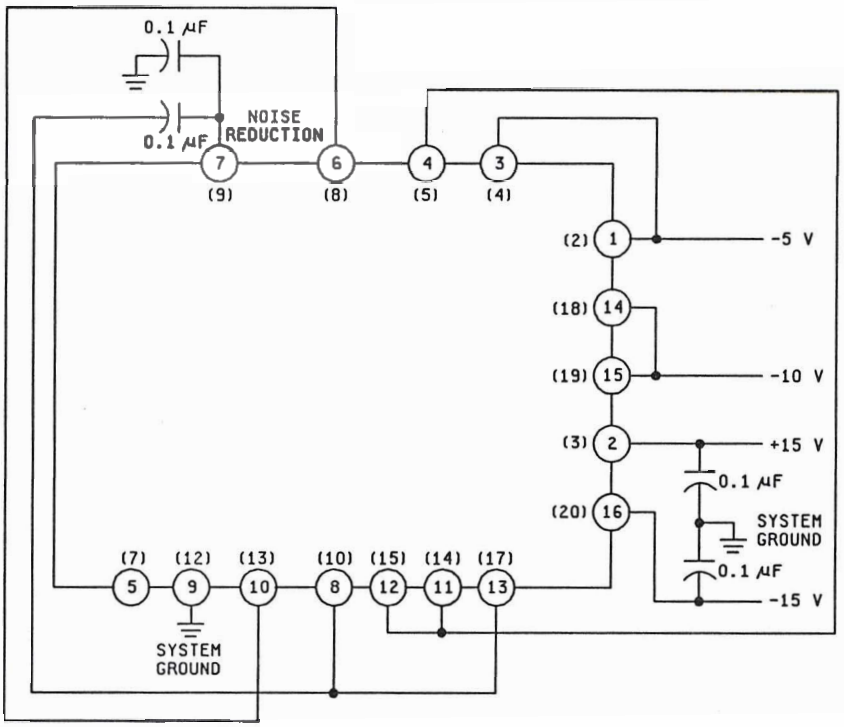
PROGRAMMABLE FUNCTION GENERATOR





NOTE: Terminal numbers within the parentheses symbol represent the case 2 package.

FIGURE 2. Logic diagram.



+10 V OUTPUT TEST CONDITIONS

NOTE: Terminal numbers within the parentheses symbol represent the case 2 package.

FIGURE 3. Test conditions – Continued.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions 1/ $-55°C \le T_A \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Output voltage error	V_{OUT}	Outputs: +10 V, -10 V,	1	01,02		±5.0	mV
		T_A = +25°C	12	02		±3.0	
		Outputs: +5.0 V, -5.0 V,	1	01,02		±5.0	
		T_A = +25°C	12	02		±3.0	
Symmetry error	S_e	Tracking mode: ±5.0 V, T_A = +25°C	1	All		±1.5	mV
Output voltage drift	dV_O / dT		2,3	01		±6.0	ppm/°C
			12	02		±4.0	
Line regulation	V_{RLN}	2/	1,2,3	All		±200	µV/V
Load regulation	V_{RLD}	+10 V output, $0 mA \le I_{OUT} \le 10 mA$	1,2,3	All		±50	µV/mA
		-10 V output, $-10 mA \le I_{OUT} \le 0 mA$				±50	
Supply current	I_{CC}		1,2,3	All		10	mA
Output current	I_{OUT}	Amplifiers A3, A4 3/	1,2,3	All	-10	+10	mA

1/ Unless otherwise specified, $+V_S$ = 15 V dc, $-V_S$ = -15 V dc. Test conditions using +10 V output, +5.0 V and –5.0 V outputs, and –10 V output, with ±5.0 V tracking are as specified on figure 3.

2/ Test conditions:

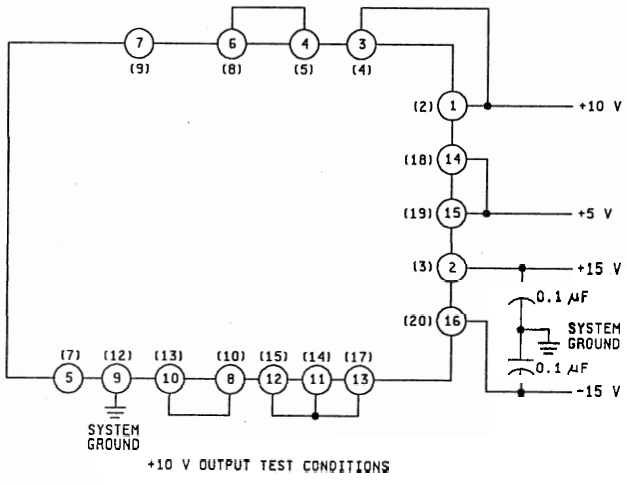
+10 V output $-V_S$ = -15 V dc, 13.5 V dc ≤ $+V_S$ ≤ 18 V dc

-10 V output $+V_S$ = +15 V dc, -18 V dc ≤ $-V_S$ ≤ -13.5 V dc

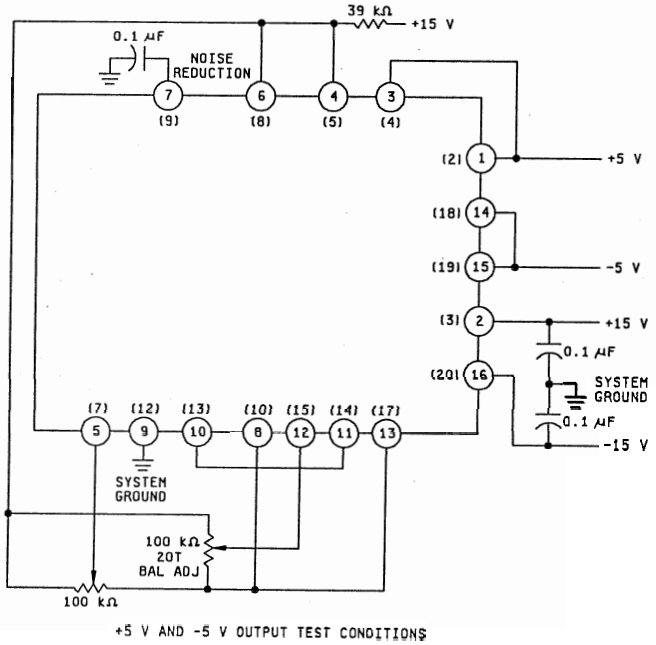
±5.0 V output $+V_S$ = +18 V dc, $-V_S$ = -10.8 V dc

$+V_S$ = +10.8 V dc, $-V_S$ = -10.8 V dc

3/ Parameters shall be tested as part of device initial characterization and after design and process change. Parameter shall be guaranteed to the limits specified in table I for all lots not specifically tested.



+10 V OUTPUT TEST CONDITIONS



+5 V AND -5 V OUTPUT TEST CONDITIONS

FIGURE 3. Test conditions.

National Semiconductor

August 2000

LM124/LM224/LM324/LM2902
Low Power Quad Operational Amplifiers

General Description

The LM124 series consists of four independent, high gain, internally frequency compensated operational amplifiers which were designed specifically to operate from a single power supply over a wide range of voltages. Operation from split power supplies is also possible and the low power supply current drain is independent of the magnitude of the power supply voltage.

Application areas include transducer amplifiers, DC gain blocks and all the conventional op amp circuits which now can be more easily implemented in single power supply systems. For example, the LM124 series can be directly operated off of the standard +5V power supply voltage which is used in digital systems and will easily provide the required interface electronics without requiring the additional ±15V power supplies.

Unique Characteristics

- In the linear mode the input common-mode voltage range includes ground and the output voltage can also swing to ground, even though operated from only a single power supply voltage
- The unity gain cross frequency is temperature compensated
- The input bias current is also temperature compensated

Advantages

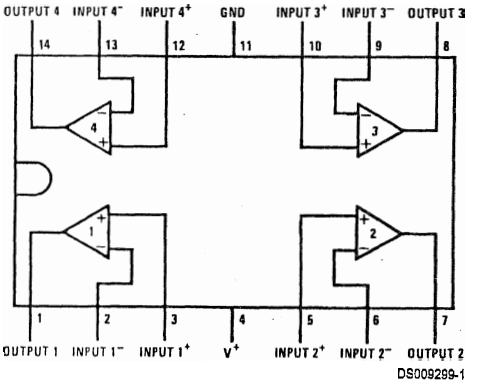
- Eliminates need for dual supplies
- Four internally compensated op amps in a single package
- Allows directly sensing near GND and V_{OUT} also goes to GND
- Compatible with all forms of logic
  Power drain suitable for battery operation

Features

- Internally frequency compensated for unity gain
- Large DC voltage gain 100 dB
- Wide bandwidth (unity gain) 1 MHz (temperature compensated)
- Wide power supply range:
  Single supply 3V to 32V
  or dual supplies ±1.5V to ±16V
- Very low supply current drain (700 µA)—essentially independent of supply voltage
  Low input biasing current 45 nA (temperature compensated)
- Low input offset voltage 2 mV and offset current: 5 nA
- Input common-mode voltage range includes ground
  Differential input voltage range equal to the power supply voltage
- Large output voltage swing 0V to V⁺ − 1.5V

Connection Diagram

Dual-In-Line Package



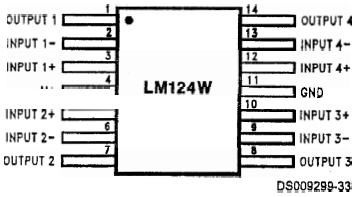
Top View

Order Number LM124J, LM124AJ, **LM124J/883** (Note 2), **LM124AJ/883** (Note 1), **LM224J, LM224AJ, LM324J,** LM324M, LM324MX, **LM324AM, LM324AMX, LM2902M, LM2902MX, LM324N, LM324AN, LM324MT,** LM324MTX or **LM2902N LM124AJRQML and LM124AJRQMLV**(Note 3)
See NS Package Number J14A, M14A or N14A

Note 1: LM124A available per JM38510/11006
Note 2: LM124 available per JM38510/11005

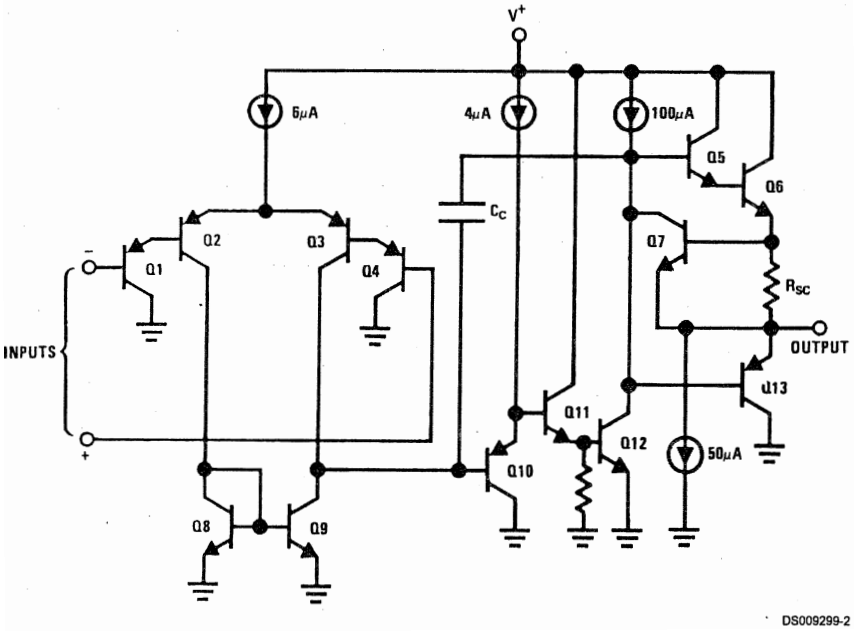
Connection Diagram (Continued)

Note 3: See STD Mil DWG 5962R99504 for Radiation Tolerant Device



Order Number LM124AW/883, LM124AWG/883, LM124W/883 or LM124WG/883
LM124AWRQML and LM124AWRQMLV(Note 3)
See NS Package Number W14B
LM124AWGRQML and LM124AWGRQMLV(Note 3)
See NS Package Number WG14A

Schematic Diagram (Each Amplifier)



Absolute Maximum Ratings (Note 12)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

	LM124/LM224/LM324 LM124A/LM224A/LM324A	LM2902
Supply Voltage, V^+	32V	26V
Differential Input Voltage	32V	26V
Input Voltage	−0.3V to +32V	−0.3V to +26V
Input Current		
(V_{IN} < −0.3V) (Note 6)	50 mA	50 mA
Power Dissipation (Note 4)		
Molded DIP	1130 mW	1130 mW
Cavity DIP	1260 mW	1260 mW
Small Outline Package	800 mW	800 mW
Output Short-Circuit to GND		
(One Amplifier) (Note 5)		
$V^+ \leq 15V$ and $T_A = 25°C$	Continuous	Continuous
Operating Temperature Range		−40°C to +85°C
LM324/LM324A	0°C to +70°C	
LM224/LM224A	−25°C to +85°C	
LM124/LM124A	−55°C to +125°C	
Storage Temperature Range	−65°C to +150°C	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	260°C	260°C
Soldering Information		
Dual-In-Line Package		
Soldering (10 seconds)	260°C	260°C
Small Outline Package		
Vapor Phase (60 seconds)	215°C	215°C
Infrared (15 seconds)	220°C	220°C
See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.		
ESD Tolerance (Note 13)	250V	250V

Electrical Characteristics

$V^+ = +5.0V$, (Note 7), unless otherwise stated

Parameter	Conditions	LM124A			LM224A			LM324A			Units
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	(Note 8) $T_A = 25°C$		1	2		1	3		2	3	mV
Input Bias Current (Note 9)	$I_{IN(+)}$ or $I_{IN(-)}$, $V_{CM} = 0V$, $T_A = 25°C$		20	50		40	80		45	100	nA
Input Offset Current	$I_{IN(+)}$ or $I_{IN(-)}$, $V_{CM} = 0V$, $T_A = 25°C$		2	10		2	15		5	30	nA
Input Common-Mode Voltage Range (Note 10)	$V^+ = 30V$, (LM2902, $V^+ = 26V$), $T_A = 25°C$	0		$V^+-1.5$	0		$V^+-1.5$	0		$V^+-1.5$	V
Supply Current	Over Full Temperature Range $R_L = \infty$ On All Op Amps										mA
	$V^+ = 30V$ (LM2902 $V^+ = 26V$)		1.5	3		1.5	3		1.5	3	
	$V^+ = 5V$		0.7	1.2		0.7	1.2		0.7	1.2	
Large Signal Voltage Gain	$V^+ = 15V$, $R_L \geq 2k\Omega$, ($V_O = 1V$ to $11V$), $T_A = 25°C$	50	100		50	100		25	100		V/mV
Common-Mode Rejection Ratio	DC, $V_{CM} = 0V$ to $V^+ - 1.5V$, $T_A = 25°C$	70	85		70	85		65	85		dB

Electrical Characteristics (Continued)

V^+ = +5.0V, (Note 7), unless otherwise stated

Parameter		Conditions		LM124A			LM224A			LM324A			Units
				Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Power Supply Rejection Ratio		V^+ = 5V to 30V (LM2902, V^+ = 5V to 26V), T_A = 25°C		65	100		65	100		65	100		dB
Amplifier-to-Amplifier Coupling (Note 11)		f = 1 kHz to 20 kHz, T_A = 25°C (Input Referred)			−120			−120			−120		dB
Output Current	Source	V_{IN}^+ = 1V, V_{IN}^- = 0V, V^+ = 15V, V_O = 2V, T_A = 25°C		20	40		20	40		20	40		mA
	Sink	V_{IN}^- = 1V, V_{IN}^+ = 0V, V^+ = 15V, V_O = 2V, T_A = 25°C		10	20		10	20		10	20		mA
		V_{IN}^- = 1V, V_{IN}^+ = 0V, V^+ = 15V, V_O = 200 mV, T_A = 25°C		12	50		12	50		12	50		µA
Short Circuit to Ground		(Note 5) V^+ = 15V, T_A = 25°C			40	60		40	60		40	60	mA
Input Offset Voltage		(Note 8)				4			4			5	mV
V_{OS} Drift		R_S = 0Ω			7	20		7	20		7	30	µV/°C
Input Offset Current		$I_{IN(+)} - I_{IN(-)}$, V_{CM} = 0V				30			30			75	nA
I_{OS} Drift		R_S = 0Ω			10	200		10	200		10	300	pA/°C
Input Bias Current		$I_{IN(+)}$ or $I_{IN(-)}$			40	100		40	100		40	200	nA
Input Common-Mode Voltage Range (Note 10)		V^+ = +30V (LM2902, V^+ = 26V)		0		V^+−2	0		V^+−2	0		V^+−2	V
Large Signal Voltage Gain		V^+ = +15V (V_OSwing = 1V to 11V) $R_L \geq 2$ kΩ		25			25			15			V/mV
Output Voltage Swing	V_{OH}	V^+ = 30V (LM2902, V^+ = 26V)	R_L = 2 kΩ	26			26			26			V
			R_L = 10 kΩ	27	28		27	28		27	28		
	V_{OL}	V^+ = 5V, R_L = 10 kΩ			5	20		5	20		5	20	mV
Output Current	Source	V_O = 2V	V_{IN}^+ = +1V, V_{IN}^- = 0V, V^+ = 15V	10	20		10	20		10	20		mA
	Sink		V_{IN}^- = +1V, V_{IN}^+ = 0V, V^+ = 15V	10	15		5	8		5	8		

Electrical Characteristics

V^+ = +5.0V, (Note 7), unless otherwise stated

Parameter	Conditions	LM124/LM224			LM324			LM2902			Units
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	(Note 8) T_A = 25°C		2	5		2	7		2	7	mV
Input Bias Current (Note 9)	$I_{IN(+)}$ or $I_{IN(-)}$, V_{CM} = 0V, T_A = 25°C		45	150		45	250		45	250	nA
Input Offset Current	$I_{IN(+)}$ or $I_{IN(-)}$, V_{CM} = 0V, T_A = 25°C		3	30		5	50		5	50	nA
Input Common-Mode Voltage Range (Note 10)	V^+ = 30V, (LM2902, V^+ = 26V), T_A = 25°C	0		V^+−1.5	0		V^+−1.5	0		V^+−1.5	V
Supply Current	Over Full Temperature Range R_L = ∞ On All Op Amps										mA
	V^+ = 30V (LM2902 V^+ = 26V)		1.5	3		1.5	3		1.5	3	
	V^+ = 5V		0.7	1.2		0.7	1.2		0.7	1.2	
Large Signal Voltage Gain	V^+ = 15V, $R_L \geq$ 2kΩ, (V_O = 1V to 11V), T_A = 25°C	50	100		25	100		25	100		V/mV
Common-Mode Rejection Ratio	DC, V_{CM} = 0V to V^+ − 1.5V, T_A = 25°C	70	85		65	85		50	70		dB
Power Supply Rejection Ratio	V^+ = 5V to 30V (LM2902, V^+ = 5V to 26V),	65	100		65	100		50	100		dB

Electrical Characteristics (Continued)

V^+ = +5.0V, (Note 7), unless otherwise stated

Parameter		Conditions		LM124/LM224			LM324			LM2902			Units
				Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
		T_A = 25°C											
Amplifier-to-Amplifier Coupling (Note 11)		f = 1 kHz to 20 kHz, T_A = 25°C (Input Referred)			−120			−120			−120		dB
Output Current	Source	V_{IN}^+ = 1V, V_{IN}^- = 0V, V^+ = 15V, V_O = 2V, T_A = 25°C		20	40		20	40		20	40		mA
	Sink	V_{IN}^- = 1V, V_{IN}^+ = 0V, V^+ = 15V, V_O = 2V, T_A = 25°C		10	20		10	20		10	20		mA
		V_{IN}^- = 1V, V_{IN}^+ = 0V, V^+ = 15V, V_O = 200 mV, T_A = 25°C		12	50		12	50		12	50		µA
Short Circuit to Ground		(Note 5) V^+ = 15V, T_A = 25°C			40	60		40	60		40	60	mA
Input Offset Voltage		(Note 8)				7			9			10	mV
V_{OS} Drift		R_S = 0Ω			7			7			7		µV/°C
Input Offset Current		$I_{IN(+)} - I_{IN(-)}$, V_{CM} = 0V				100			150		45	200	nA
I_{OS} Drift		R_S = 0Ω			10			10			10		pA/°C
Input Bias Current		$I_{IN(+)}$ or $I_{IN(-)}$			40	300		40	500		40	500	nA
Input Common-Mode Voltage Range (Note 10)		V^+ = +30V (LM2902, V^+ = 26V)		0		V^+−2	0		V^+−2	0		V^+−2	V
Large Signal Voltage Gain		V^+ = +15V (V_OSwing = 1V to 11V) $R_L \geq 2$ kΩ		25			15			15			V/mV
Output Voltage Swing	V_{OH}	V^+ = 30V (LM2902, V^+ = 26V)	R_L = 2 kΩ	26			26			22			V
			R_L = 10 kΩ	27	28		27	28		23	24		
	V_{OL}	V^+ = 5V, R_L = 10 kΩ			5	20		5	20		5	100	mV
Output Current	Source	V_O = 2V	V_{IN}^+ = +1V, V_{IN}^- = 0V, V^+ = 15V	10	20		10	20		10	20		mA
	Sink		V_{IN}^- = +1V, V_{IN}^+ = 0V, V^+ = 15V	5	8		5	8		5	8		

Note 4: For operating at high temperatures, the LM324/LM324A/LM2902 must be derated based on a +125°C maximum junction temperature and a thermal resistance of 88°C/W which applies for the device soldered in a printed circuit board, operating in a still air ambient. The LM224/LM224A and LM124/LM124A can be derated based on a +150°C maximum junction temperature. The dissipation is the total of all four amplifiers—use external resistors, where possible, to allow the amplifier to saturate of to reduce the power which is dissipated in the integrated circuit.

Note 5: Short circuits from the output to V^+ can cause excessive heating and eventual destruction. When considering short circuits to ground, the maximum output current is approximately 40 mA independent of the magnitude of V^+. At values of supply voltage in excess of +15V, continuous short-circuits can exceed the power dissipation ratings and cause eventual destruction. Destructive dissipation can result from simultaneous shorts on all amplifiers.

Note 6: This input current will only exist when the voltage at any of the input leads is driven negative. It is due to the collector-base junction of the input PNP transistors becoming forward biased and thereby acting as input diode clamps. In addition to this diode action, there is also lateral NPN parasitic transistor action on the IC chip. This transistor action can cause the output voltages of the op amps to go to the V^+voltage level (or to ground for a large overdrive) for the time duration that an input is driven negative. This is not destructive and normal output states will re-establish when the input voltage, which was negative, again returns to a value greater than −0.3V (at 25°C).

Note 7: These specifications are limited to −55°C ≤ T_A ≤ +125°C for the LM124/LM124A. With the LM224/LM224A, all temperature specifications are limited to −25°C ≤ T_A ≤ +85°C, the LM324/LM324A temperature specifications are limited to 0°C ≤ T_A ≤ +70°C, and the LM2902 specifications are limited to −40°C ≤ T_A ≤ +85°C.

Note 8: $V_O \approx$ 1.4V, R_S = 0Ω with V^+ from 5V to 30V; and over the full input common-mode range (0V to V^+ − 1.5V) for LM2902, V^+ from 5V to 26V.

Note 9: The direction of the input current is out of the IC due to the PNP input stage. This current is essentially constant, independent of the state of the output so no loading change exists on the input lines.

Note 10: The input common-mode voltage of either input signal voltage should not be allowed to go negative by more than 0.3V (at 25°C). The upper end of the common-mode voltage range is V^+ − 1.5V (at 25°C), but either or both inputs can go to +32V without damage (+26V for LM2902), independent of the magnitude of V^+.

Note 11: Due to proximity of external components, insure that coupling is not originating via stray capacitance between these external parts. This typically can be detected as this type of capacitance increases at higher frequencies.

Note 12: Refer to RETS124AX for LM124A military specifications and refer to RETS124X for LM124 military specifications.

Note 13: Human body model, 1.5 kΩ in series with 100 pF.

TIP31, TIP31A, TIP31B, TIP31C

File Number 991

Epitaxial-Base, Silicon N-P-N VERSAWATT Transistors

For Power-Amplifier and High-Speed-Switching Applications

Features:

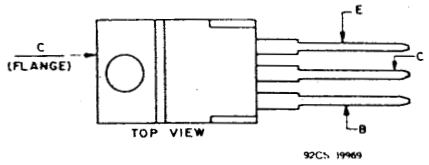
- *40 W at 25°C case temperature*
- *5 A rated collector current*
- *Min. f_T of 3 MHz at 10 V, 500 mA*
- *Designed for complementary use with TIP32-series p-n-p types**

The RCA-TIP31, TIP31A, TIP31B, and TIP31C are epitaxial-base, silicon n-p-n transistors intended for a wide variety of switching and amplifier applications, such as series and shunt regulators and driver and output stages of high-fidelity amplifiers. These power transistors are designed for complementary use with devices in the TIP32 series. They differ from each other in voltage ratings.

They are supplied in the JEDEC TO-220AB (VERSAWATT) plastic package.

* Technical data for the TIP32-series devices are given in RCA data bulletin File No. 987

TERMINAL DESIGNATIONS



JEDEC TO-220AB

MAXIMUM RATINGS, *Absolute-Maximum Values:*

	TIP31	TIP31A	TIP31B	TIP31C	
V_{CBO}	40	60	80	100	V
V_{CEO}	40	60	80	100	V
V_{EBO}	5	5	5	5	V
I_C	5	5	5	5	A
I_B	1	1	1	1	A
P_T:					
At $T_C \leq 25°C$	40	40	40	40	W
At $T_A \leq 25°C$	2	2	2	2	W
At $T_C > 25°C$ ... Derate linearly	0.32				W/°C
T_{stg}, T_J	-65 to 150				°C
T_L (During soldering):					
At distance 1/8 in. (3.17 mm) from case for 10 s max.	235				°C

ELECTRICAL CHARACTERISTICS, *At Case Temperature (T_C) = 25°C unless otherwise specified*

CHARACTERISTIC	TEST COND. VOLTAGE V dc	TEST COND. CURRENT A dc	LIMITS TIP31 Min.	TIP31 Max.	TIP31A Min.	TIP31A Max.	TIP31B Min.	TIP31B Max.	TIP31C Min.	TIP31C Max.	Units
	V_{CE}	I_C									
I_{CEO} I_B=0	30		–	0.3	–	0.3	–	–	–	–	
	60		–	–	–	–	–	0.3	–	0.3	mA
I_{CES} V_{EB}=0	40		–	0.2	–	–	–	–	–	–	
	60		–	–	–	0.2	–	–	–	–	
	80		–	–	–	–	–	0.2	–	–	mA
	100		–	–	–	–	–	–	–	0.2	
I_{EBO} V_{BE}=–5V		0	–	1	–	1	–	1	–	1	mA
$V_{CEO(sus)}$ I_B=0		0.03[a]	40[b]	–	60[b]	–	80[b]	–	100[b]	–	V
h_{FE}	4	1[a]	25	–	25	–	25	–	25	–	
	4	3[a]	10	50	10	50	10	50	10	50	
V_{BE}	4	3[a]	–	1.8	–	1.8	–	1.8	–	1.8	V
$V_{CE(sat)}$ I_B= 0.375A		3[a]	–	1.2	–	1.2	–	1.2	–	1.2	V
h_{fe} f=1 kHz	10	0.5	20	–	20	–	20	–	20	–	
$\|h_{fe}\|$ f=1 MHz	10	0.5	3	–	3	–	3	–	3	–	
t_{ON} (t_d+t_r) V_{CC}= 30V R_L=30Ω I_{B1}=I_{B2} =0.1A		1	0.4 (typ.)		0.4 (typ.)		0.4 (typ.)		0.4 (typ.)		μs
t_{OFF} (t_s+t_f) V_{CC}= 30V R_L=30Ω I_{B1}=–I_{B2} =0.1A		1	1.2 (typ.)		1.2 (typ.)		1.2 (typ.)		1.2 (typ.)		μs
$R_{\theta JC}$			–	3.125	–	3.125	–	3.125	–	3.125	°C/W
$R_{\theta JA}$			–	62.5	–	62.5	–	62.5	–	62.5	°C/W

[a] Pulsed, pulse duration = 300 μs, duty factor ≤ 2%.

[b] *CAUTION:* Sustaining voltage, $V_{CEO(sus)}$, *MUST NOT* be measured on a curve tracer.