MULTI-CHANNEL BUFFERED DATA ROUTER FOR A DIGITAL SPECTROMETER

PROJECT REPORT

Jointly submitted in partial fulfilment of requirements

for the award of the degree of

Bachelor of Engineering in Electronics

by

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UNDER THE GUIDANCE OF

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1994-95

DEPARTMENT OF ELECTRONICS

R V COLLEGE OF ENGINEERING

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BANGALORE UNIVERSITY

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BANGALORE - 560 059

Certificate

This is to certify that this project work entitled

MULTI-CHANNEL BUFFERED DATA ROUTER FOR A DIGITAL SPECTROMETER

has been successfully carried out by

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in the partial fulfilment of the requirement for the award of the Degree of

Bachelor of Engineering in Electronics

during the academic year 1994-95

T.S. Rukmini

Project Guide

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MULTI-CHANNEL BUFFERED DATA ROUTER FOR A DIGITAL SPECTROMETER

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PROJECT SYNOPSIS

Introduction:

We are involved in designing and implementing a programmable **High speed Multi Channel Data Acquistion cum Signal Processing System .** The *Buffered Data Router* is going to the front end of the **Fast Fourier Transform card (FFT)** which forms the kernel of a digital spectrometer.

The FFT card was designed at RRI. At the heart of the FFT card lies a Fast Fourier Transform Processor the PDSP16150 from PLESSEY SEMICONDUCTORS. This digital spectrometer (including our BDR) will be assimilated into the Gauribidanur radio telescope, and will be used to study carbon radio recombination lines.

Functional explanation:

The block diagram shows the overall **Multi-Channel Digital Spectrometer** hardware. The BDR is at the top of the hiearchy as far as data flow is concerned. The signals in analog domain are digitized and stored in memeory banks in BDR module itself. It is then furnished to the FFT module in contigious blocks.

The FFT module consists of the FFT chip which accepts data on two 16-bit input channels either as real or imaginary parts of a complex sequence or as two independent sequences. This chip then compiles the fast fourier transform of the input data at very high speed. The output is also in the form of 16-bit integers.

This output is fed to an integrator, where the fourier samples, are integrated in order to extract the signal buried in noise. The pipelined adders required for integration are incorporated in high density EPLDs called FLEX devices.

A PC/AT based interface has been developed for high speed acquistion of data and then transfered directly on the hard disk, at speeds of a few Mbytes per second. This interface is designed to follow **Extended Industry Standard Architecture (EISA)** bus standards, which allows 32-bit transfers.

Design of BDR:

The system is to be designed in such a way that it can acquire signal both in the time domain and in the frequency domain. To accomplish this, we intend to design the system around high speed ADCs, Multiplexers etc.

The design of the high speed BDR is still under scrutiny for the following reasons. We have two design philophies in mind, they are:

(a) To use only a single ultra high speed ADC with a analog multiplexer preceeding it.

(b) To use eight medium speed low cost ADCs

Is it feasible to use a single ultra high speed ADC operating at several megacycles per second with all the associated circuitry to compensate high

frequency errors or use eight ADCsfor the eight channels, operating at several kilocycles per second?

It is a problem of optimization of cost, performance and circuit simplicity.

Our BDR is programmable, in the sense that, the user can opt the number of channels (1to 8) and select the number of points for the FFT computation. The various modes of operation and the data rate can be 16 point complex at 24 Msamples/sec or 2*1024 point complex at 12Msamples/sec and so on.

We have to design the base band filters as depicted and a EISA interface for FFT card.

The BDR is going to have as a wide range of applications. Due to its programmable flexibility it can be used in a multitude of situations where the number of channels required vary. With just the EISA interface (excluding FFT card) the system can also perform as a high speed DAS. It can also be used as a general lab spectrum analyser. The design of the BDR is such that, in future when ultra high speed ADCs are available at low costs they can be swapped with the existing ones with rest of the circuitry unchanged.

CHAPTER ONE
PROJECT OVERVIEW

1.1 INTRODUCTION.

Fourier Transform(FT) is fundamental tool of spectrum analysis used in several applications, both commercial and scientific. Among its applications in Radio Astronomy, there is an ever-growing need for faster computation of FT over long sequences of data samples. Conventionally, this is realized with highly optimized, "fast" fourier transform algorithms written on high speed, general purpose computer system. In such a case, the cost to computation ratio for a general computer proves too very uneconomical. In several cases, it may be required to obtain spectra of signals in real-time, before recording. However there are many applications demanding a throughput rate that cannot be afforded by these computers and quite often, one needs a dedicated FT processor.

In real time applications, these devices may be used as embedded processors in the target circuits and can as well be interfaced suitably to work as "accelerators" for general purpose computers. Engineers at RRI have developed a flexible Digital Spectrometer Card(DSC) to function for both of these purposes.

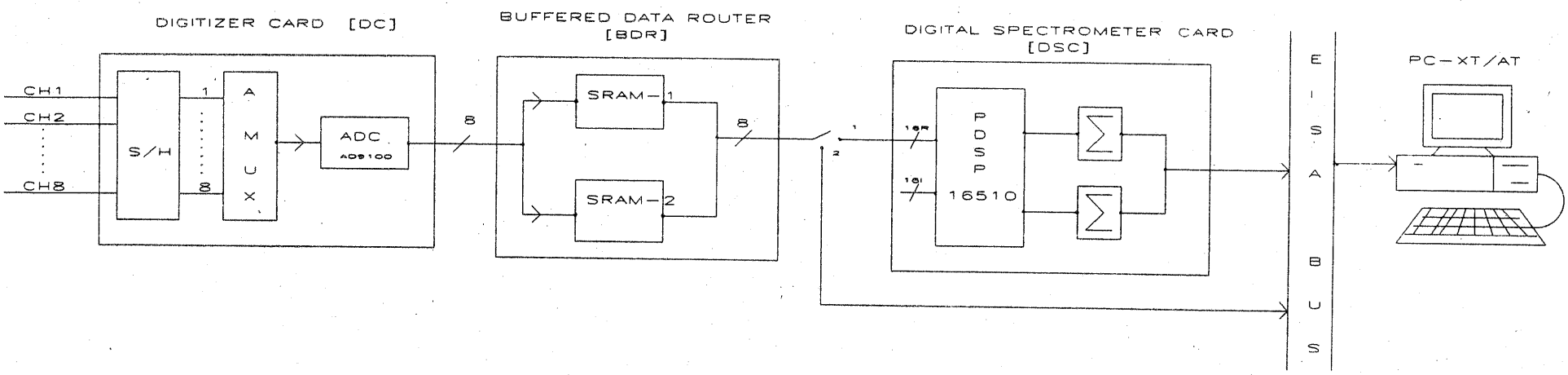
The genesis of this design is a part of an ongoing Pulsar instrumentation work. Apart from observation of pulsars, the system can be used in a variety of astronomical applications like the Radio Recombinational lines studies, Electron Proton Annihilation studies, or as a general purpose Spectrometer which can perform long stretches of integrations

1.2 MULTI - CHANNEL SPECTROMETER

At the heart of the SPECTROMETER is a DSP chip PDSP16510. This is a dedicated FFT chip. This chip accepts data on two 16-bit input channels, either as the real and imaginary parts of a complex sequence, or as two independent real sequences. It can perform FFT over different lengths of data sequence, for example- 16, 64, 256 & 1024 points at the maximum rate of 12 M samples/sec. This output can be either acquired by a PC/AT with EISA BUS interface or can be integrated in the buffers of the DSC. The integration buffers are implemented by using FIFOs as the associated control logic will be bare minimum. The user can integrate the data up to 2^{16} times in these buffers. When integrated, data can be written on to the hard disk. At the same time the integrated fourier transformed output will be written into the other FIFO and this process repeats.

The DSC does not include the necessary interface circuitry for interfacing the signals from the Real world domain to the Digital Domain. Being single channel spectrometer, it offers limited resolution. In order to develop a completely independent, multi-channel Digital Spectrometer, we have designed a programmable 8-channel Digitizer card and a Buffered Data Router(BDR). The over all block diagram of the system is shown in *fig(1.1)*

The programmable 8 channel Digitizer Card has a bank of 8 sample and hold circuits at the front end, for sampling the analog signals. It is followed by 8x1 analog multiplexer whose



OVER ALL BLOCK DIAGRAM

figure 1.1

output is fed to a 10-bit ADC. This ADC is of FLASH type which can work at a maximum speed of 18 Msamples/sec and has a novel pipelined architecture. Due to its piplined architecture, after 4 clock cycles the digitized data flows out continuously. The start of conversion and end of conversion pulses are not necessary to digitize each sample, thus simplifying the control circuitry. The digitized data is then fed to the Buffered Data Router [BDR].

The BDR is equipped with a double buffer of SRAM memory chips and the necessary control logic. Input data is first written into BUFFER-A at the rate programmed by the user depending upon the input bandwidth. As soon as the programmed number of points per channel have been written, the address counter sends a buffer full signal to the MUX circuits. At this point the MUX swaps the buffers. The input data is now written into BUFFER-B while BUFFER-A will be read by host CPU or the DSC. The buffers are swapped again when BUFFER-B sends its buffer full signal to the MUX circuits, and this process repeats.

The ALTERA programmable logic development system was used to integrate various logic circuits into MAX-7000 and MAX-5000 family EPLDs. In fact we have used EPM7128LC84 (84-pin EPLD), which appertains to the MAX-7000 family while the other is EPM5016 (20-pin EPLD) of MAX-5000 family. These chips provide a comprehensive cost-effective solution for designs, intensive in combinatorial logic.

CHAPTER TWO

DESIGN PHILOSOPHY

2.1 THE PROBLEM.

The crux of the problem lies in radio observations of low frequency **Carbon Radio Recombination Lines (CRRLs)** by making use of the Multi Channel Spectrometer. By "Lines" we ascribe to radiation at unique wavelengths. Every element has a unique emission spectrum - finger prints of elements. These lines are caused for the following reason. When an electron is excited by supplement of energy either thermal or non-thermal, the electrons move to an higher energy level (orbit). This state is quasi-stable state, hence it falls back to its previous stable state, i.e. lower energy level. In doing so the difference in energy is radiated as electromagnetic radiation. Since energy levels are quantized, the emitted energy is of definite wavelength.

At the **Gauribidanur Radio Telescope (GEETEE)** [please refer to Appendix-A.] the recombination lines can be observed at decametric wavelengths. The operating frequency of the GEETEE is **34.5 MHz,** with a good usable **bandwidth** of **2 MHz**. The CRRLs at these frequencies correspond to high principal quantum numbers around 574α, with typical line widths of the order of 1kHz. Within the observational bandwidth of GEETEE 12 of these CRRLs can be observed.[please refer to Appendix-B]. In order to observe these lines a

resolution of approximately 250 Hz is an essential condition. Hence it was conceived to build a stable Spectrometer, which could be used for the above said observations.

The DSC could not be used in its present form of single channel spectrometer, because of the poor resolution that could be obtained, which is elucidated in the following discussion.

The resolution of the Spectrometer is defined as:

Resolution = BW / N Hz.

where BW is the Bandwidth and N is the number of points of FFT performed.

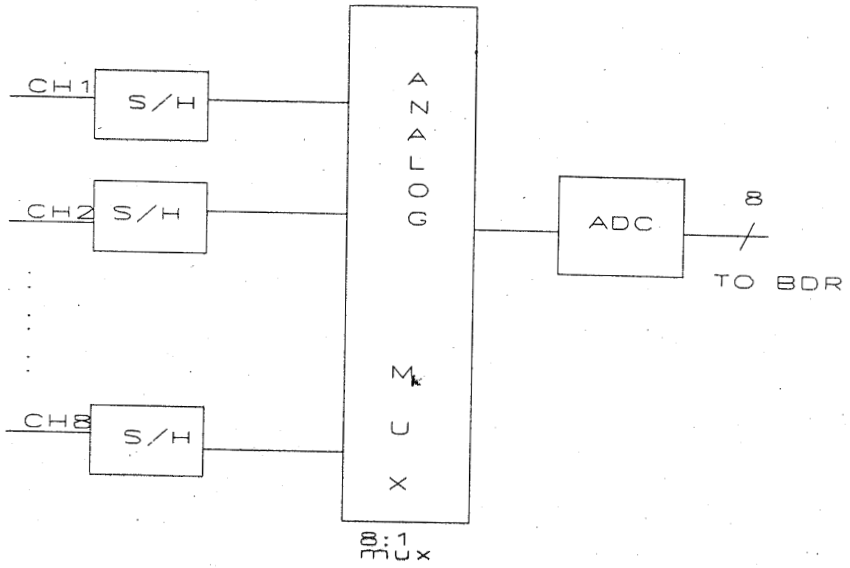
If we determine the resolution of the Spectrometer for 2 MHz bandwidth with 1024 points FFT it turns out to be :

Resolution = 2 MHz / 1024 = 1953.12500 Hz

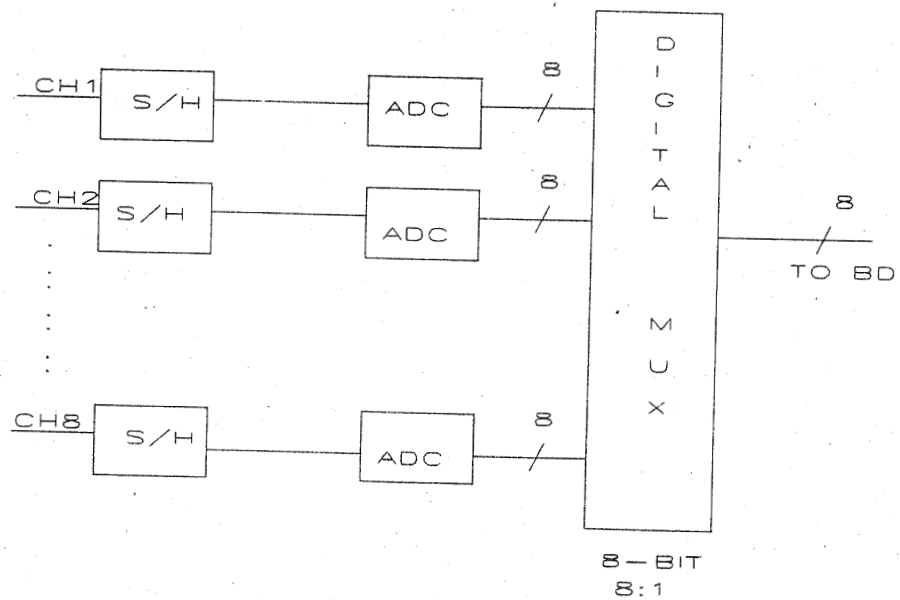
The resolution obtained is clearly inadequate for useful observations. In order to improve the resolution, we have hit upon the novel idea of splitting the 2 MHz bandwidth into 8 separate bands each of bandwidth 250 kHz and then performing a 1024 point FFT on each of them. This will improve the Resolution, by a factor of 8 and the resolution would now be

Resolution = 250 kHz / 1024 = 244.140625 Hz

which could be used conveniently for the observations.



DESIGN (a)



DESIGN (b)

DESIGN OPTIONS

figure 2.1

2.2 DESIGN PRINCIPLE OF DIGITIZER CARD.

The design dogma is now dictated by the *reductio ad absurdum* in the previous section. It is now clear that the number of input channels for BDR is 8. There are two design philosophies which can be implemented.

They are:

(a) To use a single high speed ADC with a analog multiplxer.

(b) To use eight medium speed ADCs with a digital multiplxer.

The block diagram of the two designs are shown in *fig(2.1)*. Comparing the two design philosophies, we will come to know that design (a) is cost effective and simple in terms of circuitry. The reasons are obvious, when one looks at the two designs. The first point we notice is that we need 8 ADCs for design (b) while only one ADC is sufficient for design (a). Since the ADCs are of 8-bit resolution we need a **8-bit 8:1 Digital Multiplexer** for design (b). The Digital Multiplexer may not be available or may be too expensive. All these bottle necks are not encountered in design (a).

2.3 DESIGN PRINCIPLE OF BUFFERED DATA ROUTER.

The BDR furnishes digitized data to the DSC card. It should take heed of supplying data in proper format and at required throughput rates so that both of them work in synchronism.

When we give a "**Sample**" command to the S/H circuit we are actually sampling 8 input analog signals appearing at 8 input channels. After digitizing we obtain a serial output of 8 data points, each of which corresponds to 8 channels in sequential order. It is quite evident that we cannot send these data words directly to DSC, because individual data points do not have any correlation with each other as they are from different channels. There is one way out of this bottle neck, that is by storing the data temporarily on some storage device and then throughputting the data in contiguous blocks to the PDSP chip. Therefore we are making use of a memory (SRAM) as temporary storage.

After 1024 data points from each channel has been written, it is read out of the memory in the fashion the PDSP desires. Subsequently we will be storing a maximum of 8 * 1024 = 8192 data points. Inevitably we need a 8K RAM chip to accommodate this data.

Continuum supply of data necessitates read and write simultaneously Since this is not possible on a RAM chip, we are left with a choice of using two 8K RAM chips(of course, we

could use Dual-Port RAM, but the control circuitry would be involving and complex) hence we restrain ourselves to a simple design involving two RAMs. We apportion 1K in both of the 8K RAM chips for each channel. Individual data points are written in their respective 1K blocks. After 8192 samples and digitization we are left with one of the RAM chips full of data where in, each 1K block of memory corresponds to one particular channel. Now we can read out of RAM chip and furnish this data to DSP. Simultaneously we can continue to write fresh data into the second RAM chip. Under this circumstance the PDSP chip sees a continuous stream of data from BDR even though the acquisition is by fits and starts.

CHAPTER THREE

HARDWARE IMPLEMENTATION

3.1 DIGITIZER CARD IMPLEMENTATION

With the design of digitizer card finalized, it can be seen that it will require these basic components:

- ***Sample and Hold circuits***
- ***Analog Multiplexer***
- ***Analog to Digital Converter***

Sample and Hold circuit:

The signals from all the 8 channels are sampled at the same instant of time. The S/H circuits will be holding the same analog value till the next sample pulse is applied. With an input frequency band of 250 kHz, the Nyquist sampling frequency will be 500 kHz. So the time interval between two samples is 2μsecs. In this time period the ADC will have to digitize all 8 channel outputs starting from the first channel through the last channel in sequential order. Hence there will be 0.25μseconds for each channel to be digitized. The S/H on the 8th channel will therefore, have to hold its output for 1.75μseconds. We have chosen ***AD9100*** for sampling the analog signals, which has a typical droop rate of 1mV/μs. The droop in output voltage of the last S/H is 1.75mV. The resolution of the ADC used (AD773) is 0.97mV. So a change of 1.75mV at the S/H output will lead to an approximate change of 2 bits in the digitized value of the ADC output. This

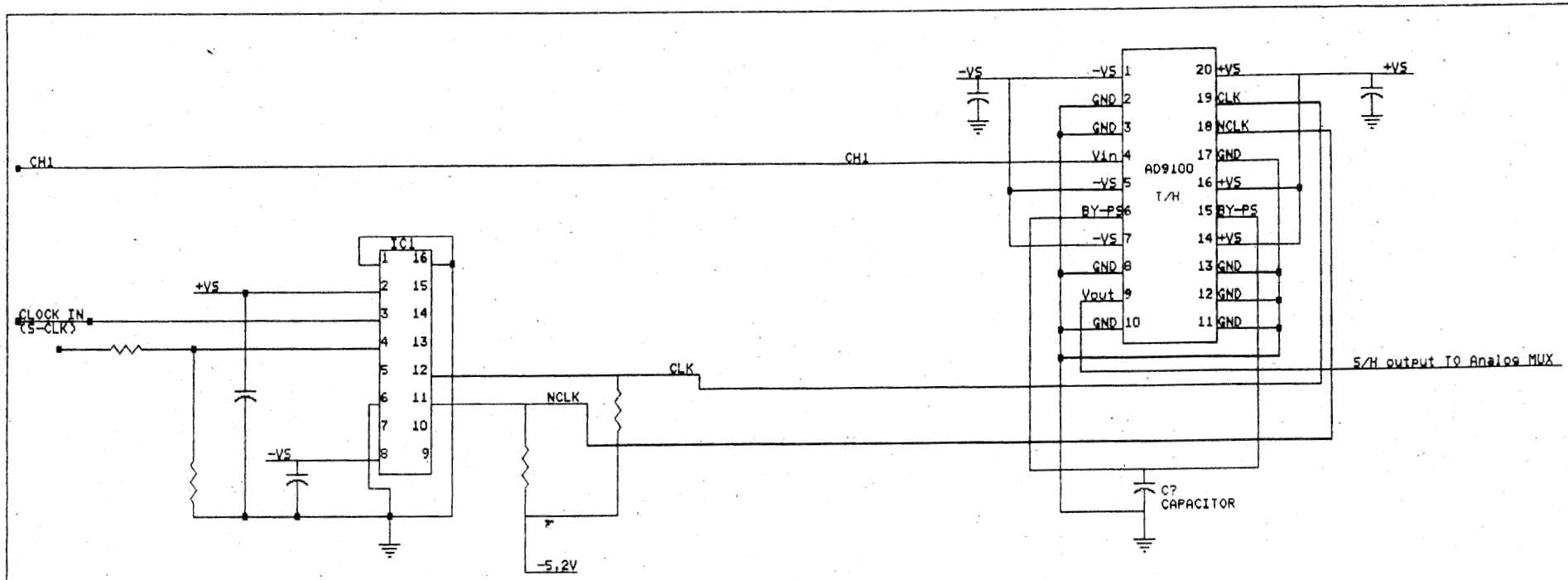
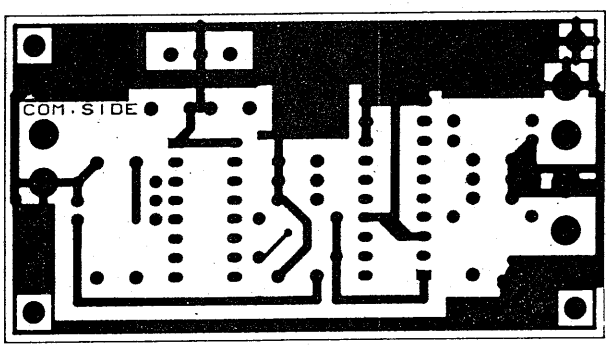
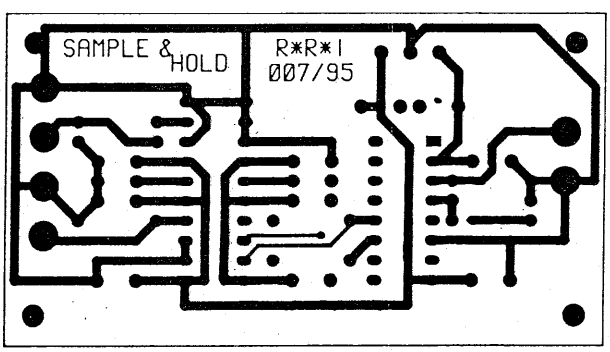

CH1
CH1
CLOCK IN
(S-CLK)
+VS
-VS
IC1
1
2
3
4
5
6
7
8
16
15
14
13
12
11
10
9
CLK
NCLK
-5,2V
-VS
GND
GND
Vin
-VS
BY-PS
-VS
GND
Vout
GND
1
2
3
4
5
6
7
8
9
10
AD9100
T/H
20
19
18
17
16
15
14
13
12
11
+VS
CLK
NCLK
GND
+VS
BY-PS
+VS
GND
GND
GND
-VS
+VS
C?
CAPACITOR
S/H output TO Analog MUX

FIG 3.1a





PCB Layout of S/H Circuit

Fig 3.1

kind of accuracy is acceptable for all practical purposes. The schematic and the PCB layout of the S/H circuit is as shown in the *fig (3.1a & b)*. Further details of the S/H AD9100 can be found in *Appendix D*.

Analog Multiplexer:

The Analog MUX will have to switch all the eight outputs of the S/H circuits to the ADC for digitizing before the arrival of the next sample pulse. This gives it an interval of 0.25μseconds to switch between two channels. This time should include all the delays involved in a MUX, like settling time and channel has a settling time of 70ns (typical), and channel switching time of 40ns (typical). The AD9300 is a 4:1 multiplexer. However, its output can be put into high impedance state. This will allow us to use two such MUXes in parallel, forming a 8:1 multiplexer. The schematic and PCB layout of the MUX are shown in *fig(3.2a & b)*. Further details of the MUX can be found in *Appendix D*.

Analog to Digital converter:

After the sample pulse is given to the S/H circuits the Analog to Digital converter will have to digitize the outputs of all the 8 channels. So the ADC will have to operate at eight times the speed of the S/H circuits. With a sampling frequency of 500 kHz given to the S/H circuits, the ADC has to therefore, operate at 4 MHz, giving the ADC a conversion time of 0.25μseconds. With this factor in view the ADC we selected was ***AD773***. It is a monolithic 10-bit, flash ADC, with a throughput rate of 18 MSPS ADC with a on board track and hold

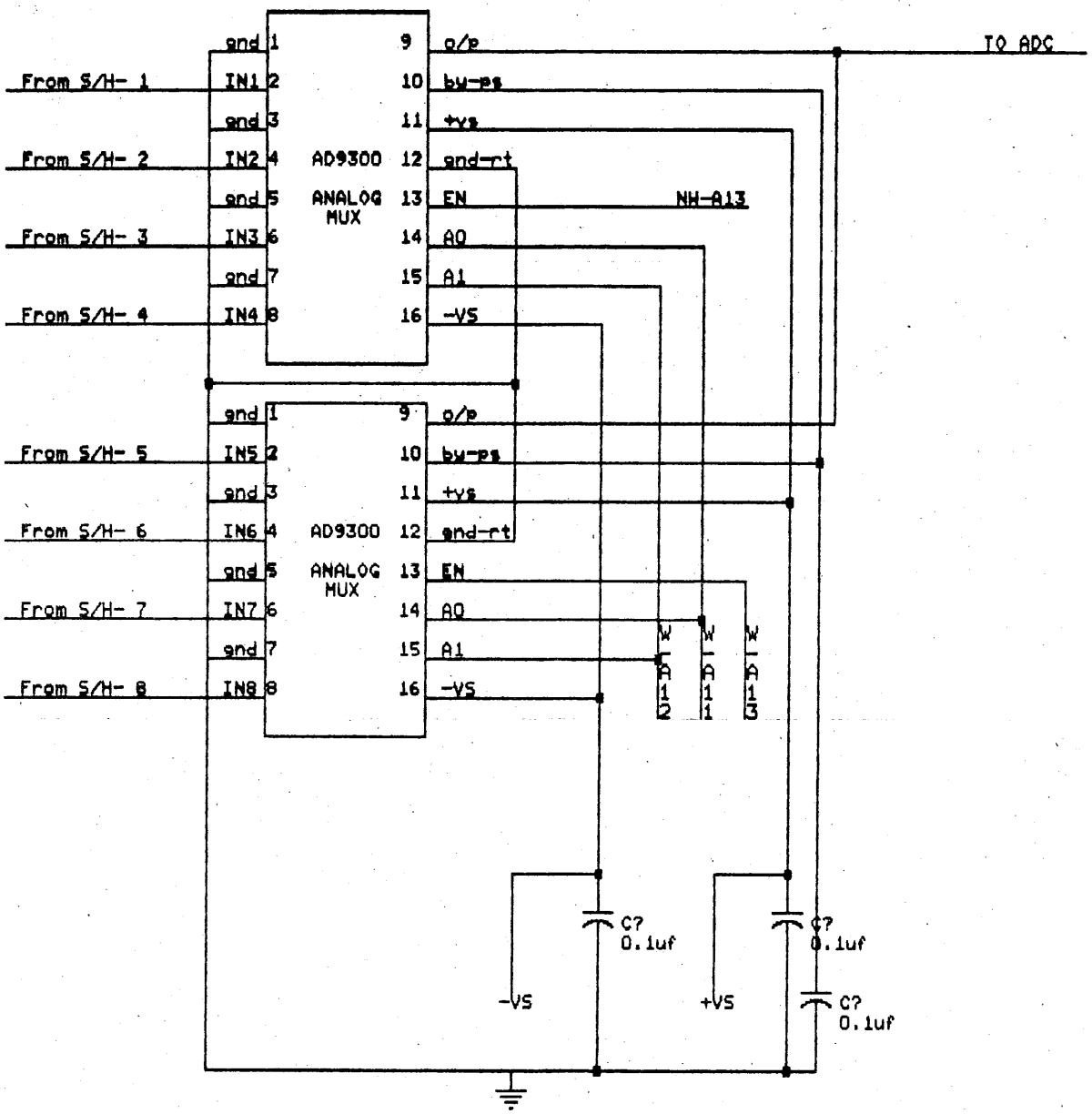
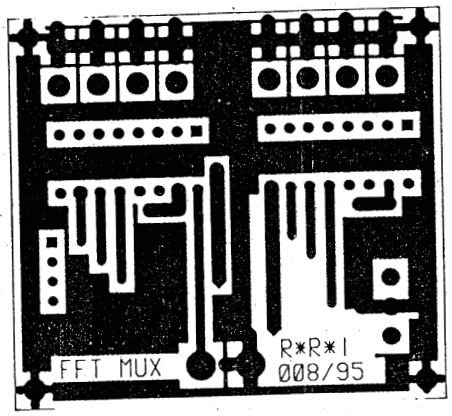
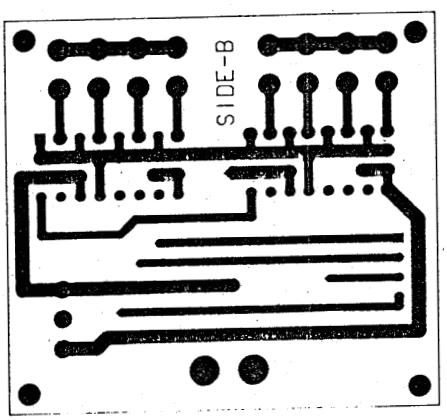

gnd 1
IN1 2
gnd 3
IN2 4
gnd 5
IN3 6
gnd 7
IN4 8
AD9300
ANALOG
MUX
9 o/p
10 by-ps
11 +vs
12 gnd-rt
13 EN
14 A0
15 A1
16 -VS
From S/H- 1
From S/H- 2
From S/H- 3
From S/H- 4
TO ADC
NH-A13
gnd 1
IN5 2
gnd 3
IN6 4
gnd 5
IN7 6
gnd 7
IN8 8
AD9300
ANALOG
MUX
9 o/p
10 by-ps
11 +vs
12 gnd-rt
13 EN
14 A0
15 A1
16 -VS
From S/H- 5
From S/H- 6
From S/H- 7
From S/H- 8
A12
A11
A13
C?
0.1uf
C?
0.1uf
C?
0.1uf
-VS
+VS

FIG 3.2a





PCB Layout of Analog MUX Circuit

Fig 3.2

amplifier. AD773 is a pipe lined device. It has a delay of four clock pulses between an analog voltage applied at its input and the corresponding digitized data appearing at its output. It has an input range of 1V (peak-to-peak). Since the resolution of a ADC is given by:

$$\textit{Resolution} = \textit{input voltage swing} / (2^n);$$

where n is the number of bits of ADC output.

This gives a resolution of (1V/(1024)

$$\textit{Resolution} = 977.4\ \mu V.$$

With a conversion time of 5.55×10^{-08}, this ADC is ideally suited for specifications imposed by the Digitizer card. The schematic of the ADC and it's PCB layout is shown in *fig (3.3a & b)*. Further details regarding AD773 can be obtained in *Appendix D.*

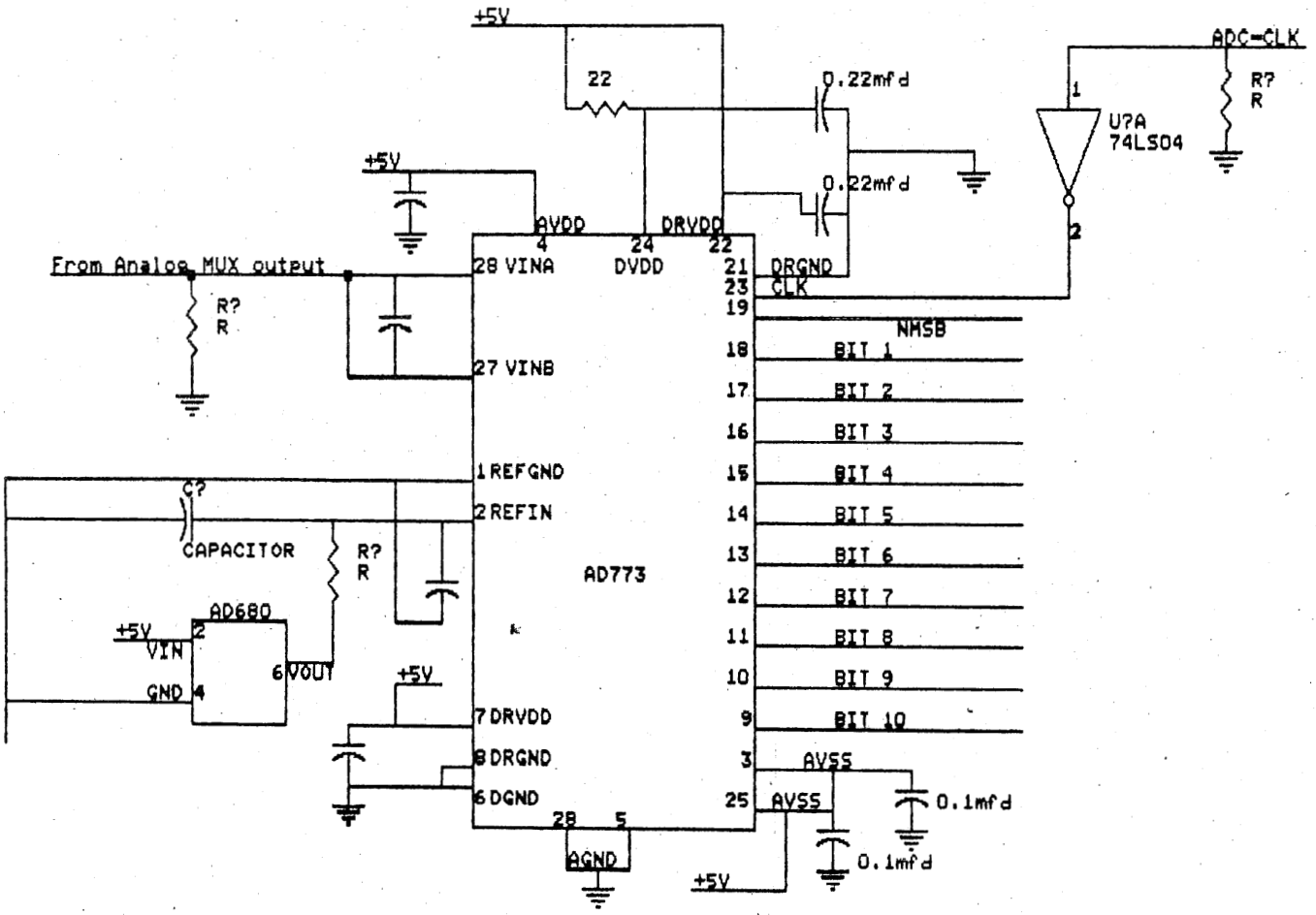


FIG 3.3a

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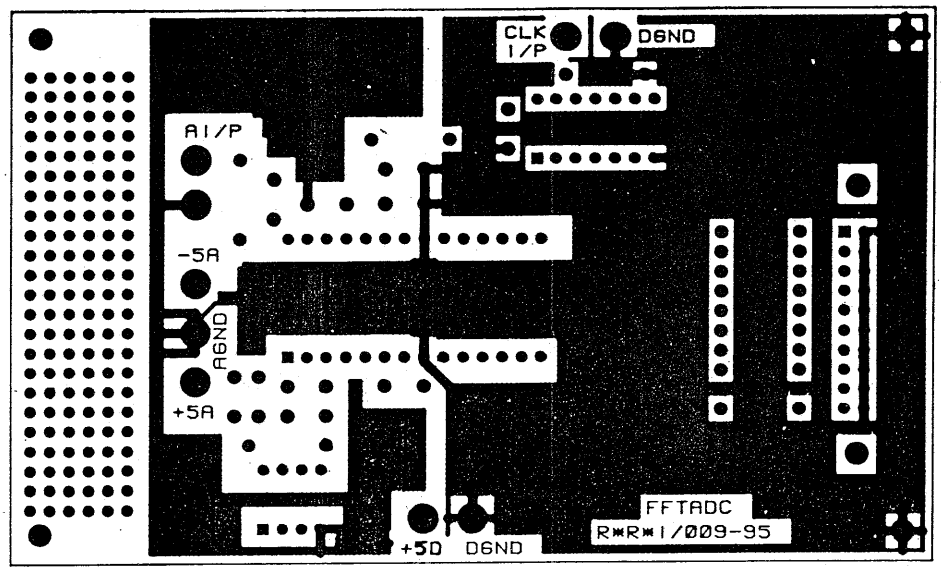
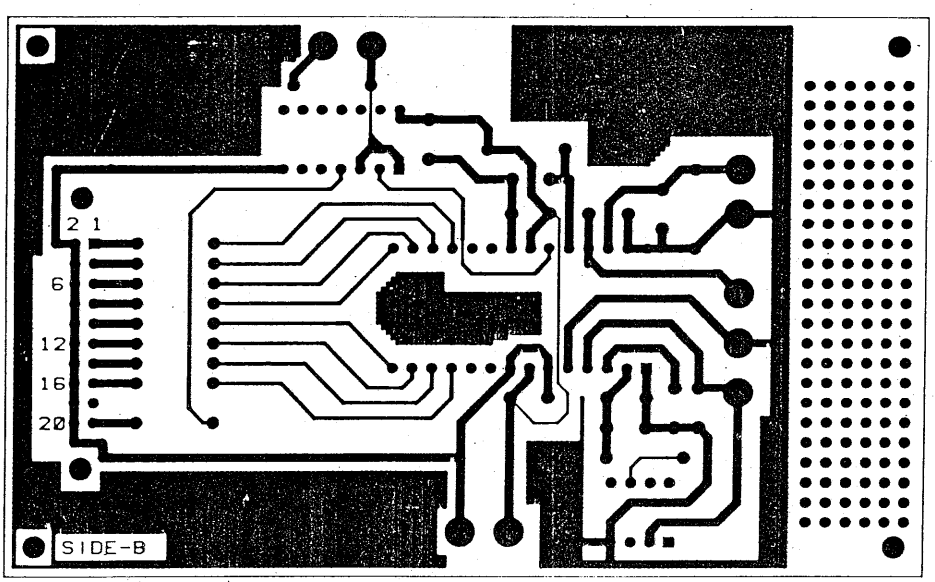




PCB Layout of ADC Circuit

Fig 3.3

3.2 BUFFERED DATA ROUTER

Spectrometric analysis of the signals received from the radio telescope is continuous process. This involves a continuous flow of data through the ***Buffered Data Router*** *(fig(3.4))*, to the FFT card. With 8 different channels involved, a rearrangement of digitized ADC output is needed. This is because the FFT chip requires the entire set of 1024 (or 512 or 256 ...) points of a single channel, given to it consecutively. But the ADC will be digitizing the signals of all the channels' one after another. So if at the n^{th} clock pulse, the digital output from ADC is from channel x (say), then at the (n+1)th clock pulse the digital output is from (x+1)th channel. If the ADC output was to be given directly to the FFT card, two consecutive data outputs from the ADC will be from two entirely different channels as shown in *fig (3.5)*. Processing of such a stream of data would lead to faulty results in the FFT output.

To sort out this problem, rearrangement of the ADC output must be performed. This task involves temporary storage of digitized data on the ***BDR***. RAMs are best suited for the job of temporary storage, when the required speed of operation and cost are taken into perspective. With the requirement of 1024 points FFT on all 8 channels, the total amount of data to be stored will be 8192 bytes, with 1kB for each channel. Data from a channel will be written into its corresponding 1kB block, after being digitized by the ADC. This stored data is then read in a stream of 1024 data points from the same channel.

To keep the data flowing ceaselessly, it must be read from and written into the RAMs simultaneously. But RAMs present a problem. At a given instant of time, they can perform

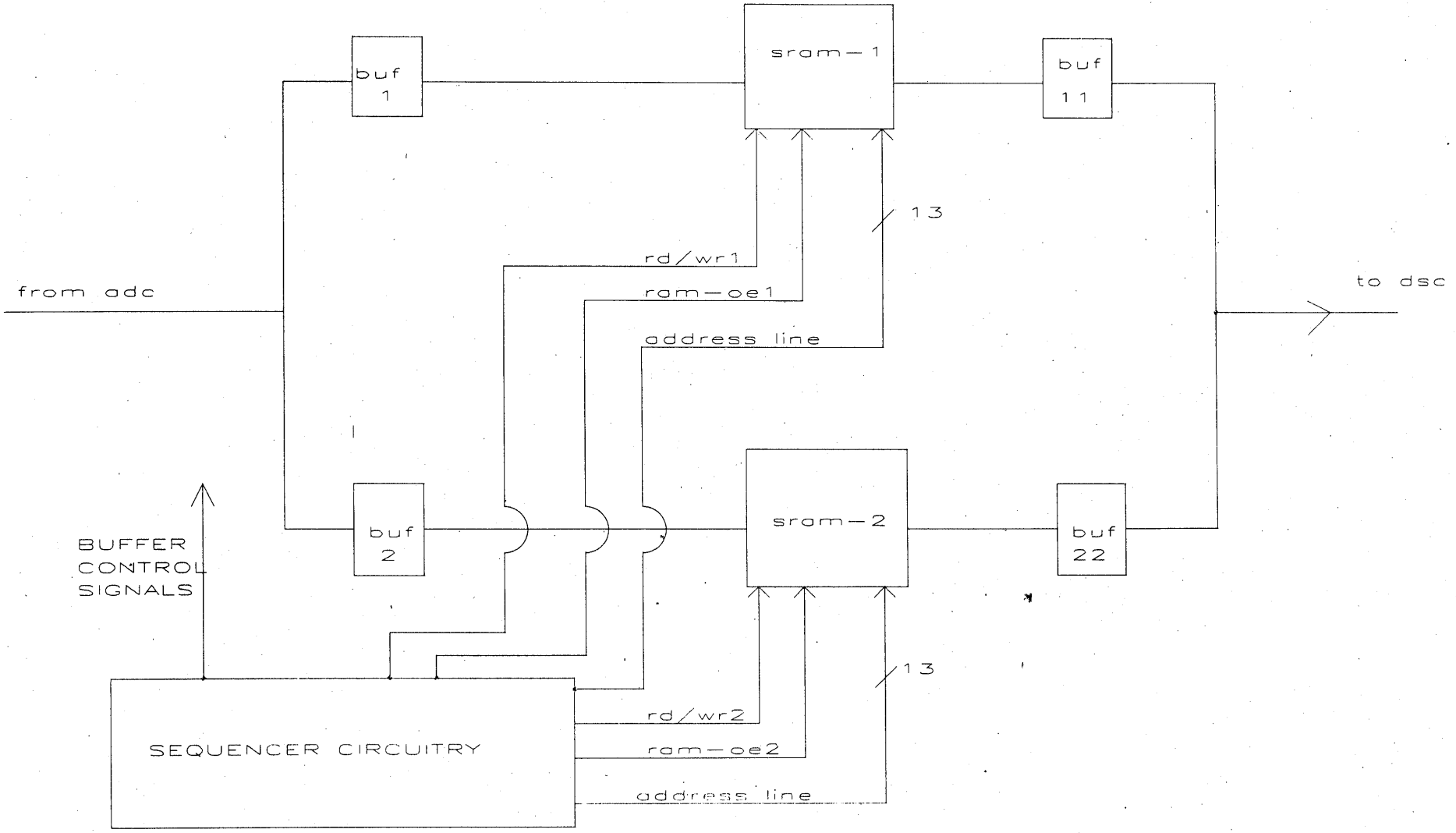

buf
1
sram—1
buf
11
13
rd/wr1
ram—oe1
address line
from adc
to dsc
buf
2
sram—2
buf
22
BUFFER
CONTROL
SIGNALS
13
rd/wr2
ram—oe2
address line
SEQUENCER CIRCUITRY

FIG 3.4

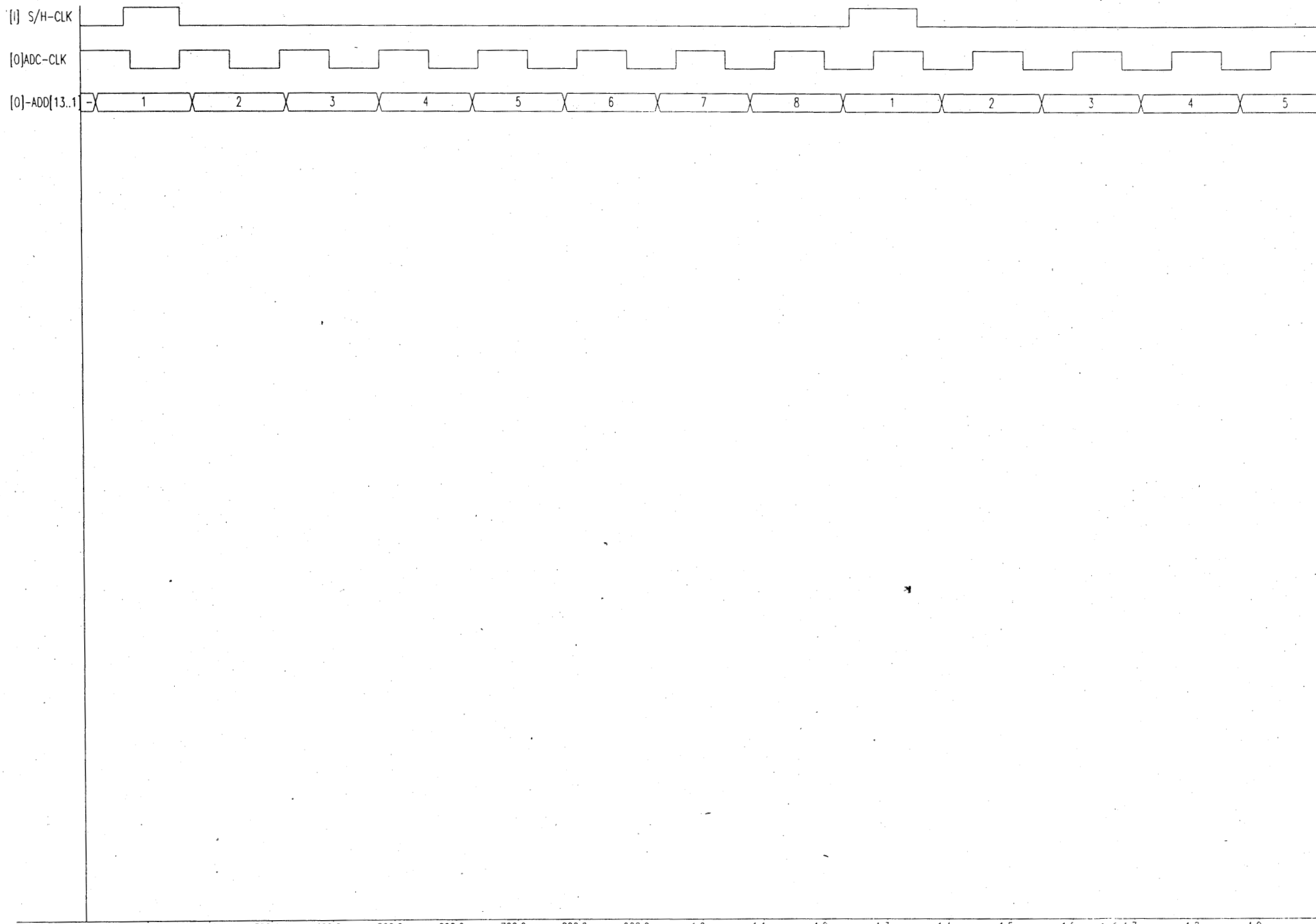

[I] S/H-CLK
[O]ADC-CLK
[O]-ADD[13..1]
1
2
3
4
5
6
7
8
1
2
3
4
5
100.0ns
200.0ns
300.0ns
400.0ns
500.0ns
600.0ns
700.0ns
800.0ns
900.0ns
1.0us
1.1us
1.2us
1.3us
1.4us
1.5us
1.6us
1.7us
1.8us
1.9us

Fig 3.5

only one task, either reading or writing. Both these operations cannot be performed simultaneously. This predicament is preempted by using two separate memories. While one of them is storing data from the ADC, the other will be sending previously stored data down to the FFT card after the required rearrangement.

To perform this prestidigitation of writing and reading data simultaneously into the respective memories and then swapping the operation, the ***Buffered Data Router*** has been used.

The BDR consists of the following blocks:

(a) Sequencer Circuit

(b) Memory banks.

3.2-1 SEQUENCER CIRCUIT:

The sequencer circuit forms the quintessence of the ***Buffered Data Router***. It functions as an address generator for the two memories and also for controlling the read and write operations of static RAMs. The ability to program the number of points and channels involved in the FFT process, is one of the feature incorporated into the ***BDR***.. This means the user will stipulate the number of points and channels. This is a vital information for the sequencer circuitry.

The inputs to the sequencer circuit are as follows:

- number of points
- number of channels
- clock
- enable signal

The stipulated number of channels and points are accepted from the user by means of a program written in C language. Using either an ISA or EISA interface card, this information is then fed to the ***BDR***.. The sequencer circuit in the ***BDR*** accepts this data and stores it in the appropriate latches.

The block diagram of the sequencer circuit is as shown in *fig(3.6)*. The sequencer circuit itself can be categorized as:

a) Address Generator and Multiplexer

b) Clock Controller

ADDRESS GENERATOR:

The address generator is used for generating address sequence for read and operations performed on the two memories. In order to access all 8k locations in the S-RAMs, a 13 bit address is required. This 13 bit address is generated by a 13 bit counter. With reading and writing address taking place simultaneously two address generators are required, namely, the read address generator and write address generator.

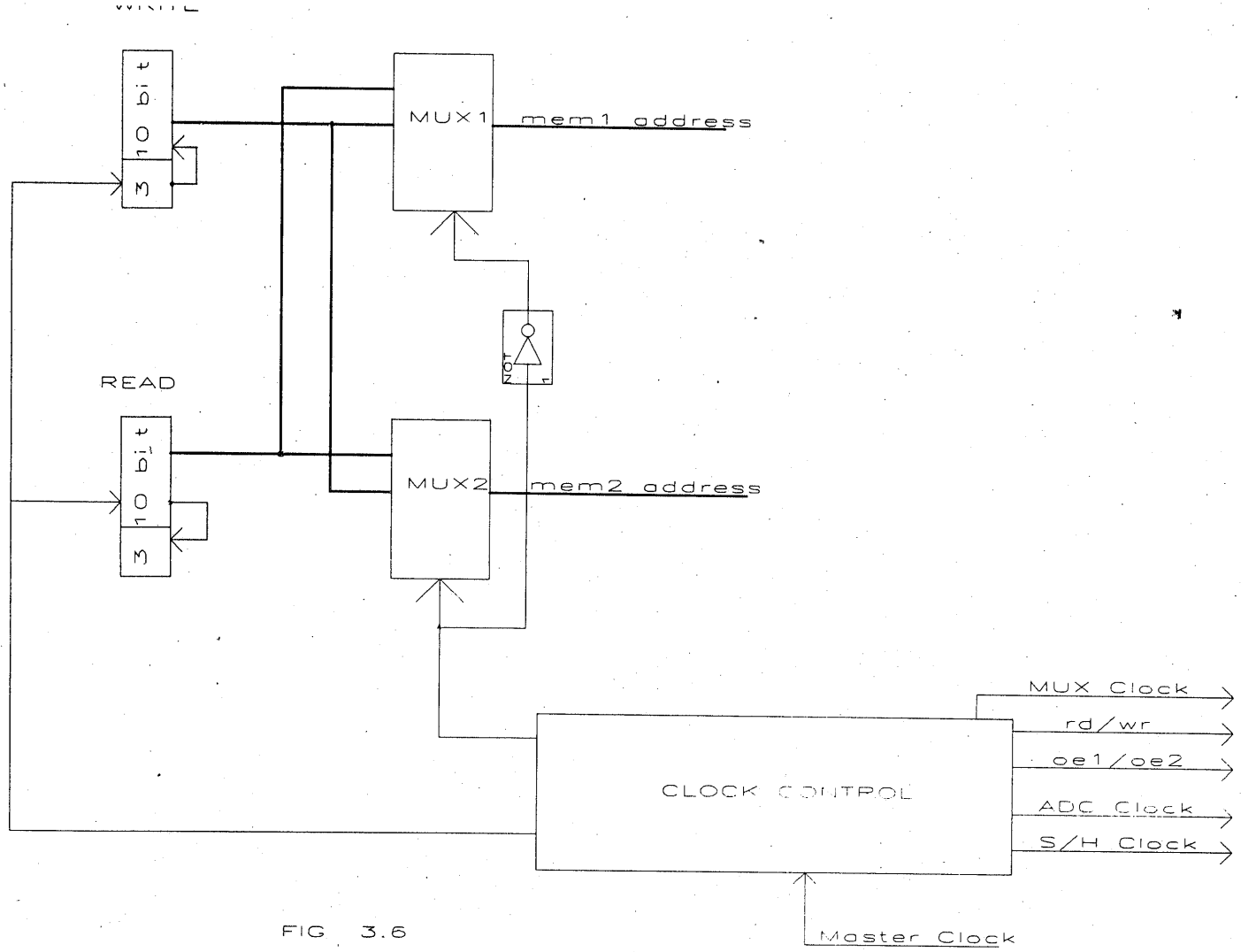


FIG 3.6

BLOCK DIAGRAM OF SEQUENCER CIRCUIT

(a) Write Address Generator:

As explained earlier, the memory is divided into eight 1 kB blocks and each 1k block is for holding data from one channel. Two consecutive outputs of ADCs are from two different channels. They need to be stored into their respective 1k blocks. Therefore at every clock pulse the write address generator has to increment itself by 1024 in order to point to the correct memory block. After storing data points from all N_c channels it will have to switch to switch to first 1k block and point to next free location in it. The sequence of write address generated is shown in *fig(3.7)*

To achieve this the write address generator is divided into 2 parts a 3 bit counter and a 10 bit counter. Both these counters are programmable. The number of points are programmed into the 10 bit counter and the number of channels are programmed into the 3 bit counter. The 3 bit counter is clocked by the master clock. At every clock pulse, it's incremented by one. The significance of this 3 bit counter, is that the 13 bit address is incremented by 1024 at every clock pulse. After being through with all the channels, this counter is reset. This reset pulse clocks the 10 bit counter and is incremented by one, thereby pointing to next location in the memory of the first 1K block.

The write address generator circuit is shown in the overall circuit diagram. *Refer to fig(3.9)*

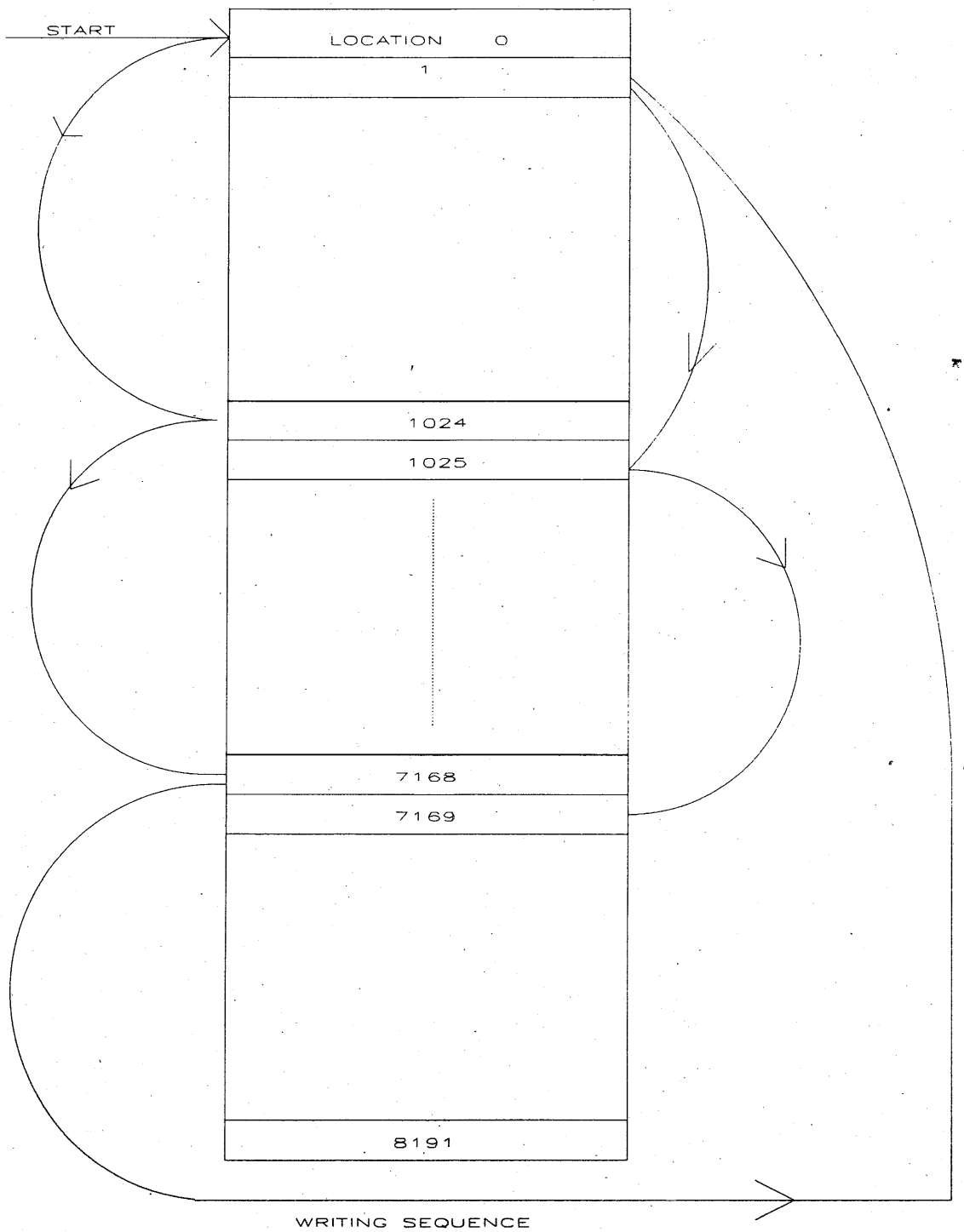

START
LOCATION 0
1
1024
1025
7168
7169
8191
WRITING SEQUENCE

FIG 3.7

(b) Read Address Generator:

The data stored in the memory has to read out sequentially into the FFT card. All data points stored in one 1k block, which corresponds to the data from one channel, are read first before going over to the next 1k block and the process is repeated.

This means that the address pointer has to be incremented by one at every clock pulse and after reading N_p points, has to be incremented to the starting position of next 1k block. The sequence of read address generated is shown in *fig(3.8)*.

In order to achieve this sequence of addressing the address generator is built by cascading 10 bit and 3 bit counters. But in this case the 10 bit counter is clocked by the master clock. This will cause the address pointer to be incremented by one at every clock. When the output of this counter is clocks the 3 bit counter.

Hence, the address generator will now point to the starting location of the next 1kB block. The read address generator circuit is shown in the overall circuit diagram. *Refer to fig(3.9)*

Address Multiplexer:

With both S-RAMs involved in read and write operations, the two of them will have to be provided with both the read and write address sequences. So the outputs of the two address generators are time multiplexed, and the outputs of the multiplexer forms the address bus of the two memories. The control bits for the multiplexer are provided by the status registers.The address multiplexer is as indicated in the overall circuit diagram. *Refer to fig (3.9).*

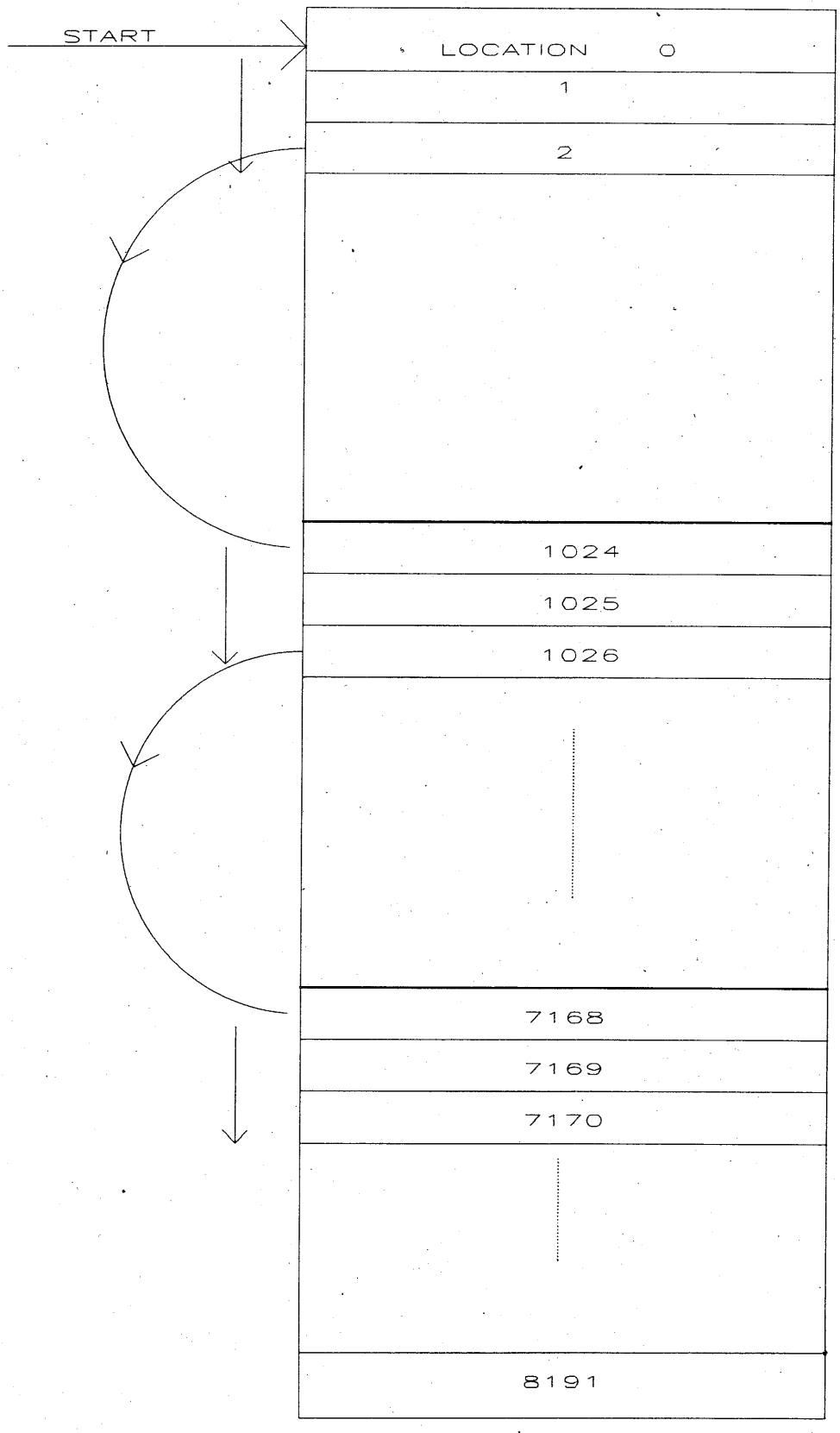
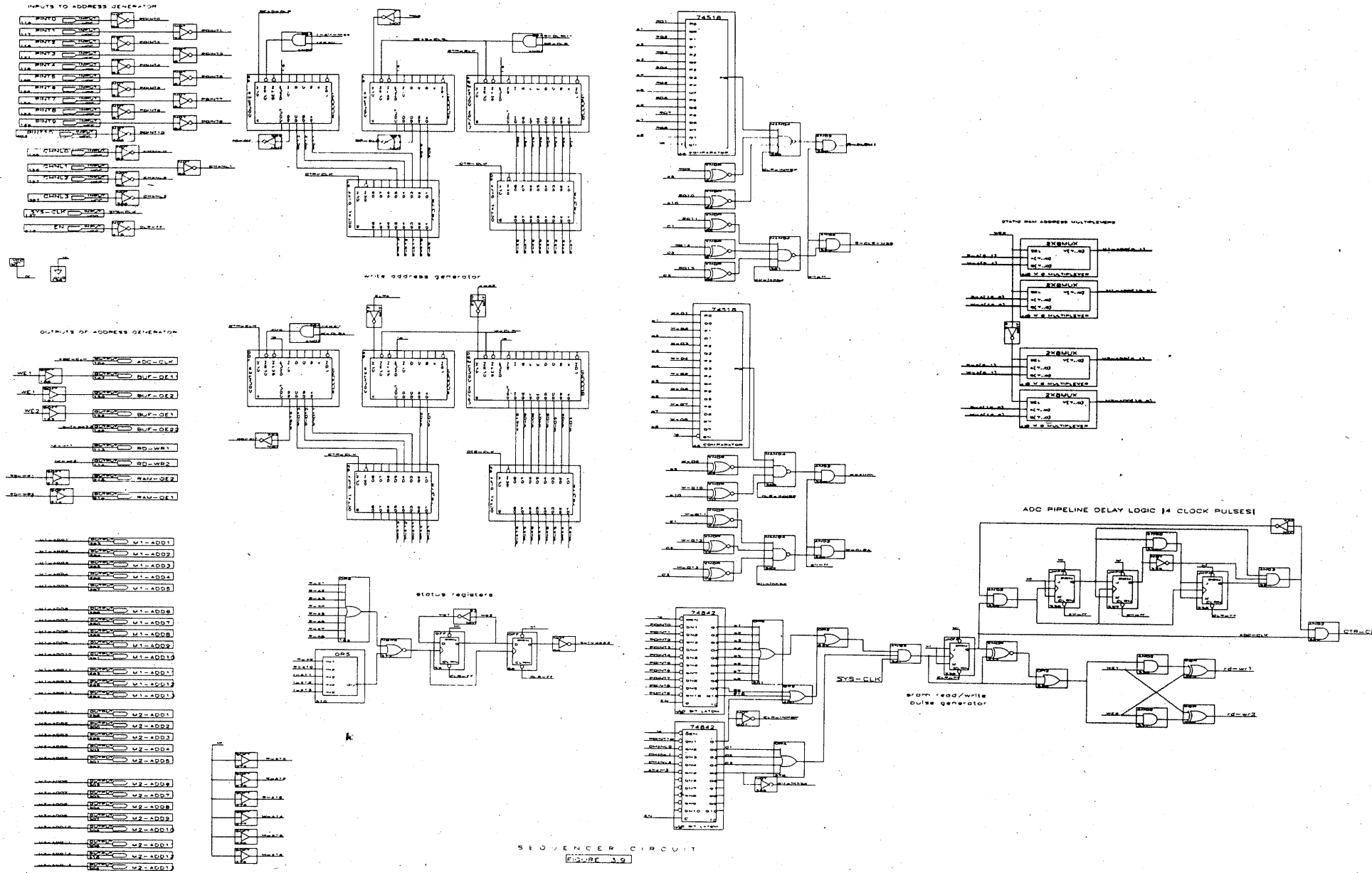

START
LOCATION 0
1
2
1024
1025
1026
7168
7169
7170
8191
READING SEQUENCE

FIG 3.8



SEQUENCER CIRCUIT

FIGURE 3.9

3.3 CLOCK CONTROL CIRCUIT:

The clock control circuit is used for providing appropriate clock pulses to the various functional blocks. It is fed with a master clock from an external circuit. The clock signals provided are :

- **Memory address clock:** clock for the memory address generators.
- **Read and Write control signals:** enabling signals for the S- RAMs and buffers.
- **Clock Control for Analog circuitry:** clocking pulses for the ADC, sampling clock for sample and hold circuits.

The method of generation of various signals is represented schematically in *fig(3.10)*.

Clock for Memory Address Generators:

The ADC being a pipe lined device has a delay of 4 clock pulses, between an analog signal being given at its input and the corresponding digitized data appearing at the ADC output. The digital data from the ADC is then written into SRAMs. So the address generators used for generating writing address should start only after this delay. A 3 bit synchronous self stopping counter is used for this purpose. The output of this counter is decoded and used to enable clock to the address generator.

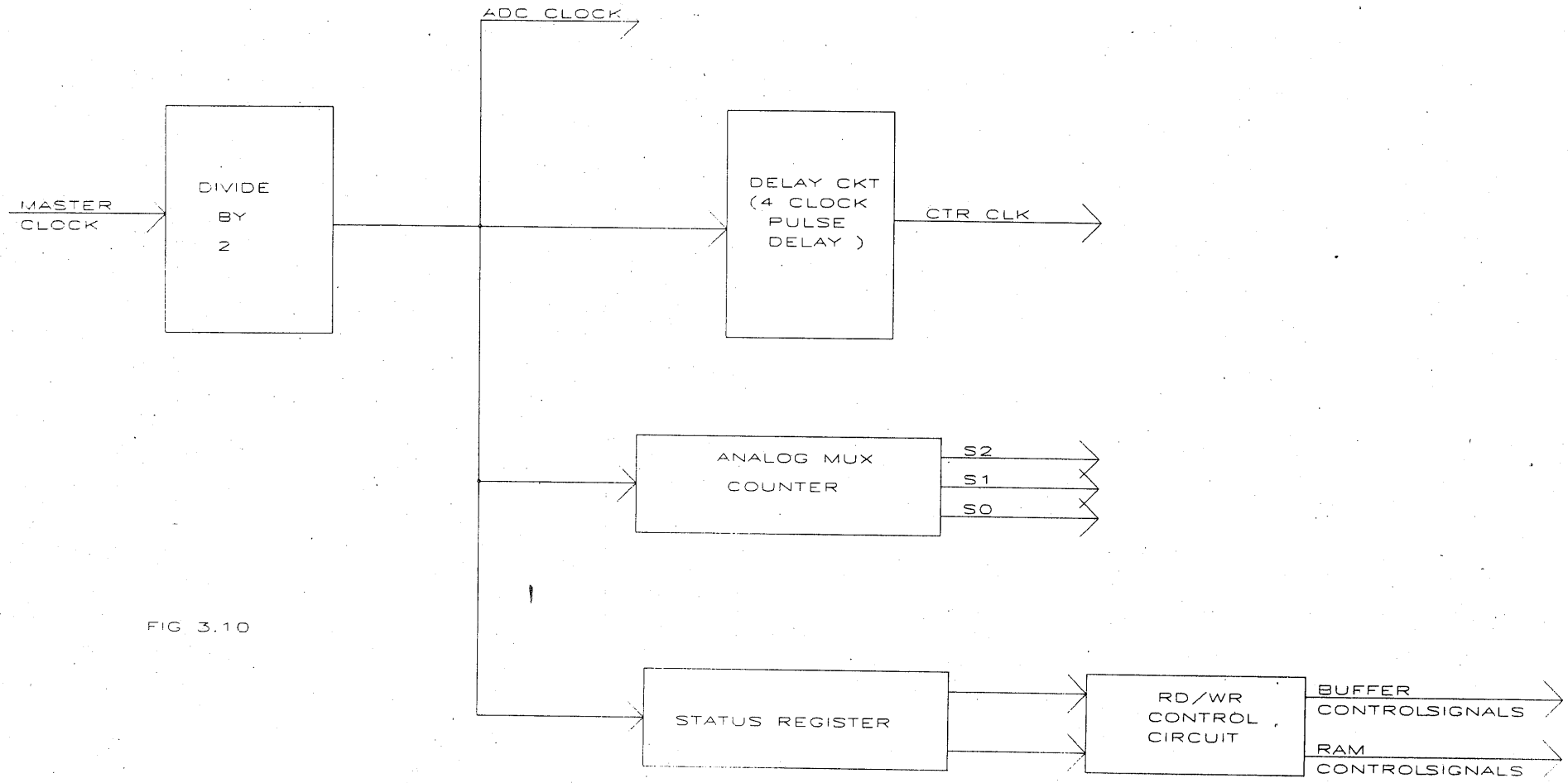

ADC CLOCK
MASTER CLOCK
DIVIDE BY 2
DELAY CKT (4 CLOCK PULSE DELAY)
CTR CLK
ANALOG MUX COUNTER
S2
S1
S0
STATUS REGISTER
RD/WR CONTROL CIRCUIT
BUFFER CONTROLSIGNALS
RAM CONTROLSIGNALS

FIG 3.10

At the time of power up or any ensuing initialization of the ***BDR*** this 3 bit counter is also cleared. It then accumulates 4 counts. On the 5th pulse this counter is stopped and the clock to the read and write address generator is enabled. The appropriate waveforms are indicated in *fig(3.11)*.

Read/Write Control Signals:

The two SRAMs and their associated buffers need control pulses, like output enable, write enable etc., for their operation. The read write controller in the clock control circuit generates these control pulses. The operation of each control pulse is discussed below briefly.

- **BUF-OE**: It is used to control the output of the buffer. When BUF-OE is low, output of the buffer is enabled and with BUF-OE high, the output is tri-stated.
- **RAM-OE**: This signal enables the output of the SRAMs. With RAM-OE low the data can be read out of the memory and if it is high the memory may be used for writing (if WR = 1). If RAM-OE is high output of memory will be tri-stated.
- **RD/WR**: This signal controls the state of the SRAMs, that is, it decides whether data can be written into the SRAM or read from it.

The read write controller logic circuit is indicated in the overall circuit diagram. The two D type flip-flops are so connected that their outputs are perpetually complements of each

status registers
R_41
R_42
R_43
R_44
R_45
R_46
R_47
R_48
OR8
R_49
R_410
R_411
R_412
R_413
OR5
OUT
ZOR2
DFF
D
PRN
CLRN
Q
CLR_FF
HI
we1
we2
NOT
hi
ZOT
bus_oe22

other. Their outputs have been used to dictate the generation of the control pulses and thereby decide the status of the two memories (which is why the two of them together have termed as status registers). In fact, they give a clear indication of which memory is in read cycle and which is in the write cycle.

The RD/WR and RAM-OE signals should be pulses of duration less than the clock given to the counter to, prevent data being duplicated or overwritten in the memories. Different conditions resulting from different values of WE_1 and WE_2 are discussed below briefly:

- **$WE_1 = 0$ and $WE_2 = 1$**: With $WE_1 = 0$ AND_1 is disabled and AND_2 is enabled. The output of the XOR_2 will be same as the pulse given to AND_1 (since $WE_1=0$). The output of the XOR_1 will be continuously high ($WE_2 = 1$).
- **$WE_1 = 1$ and $WE_2 = 0$:** With $WE_1 = 1$ AND_1 is enabled and AND_2 is disabled. The output of XOR_1 will be pulsating and output of XOR_2 will be in high state continuously.

The RD/WR_1 and RD/WR_2 signal are also used to control the output of $SRAM_1$ and $SRAM_2$.

The logic discussed above has been programmed into EPM 7128LC84. The details of which are provided in the *Appendix D*. The final schematic of the ***BDR*** is also included in the following page.

Analog clock Generators:

There are three signals that the digital control circuits have to provide the analog part of the circuit with, namely:

- **ADC clocking**
- **Analog MUX selection**
- **Sampling clock for sample and hold circuits**

The ADC clock frequency is same as the memory address clock frequency. It is directly provided by the clock controller.

The Analog MUX selection bits are generated by a 3 bit synchronous counter, which is clocked by ADC clock. Since this MUX has to switch between the selected number of channels, the counter has been made programmable. As earlier the PC, during the time of initializing the ***BDR*** card programs this counter also. The sampling clock is the signal given to the sample and hold circuits for putting them into the hold state. It is generated at the of $(1/N_c)$ times the ADC clocking frequency, where N_c is the number of channels input.

The circuit diagram of the analog clock control circuit is shown in *fig(3.12)*.

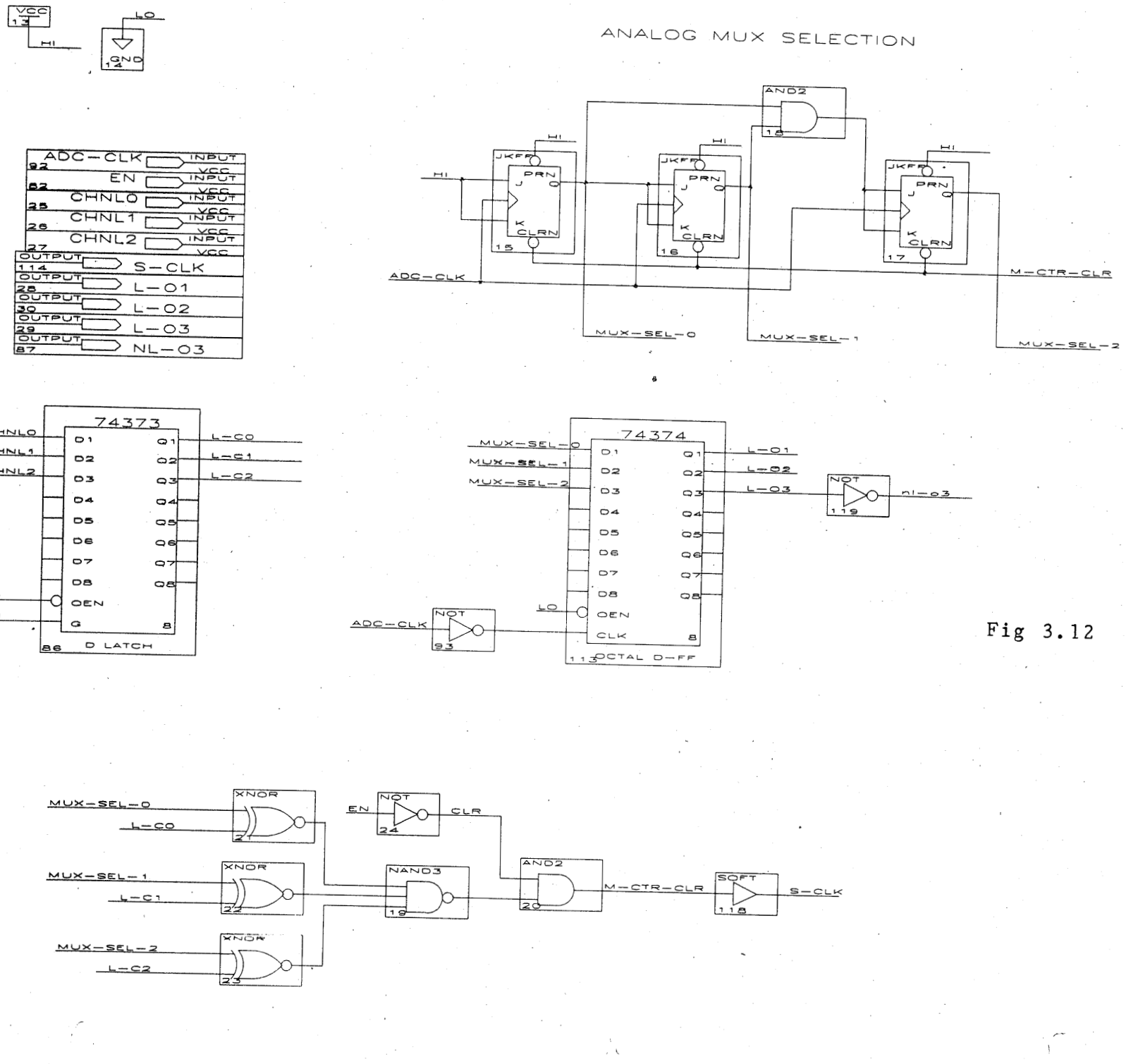

ANALOG MUX SELECTION
VCC
13
HI
GND
14
LO
ADC-CLK INPUT
92
EN INPUT VCC
82
CHNL0 INPUT VCC
25
CHNL1 INPUT VCC
26
CHNL2 INPUT VCC
27
OUTPUT 114 S-CLK
OUTPUT 28 L-01
OUTPUT 30 L-02
OUTPUT 29 L-03
OUTPUT 87 NL-03
AND2
18
JKFF
PRN
CLRN
15
16
17
ADC-CLK
M-CTR-CLR
MUX-SEL-0
MUX-SEL-1
MUX-SEL-2
74373
CHNL0
CHNL1
CHNL2
D1
D2
D3
D4
D5
D6
D7
D8
OEN
G
Q1
Q2
Q3
Q4
Q5
Q6
Q7
Q8
L-C0
L-C1
L-C2
LO
EN
8
86
D LATCH
74374
MUX-SEL-0
MUX-SEL-1
MUX-SEL-2
L-01
L-02
L-03
NOT
119
NL-03
ADC-CLK
93
CLK
113
OCTAL D-FF
XNOR
MUX-SEL-0
L-C0
21
EN
NOT
24
CLR
MUX-SEL-1
L-C1
22
NAND3
19
AND2
20
M-CTR-CLR
SOFT
118
S-CLK
MUX-SEL-2
L-C2
23

Fig 3.12

MEMORY BANK:

The memory bank consists of two HY62C256/L ICs which are 32,768 word by 8-bit CMOS Static RAMs, of which only 8k have been put to use. The HY62C256/L has a typical access time of 100ns. The need for two such devices has been explicitly explained in previous chapters. Further details about HY62C256/L can be found in *Appendix D.*

CHAPTER FOUR

TESTING AND CONCLUSION

4.1 TESTING OF DIGITAL CONTROL LOGIC

First the logic of the control system implemented using EPLD are tested. This is done by entering the required logic in to the graphic editor file of MAX + PLUS-2 (details of MAX +PLUS II are in *Appendix C* and then simulating its functioning. Two levels of simulation are done:

Software Simulation: It is done before programming the logic into the EPLD. The desired inputs to the EPLD are entered into a simulator file as waveforms. The logic simulator on MAX + PLUS-2 is then used to run a simulation of this file. The simulated outputs are observed in the simulator file. It is found to be in agreement with the desired results.

Hardware Simulation: The logic discussed earlier in *chapter 3* is fused into a EPLD (EPM 7128) by the programmer of MAX + PLUS-2. For this the EPLD is placed in the MAX + PLUS-2 programming module. The programmed EPLD is now used to perform hardware simulation, i.e., the input signals (entered in simulator file) are generated from the PC and sent to the EPLD (placed in the adapter module). The EPLD outputs are monitored and this outputs are found to match with software output.

Testing Details:

The buffered data router being developed is a prototype board. It is therefore first implemented on general purpose PCB. This would help us make modifications, if necessary, in case of bugs found in the circuit, which would be a trouble-some process with a custom made PCB.

Due to the non-availability of the required analog components at the right time, the Analog conditioning and digitizer circuit could not be implemented. So it was decided that the **BDR** and its associated control logic must be tested independent of these analog components.

This can be achieved by a digital circuit that would simulate the output of the ADC. The output of such a digital circuit should preferably sequential and synchronous with the **memory address clock**. This will allow us to predict the output of the data router card effectively.

The digital circuit involved is a simple 3 bit counter. This 3 bit counter, called the test counter, is clocked at the same rate as the address generators (with necessary compensation for ADC pipe line delay).

Since the DSC itself is PC based, it is only apt that this project, the buffered data router is also PC based. The PC is used to initialize the Buffered Data Router (**BDR**), during which the number of channels and number of points the user specifies are loaded into the card. The interface between the PC and the **BDR** CARD is a 48 line I/O port (a 8255 based card, containing two 8255A chips). The card details can be obtained in *Appendix D.*

The 48 lines of the 8255 card have been split into two groups (1) 24 lines for input (2) 24 line for output. Out the 24 output lines 16 have been used: 11 for loading number of points, 4 for loading number of channels, one line for sending the enable pulse at the time of initialization.

Initializing the **BDR** and configuring the ports of I/O card is accomplished by a program written in C language. The program source code is given in the following page.

The program itself is user friendly and interactive. The tasks of initialization, acquisition and browsing of acquired data have been made very simple with self explanatory menus.

Incidentally, a second 8 bit bus from the **BDR** sends the output data from the data router to the PC via the input port of the 8255 I/O card.

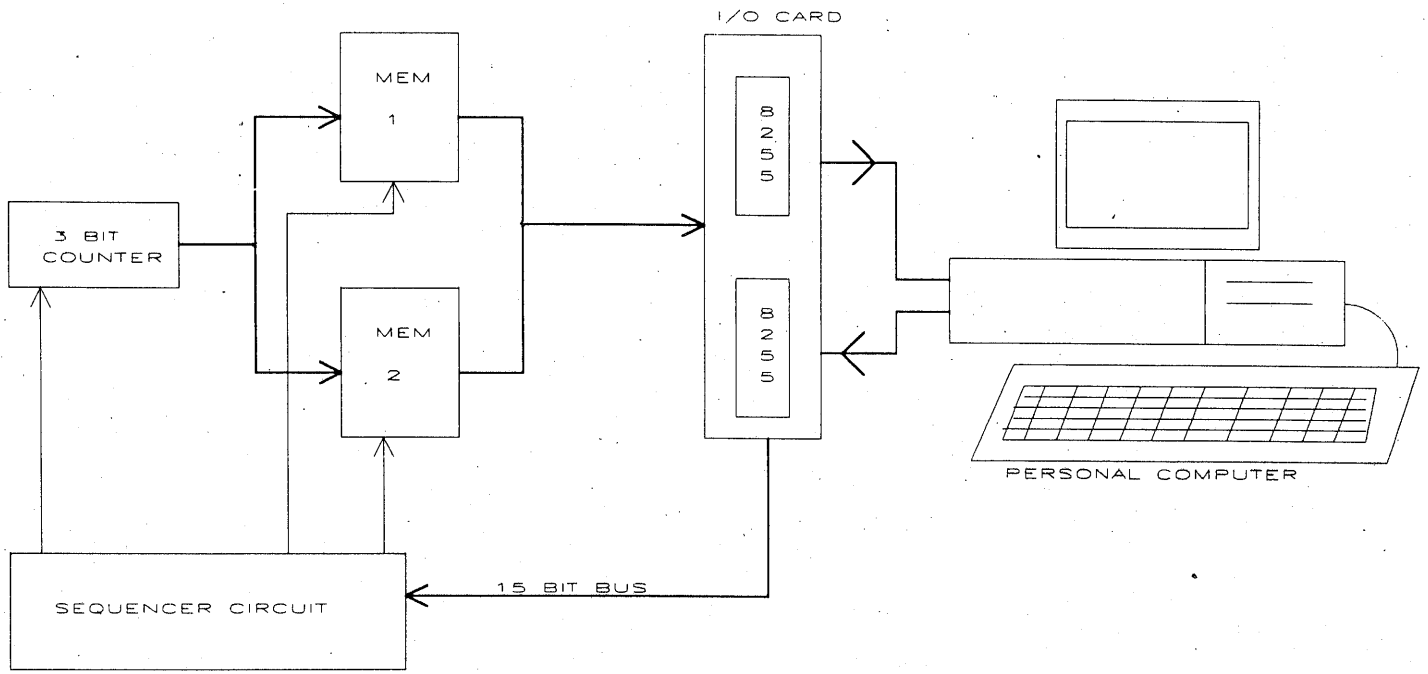
With write address being incremented by 1024 at every clock pulse (while the test counter is incremented by 1), a different number is written into each 1 kB block of the 8 kB memory. The numbers stored adjacent memory block will therefore differ by one. The data stored in memories are read out sequentially. Thereby reading all the number stored in a 1k block before going over to the next (1k block). The output sequence can now predicted. Each number is number will be repeated N_p number of times. The block diagram of the test circuitry is shown in *fig(4.1)*.

The PC clock and clock given **BDR** being different will not be synchronous. So the data output from **BDR**, may not be synchronized with the inport instruction executed by the

```
# include <stdio.h>
# include <conio.h>
# include <dos.h>
# include <time.h>

# define TRUE    1
# define FALSE   0

static int arr[8192],flag=1,lflag=FALSE,pjunk=0,col,temp;
unsigned int points=1025,temp_points,chanls=9;
unsigned int byte_1=0x00ff,byte_2=0x000f;

void main()
        {
        clrscr();
        accept_pts_chnls();
        load_card();
        acquire_data();
        save_file();
        }

/*---------------------- accept_pts_chnls() ----------------------*/
accept_pts_chnls(void)
        {
         lflag = FALSE;
         points=1025;
         chanls=9;
         byte_1=0x00ff;
         byte_2=0x000f;

         while (points < 0 || points > 1024)
                {
                gotoxy(21,11);
                printf("Enter the no. of points [Max-1024] : ");
                scanf("%4d",&points);
                }
         temp_points=points;

         while (chanls < 0 || chanls > 8)
                {
                gotoxy(25,11);
                printf("Enter no. of chanls [Max-8] : ");
                scanf("%1d",&chanls);
                }
```

```
          byte_1=byte_1 & points;
          byte_2=byte_2 & chanls;
          byte_2=byte_2 << 3;
          points=points >> 8;
          byte_2=byte_2 | points;
          gotoxy(22,4);
          lflag = TRUE;
          return;
         }
/*--------------- END OF FUNCTION ACCEPT_PTS_CHNLS ------------*/

/*------------------------- LOAD CARD() -------------------------*/
load_card(void)
{
   /*   port addresses
        PORT A -- 0x600
        PORT B -- 0x601
        PORT C -- 0x602
        CONTROL PORT 0x603
   */
        outportb(0x603,0x80); /* configure all the
                                 ports of 8255 as outputs */
        delay(1);
        outportb(0x602,0x00); /* initially make EN low */
        delay(1);

        outportb(0x600,byte_1);  /* output npint and nchnl
                                    to the card. */
        delay(1);
                                 /* PA7  PA6  PA5  PA4  PA3  PA2  PA1   PA0 */
        outportb(0x601,byte_2); /*  7    6    5    4    3    2    1    NPINT0 */
        delay(1);
                              /*  PB7 PB6 PB5 PB4   PB3      PB2 PB1 PB0 */
                              /*      3   2   1     CHNL0    10  9   NPINT8 */
        outportb(0x602,0xff);    /* now make EN high */
        delay(1);
        return;
}
/*---------------------- END OF FUNCTION LOADCARD -----------------*/
```

```
/*---------------------- ACQUIRE DATA() -------------------------*/
acquire_data(void)
{
        int s;
        outportb(0x607,0x9b);
        gotoxy(9,18);

        textcolor(YELLOW);
        gotoxy(10,20);

        outportb(0x602,0x00);  /* make EN low */
        delay(1);
        for(s=0;s<8192;s++)
        {
                while(inportb(0x606)==0);
                arr[s]=inportb(0x604);
                if(s%130==0)
                   cprintf("%c",219);
                while(inportb(0x606)!=0);
        }
        return;
}
/*--------------------- END OF FUNCTION ACQUIREDATA -----------*/

/* ------------ UDF : Saves data acuired from memory ---------*/
save_file(void)
        {
        auto int h;
        FILE *fptr;
        fptr = fopen("sample.dat","w");
        cprintf("   Downloading data from SYSTEM RAM    ");
        gotoxy(19,14);
        cprintf("         to a new file SAMPLE.DAT .     ");
        gotoxy(19,15);
        cprintf("           Please wait.....             ");
        for(h=0;h<=8191;h++)
        {
                fprintf(fptr,"%d ",arr[h]);
                if((h+1)%temp_points==0) fputc('\n',fptr);
        }
        fclose(fptr);
        return;
        }
/* ---------------------------- END ----------------------------*/
```



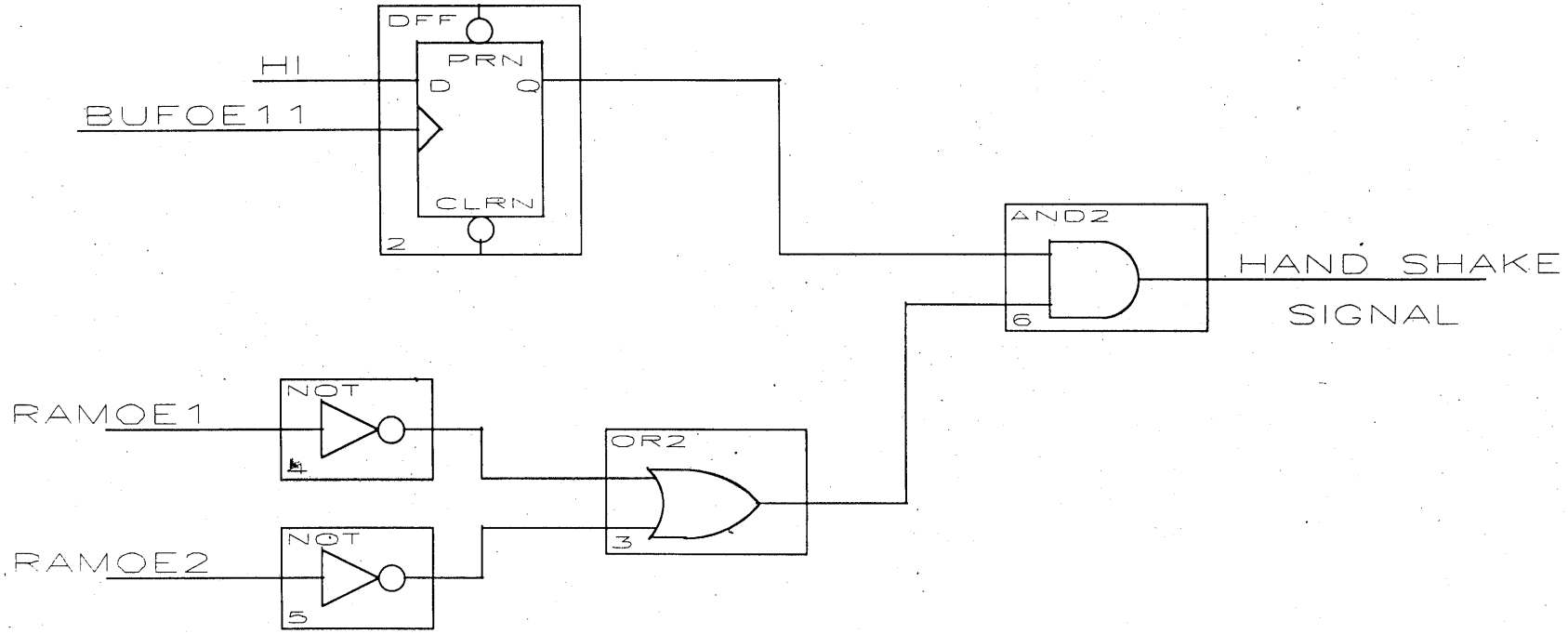
BLOCK DIAGRAM OF TESTING SET – UP.

FIG 4.1

PC. This leads to the same data being read twice or it being completely lost. To overcome this problem, the synchronization circuit is used period. The output enable signal of the two SRAMs has been used to generate a **Data Ready Signal (DRS)** as shown in *fig(4.2)*. This would inform the PC when fresh data has been put on the data bus. Care has also been to taken to prevent acquisition of data during the very first write cycle when the content of the one of the memory chips is invalid. The program will polling for this data ready signal and acquires a data point, at every DRS. This forms the necessary hand shake signal between the **BDR** and the host CPU or the DSC.

This data is stored in the memory of the PC, which can be down loaded into a file, in ASCII format, if the user so wishes. This allows for storing away the acquired data in the hard disk for later use. Since the data is stored in ASCII format any text editor can be used to view the contents of the file.

The ***Buffered Data Router*** was tested extensively in the afore said method. The card performed according to the specifications.



CIRCUIT DIAGRAM OF SYNCHRONISATION CIRCUIT

FIG 4.2

CONCLUSION

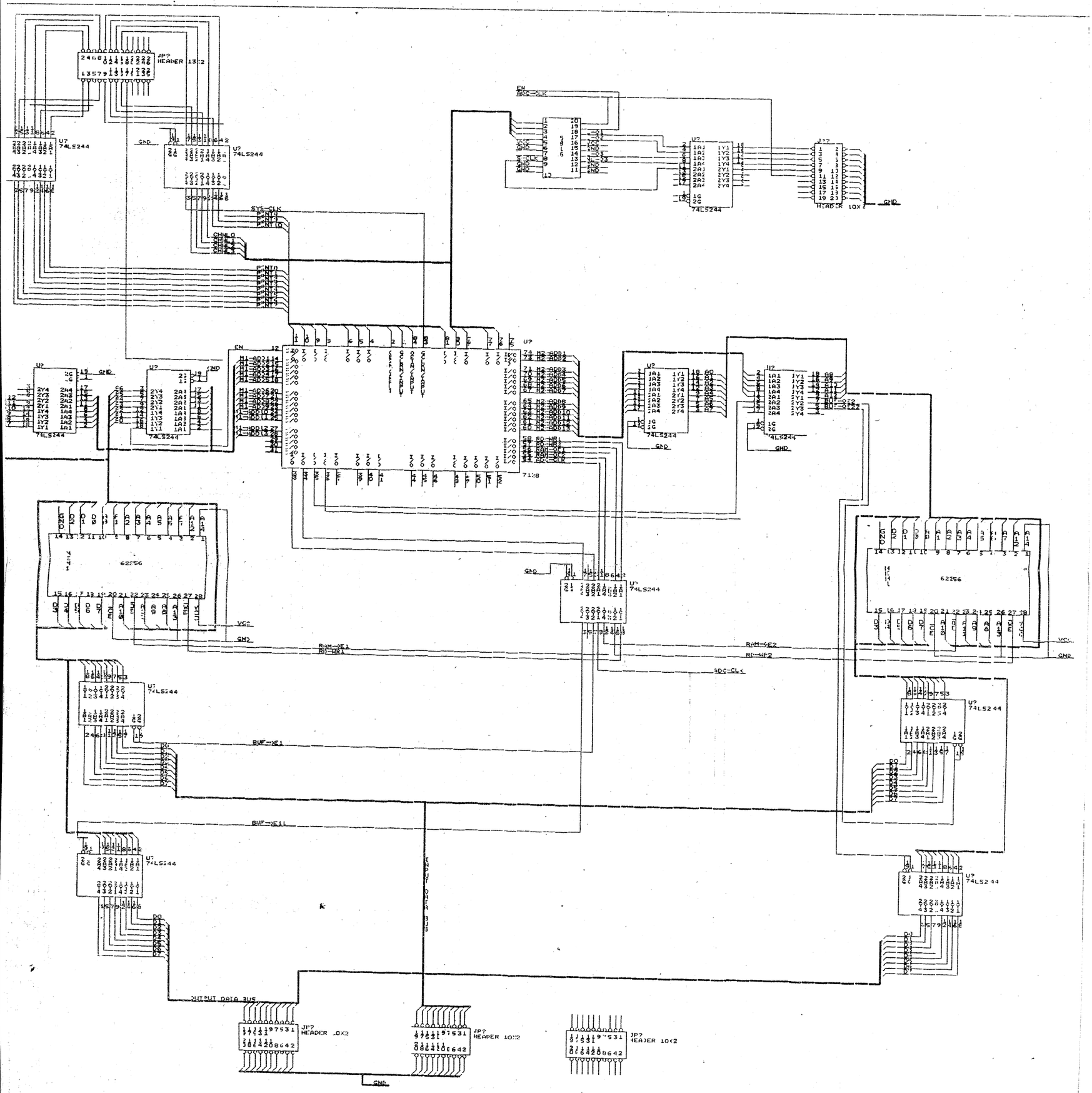
The Multi channel digitizer card combined with the Buffered Data Router is a versatile tool in the field of data acquisition systems. It has ability to be programmed through a IBM 80x86 PC, with the help of menu driven program.

The most important feature of the Buffered Data Router, is that it can effectively convert a single DSC into a multi-channel one, without affecting the speed of the DSC. It can assist in General Spectral Analysis apart from using it for studying CRRLs.

The Analog Multiplexer forms a bottleneck in the entire system, with its high settling time. This again can be remedied easily, because this circuit has also been implemented on a separate PCB.

A very high speed ADC has been included into the circuit, on a separate PCB. The speed of the ADC is sufficing for all practical purposes. But in the future, if the need be, the ADC can be replace with a faster one, on availability of such a device.It can also be function as a laboratory spectrum analyzer.

Other than that the system can perform as a multi-channel data acquisition system. A data ready signal incorporated into the system can be used for synchronizing the board with the next stage.



APPENDIX A

GEETEE

The Gauribidanur Radio Telescope is of the ARRAY type operating at 34.5 MHz center frequency with a bandwidth of 2 MHz. It is essentially a **meridian transit instrument.** The telescope consists of 1,000 broad band dipoles arranged in the form of the letter "**T**". The outputs of four dipoles along East West (EW) direction are combined in a Christmas tree fashion using open wire (balanced) transmission lines, and transformers to form a "**basic array element.**"

Such basic array elements, numbering two hundred and fifty are arranged to form a 1.38 km long EW array along the East West direction. Similarly ninety basic array elements are arranged to form a 0.45 km long south array along the south direction from the center of the EW array. The signals from the basic array units are brought to the laboratory through open wire transmission lines. East West array has an effective collecting area of approximately 12,000 m^2, while that of the North South array is approximately 7,000 m^2.

The receiver permits observation of a 15^o patch of sky (in the N-S direction) with 46 beams. The resolution is 26 X 40 sec ZA (ZA is the zenith angle). The sensitivity is around 20 Jansky.

APPENDIX B

CARBON RADIO RECOMBINATION LINES [CRRLs]

These lines involve highly excited states, presumably of carbon , during the transient recombination of a carbon ion with an electron. These lines(representing the highest excited states yet detected in interstellar gas) should be valuable indicators of conditions in the interstellar medium. Assuming carbon as the element involved, the presumed scenario is that a singly ionized carbon ion (C^+) recombines briefly with an electron. The resulting neutral , but highly excited states accompanied by emission or absorption. The higher the excitation, the more numerous and closely spaced the lines become so that the energies of transition ($\eta\varpi$) and the resulting frequencies(ν)are less with many falling below 100 MHz.

The twelve CRRLs are listed below;

Sl. no.	Orbital Quantum Number ' n '	Frequency in MHz
1	570	**35.43389892**
2	571	35.24821929
3	572	35.06383472
4	573	34.88073395
5	574	34.69890580
6	575	34.51458867
7	576	34.33476567
8	577	34.16094739
9	578	33.98410055
10	579	33.63405521
11	580	33.63405215
12	581	34.47971491

The above frequencies were calculated using the below formula;

$$F = 3.2896919 \times 10^9 [1/n^2 - 1/(n+1)^2] \quad MHz$$

where 'n' is the orbital quantum number.

APPENDIX C

MAX + PLUS AND EPLD

MAX+PLUS - the MAX programmable logic user system from Altera Corporation is a "fully integrated package for developing and implementing custom logic circuits with Altera's Multiple Array Matrix (MAX) family of high density Erasable Programmable Logic Devices (EPLDs)". The MAX+PLUS software offers different ways to enter the circuit design, compiles and fits the design to use MAX architecture in the most efficient way possible, and generates a file for programming the EPLD. One can also simulate the logic and timing characteristics of the design. The MAX + PLUS hardware consists of a software controlled Logic Programming Unit used for device programming.

Programmable logic devices (known by various names such as PAL, PLA, PLD, EPLD etc.) combine the logistical advantages of standard, fixed integrated circuits with the architectural flexibility of custom devices. They allow to electrically program standard, off the shelf logic elements to meet the specific needs of their applications. This eliminates various problems due to use of individual ICs in a circuit and reduces the overall cost and the time for the design.

The fundamental building block of an EPLD is the "macrocell". Each macrocell consists of three parts.

(1) The logic array that implements all combinatorial logic functions.

(2) The programmable register that provides D, T, JK or SR flip-flops.

(3) Programmable I/O that allows each I/O pin to be configured as input, output, or bi-directional operation.

The logic array consists of a programmable AND/fixed-OR PLA array. Inputs to the AND array come from the true and complement of the dedicated input and clock pins, and from the macrocell and I/O feedback paths. The connections between them are opened during the programming process.

Programmable flip-flop are used to create a variety of logic functions that use a minimum of EPLD resources. If the flip flop is not required for macrocell logic, it may simply be bypassed. In general purpose EPLDs each flip flop may be clocked from a dedicated system clock, any input or I/O pin or any internal logic function. EPLD registers are positive edge triggered with data transitions that occur on the positive edge of the clock. In addition, gated clock and clock enable logic can be implemented but their delay time is larger.

The EPLD I/O control block contains a tri-state buffer controlled by a ,macrocell product term and drives the I/O pin. I/O pins may be configured as dedicated outputs, bi-directional outputs, or as additional dedicated inputs.

The EPLDs have been built using the " CMOS EPROM " technology. The density of the chips range from hundreds to thousands of gates, offered in variety of packages with 20 to 100 pins.

EPLD families are divided into two architectural categories. The first one is the general purpose group which provide maximum flexibility for general purpose logic replacement. The EP series and EPM5000 series come under this group. The second group are the function

specific EPLDs specialized for performing specific system design tasks. The EPB and EPS series constitutes this group.

EPLDs are offered in a variety of packages including the dual in-line package (DIP), J-lead chip carrier (JLCC) , Quad Flat Pack (QFP) , Pin Grip Array (PGA) etc. EPLDs which are re-programmable are provided with windows are made of ceramic whereas , for high volume production one-time programmable plastic versions are available.

As already explained, the MAX+PLUS software is used for programming the chips.

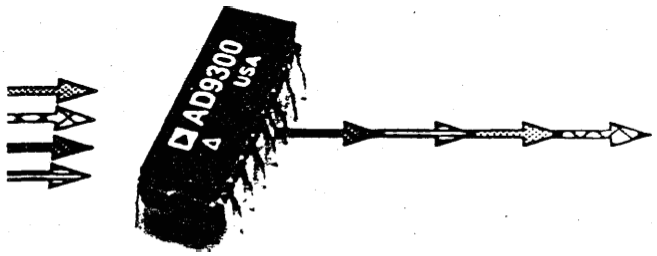
APPENDIX D

4 × 1 Wideband Video Multiplexer

AD9300

FEATURES
- 34MHz Full Power Bandwidth
- ±0.1dB Gain Flatness to 8MHz
- 75dB Crosstalk Rejection @ 10MHz
- 0.05°/0.05% Differential Phase/Gain
- Cascadable for Switch Matrices

APPLICATIONS
- Video Routing
- Medical Imaging
- Electro-Optics
- ECM Systems
- Radar Systems
- Data Acquisition



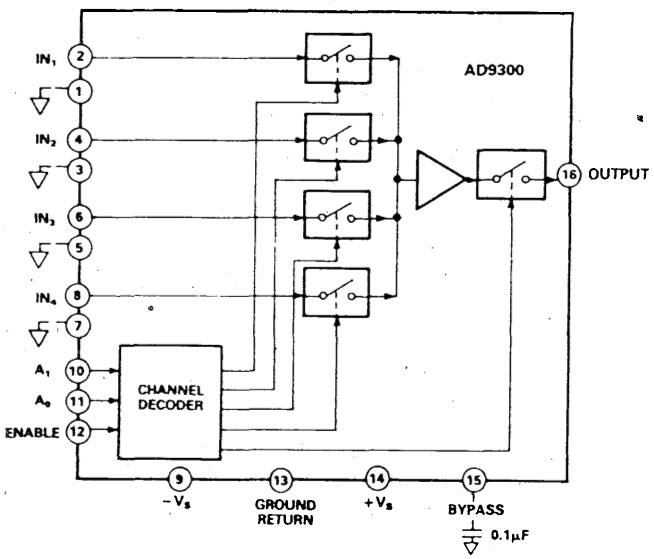
GENERAL DESCRIPTION

The AD9300 is a monolithic high-speed video signal multiplexer useable in a wide variety of applications.

Its four channels of video input signals can be randomly switched at megahertz rates to the single output. In addition, multiple devices can be configured in either parallel or cascade arrangements to form switch matrices. This flexibility in using the AD9300 is possible because the output of the device is in a high-impedance state when the chip is not enabled; when the chip is enabled, the unit acts as a buffer with a high input impedance and low output impedance.

An advanced bipolar process provides fast, wideband switching capabilities while maintaining crosstalk rejection of 75dB at 10MHz. Full power bandwidth is a minimum 30MHz. The device can be operated from ±10V to ±15V power supplies.

The AD9300KQ is packaged in a 16-pin ceramic DIP and is designed to operate over the commercial temperature range of 0°C to +70°C. For military temperatures of −55°C to +125°C, order part number AD9300TQ, which is also a 16-pin ceramic DIP. In addition to DIP packages, the AD9300 is also available in a 20-pin LCC as the model AD9300TE, which operates over a temperature range of −55°C to +125°C.



AD9300 Functional Block Diagram (Based on Cerdip)

ORDERING INFORMATION

Device	Temperature Range	Description	
AD9300KQ	0 to +70°C	16-Pin Cerdip, Commercial	
AD9300TQ	−55°C to +125°C	16-Pin Cerdip, Military Temperature	
AD9300TE	−55°C to +125°C	20-Pin LCC, Military Temperature	

One Technology Way; P. O. Box 9106; Norwood, MA 02062-9106 U.S.A.
Tel: 617/329-4700 Twx: 710/394-6577
Telex: 924491 Cables: ANALOG NORWOODMASS

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltages ($\pm V_S$) . . . . . $\pm 16V$
Analog Input Voltage Each Input (IN_1 thru IN_4) . . . . . $\pm 3.5V$
Differential Voltage Between Any Two Inputs (IN_1 thru IN_4) 5V
Digital Input Voltages (A_0, A_1, ENABLE) . . $-0.5V$ to $+5.5V$
Output Current
  Sinking 6.0mA
  Sourcing 6.0mA
Operating Temperature Range
  AD9300KQ . . . . . 0°C to +70°C
  AD9300TQ/TE . . . . . −55°C to +125°C
Storage Temperature Range . . . . . −65°C to +150°C
Junction Temperature . . . . . +175°C
Lead Soldering (10sec) . . . . . +300°C

ELECTRICAL CHARACTERISTICS ($\pm V_S = \pm 12V \pm 5\%$; $C_L = 10pF$; $R_L = 2k\Omega$, unless otherwise noted)

Parameter (Conditions)	Temp	Test Level	COMMERCIAL 0 to +70°C AD9300KQ Min	Typ	Max	Military Subgroup[2]	MILITARY −55°C to +125°C AD9300TQ/TE Min	Typ	Max	Units
INPUT CHARACTERISTICS										
Input Offset Voltage	+25°C	I		3	10	1		3	10	mV
Input Offset Voltage	Full	VI			14	2, 3			18	mV
Input Offset Voltage Drift[3]	Full	V		75				83		µV/°C
Input Bias Current	+25°C	I		15	37	1		15	37	µA
Input Bias Current	Full	VI			55	2,3			55	µA
Input Resistance	+25°C	V		3.0				3.0		MΩ
Input Capacitance	+25°C	V		2				2		pF
Input Noise Voltage (dc to 8MHz)	+25°C	V		16				16		µV rms
TRANSFER CHARACTERISTICS										
Voltage Gain[4]	+25°C	I	0.990	0.994		1	0.990	0.994		V/V
Voltage Gain[4]	Full	VI	0.985			2,3	0.985			V/V
DC Linearity[5]	+25°C	V		0.01				0.01		%
Gain Tolerance (V_{IN} = ±1V)										
dc to 5MHz	+25°C	I		0.05	0.1	4		0.05	0.1	dB
5MHz to 8MHz	+25°C	I		0.1	0.3	4		0.1	0.3	dB
Small-Signal Bandwidth (V_{IN} = 100mV p-p)	+25°C	V		350				350		MHz
Full Power Bandwidth[6] (V_{IN} = 2V p-p)	+25°C	I	30	34		4	30	34		MHz
Output Swing	Full	VI	±2			1, 2, 3	±2			V
Output Current (Sinking @ 25°C)	+25°C	V		5				5		mA
Output Resistance	+25°C	III		9	15	12		9	15	Ω
DYNAMIC CHARACTERISTICS										
Slew Rate[7]	+25°C	I	190	215		4	190	215		V/µs
Settling Time (to 0.1% on ±2V Output)	+25°C	III		70	100	12		70	100	ns
Overshoot										
To T-Step[8]	+25°C	V		<0.1				<0.1		%
To Pulse[9]	+25°C	V		<10				<10		%
Differential Phase[10]	+25°C	III		0.05	0.1	12		0.05	0.1	
Differential Gain[10]	+25°C	III		0.05	0.1	12		0.05	0.1	%
Crosstalk Rejection										
Three Channels[11]	+25°C	I	70	75		4	70	75		dB
One Channel[12]	+25°C	I	80	83		4	80	83		dB
SWITCHING CHARACTERISTICS[13]										
A_X Input to Channel HIGH Time[14] (t_{HIGH})	+25°C	I		40	50	9		40	50	ns
A_X Input to Channel LOW Time[15] (t_{LOW})	+25°C	I		35	45	9		35	45	ns
Enable to Channel ON Time[16] (t_{ON})	+25°C	I		30	40	9		30	40	ns
Enable to Channel OFF Time[17] (t_{OFF})	+25°C	I		20	30	9		20	30	ns
Switching Transient[18]	+25°C	V		60				60		mV

Parameter (Conditions)	Temp	Test Level	COMMERCIAL 0 to +70°C AD9300KQ Min	Typ	Max	Military Subgroup[2]	MILITARY −55°C to +125°C AD9300TQ/TE Min	Typ	Max	Units
DIGITAL INPUTS										
Logic "1" Voltage	Full	VI	2			1,2,3	2			V
Logic "0" Voltage	Full	VI			0.8	1,2,3			0.8	V
Logic "1" Current	Full	VI			5	1,2,3			5	μA
Logic "0" Current	Full	VI			1	1,2,3			1	μA
POWER SUPPLY										
Positive Supply Current (+12V)	+25°C	I		13	16	1		13	16	mA
Positive Supply Current (+12V)	Full	VI		13	16	2,3		13	16	mA
Negative Supply Current (−12V)	+25°C	I		12.5	15	1		12.5	15	mA
Negative Supply Current (−12V)	Full	VI		12.5	16	2,3		12.5	16	mA
Power Supply Rejection Ratio ($\pm V_S = \pm 12V \pm 5\%$)	Full	VI	67	75		1,2,3	67	75		dB
Power Dissipation (±12V)[19]	+25°C	V		306				306		mW

NOTES

[1]Permanent damage may occur if any one absolute maximum rating is exceeded. Functional operation is not implied, and device reliability may be impaired by exposure to higher-than-recommended voltages for extended periods of time.
[2]Military Subgroups apply to military-qualified devices only.
[3]Measured at extremes of temperature range.
[4]Measured as slope of V_{OUT} versus V_{IN} with $V_{IN} = \pm 1V$.
[5]Measured as worst deviation from end-point fit with $V_{IN} = \pm 1V$.
[6]Full Power Bandwidth (FPBW) based on Slew Rate (SR). $FPBW = SR/2\pi V_{PEAK}$
[7]Measured between 20% and 80% transition points of ±1V output.
[8]T-Step = Sin^2X Step, when Step between 0V and +700mV points has 10%-to-90% risetime = 125ns.
[9]Measured with a pulse input having slew rate >250V/μs.
[10]Measured at output between 0.28Vdc and 1.0Vdc with V_{IN} = 284mV p-p at 3.58MHz and 4.43MHz.
[11]This specification is critically dependent on circuit layout. Value shown is measured with selected channel grounded and 10MHz 2V p-p signal applied to remaining three channels. If selected channel is grounded through 75Ω, value is approximately 6dB higher.
[12]This specification is critically dependent on circuit layout. Value shown is measured with selected channel grounded and 10MHz 2V p-p signal applied to one other channel. If selected channel is grounded through 75Ω, value is approximately 6dB higher.
[13]Consult system timing diagram.
[14]Measured from address change to 90% point of −2V to +2V output LOW-to-HIGH transition.
[15]Measured from address change to 10% point of +2V to −2V output HIGH-to-LOW transition.
[16]Measured from 50% transition point of ENABLE input to 90% transition of 0V to −2V output.
[17]Measured from 50% transition point of ENABLE input to 10% transition of +2V to 0V output.
[18]Measured while switching between two grounded channels.
[19]Maximum power dissipation is a package-dependent parameter related to the following typical thermal impedances:
16-Pin Ceramic θ_{JA} = 87°C/W; θ_{JC} = 25°C/W
20-Pin LCC θ_{JA} = 74°C/W; θ_{JC} = 10°C/W

Specifications subject to change without notice.

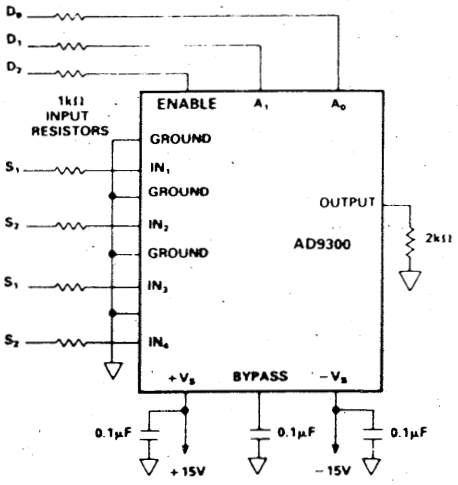
EXPLANATION OF TEST LEVELS

Test Level I	–	100% production tested.
Test Level II	–	100% production tested at +25°C, and sample tested at specified temperatures.
Test Level III	–	Sample tested only.
Test Level IV	–	Parameter is guaranteed by design and characterization testing.
Test Level V	–	Parameter is a typical value only.
Test Level VI	–	All devices are 100% production tested at +25°C. 100% production tested at temperature extremes for military temperature devices; sample tested at temperature extremes for commercial/industrial devices.

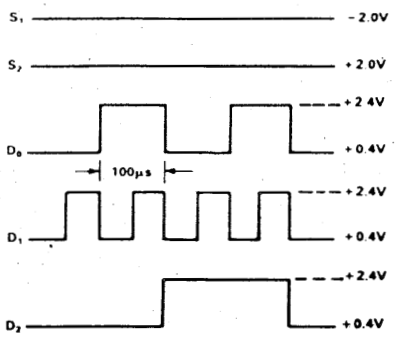
EXPLANATION OF GROUP A MILITARY SUBGROUPS

Subgroup 1	–	Static tests at +25°C. (5% PDA calculated against Subgroup 1 for high-rel versions)
Subgroup 2	–	Static tests at maximum rated temperature.
Subgroup 3	–	Static tests at minimum rated temperature.
Subgroup 4	–	Dynamic tests at +25°C.
Subgroup 5	–	Dynamic tests at maximum rated temperature.
Subgroup 6	–	Dynamic tests at minimum rated temperature.
Subgroup 7	–	Functional tests at +25°C.
Subgroup 8	–	Functional tests at maximum and minimum rated temperatures.
Subgroup 9	–	Switching tests at +25°C.
Subgroup 10	–	Switching tests at maximum rated temperature.
Subgroup 11	–	Switching tests at minimum rated temperature.
Subgroup 12	–	Periodically sample tested.

AD9300 BURN-IN DIAGRAM



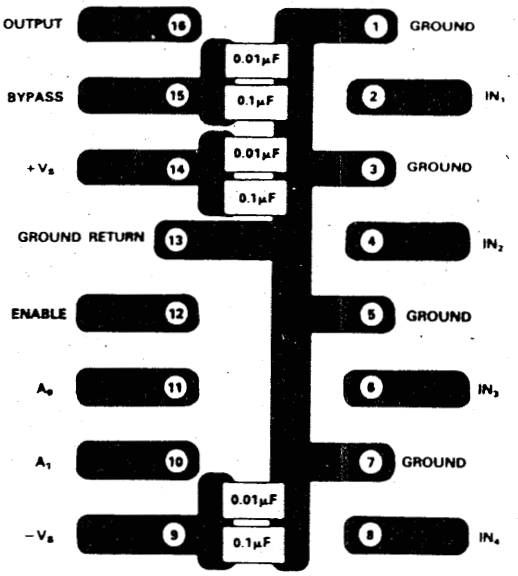
ALL RESISTORS ±5%
ALL CAPACITORS ±20%
ALL SUPPLY VOLTAGES ±5%



OPTION #1 (STATIC) $S_1 = -2.0V$; $S_2 = +2.0V$
$D_0 = D_1 = +2.4V$; $D_2 = 0V$

OPTION #2 (DYNAMIC) SEE WAVEFORMS

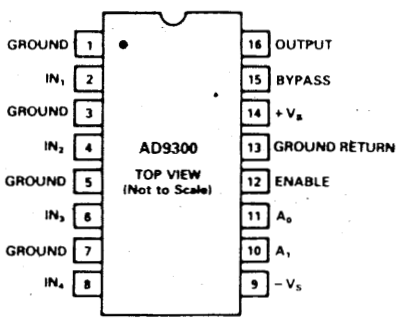
SUGGESTED LAYOUT OF AD9300 PC BOARD



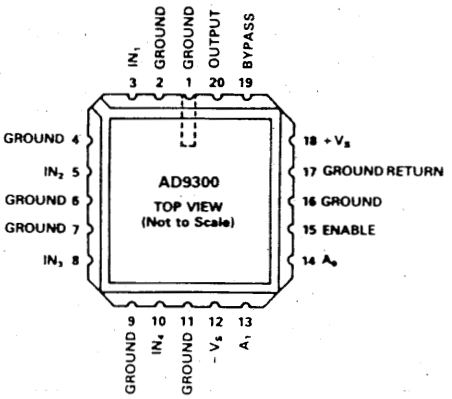
(Bottom View – Not to Scale)
Component Side Should be Ground Plane

PIN DESIGNATIONS

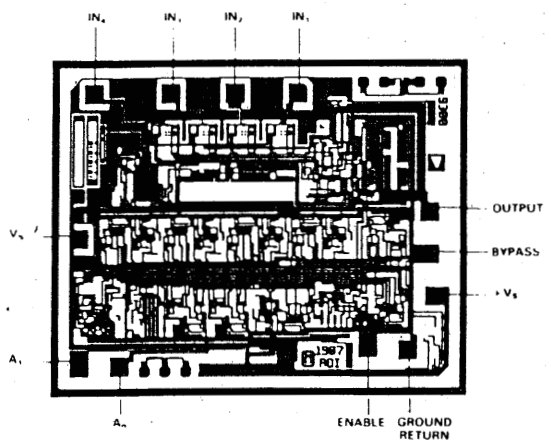
DIP



LCC



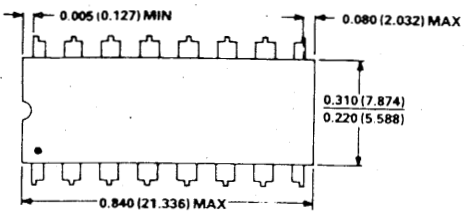
METALIZATION PHOTOGRAPH

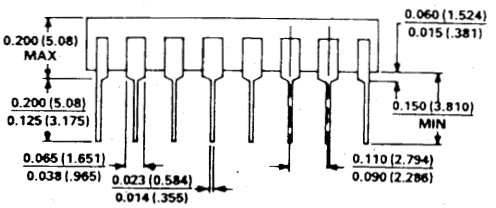


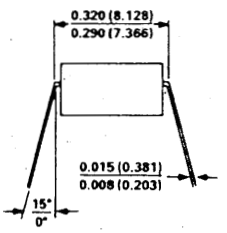
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

16-Pin Cerdip (Q) Package





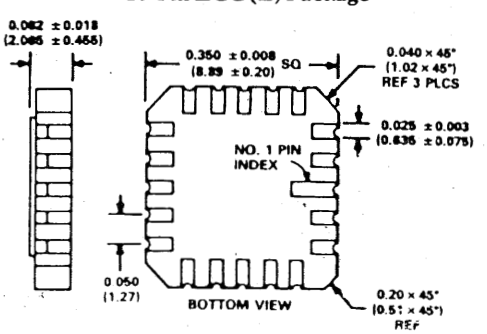


NOTES:
LEAD NO. 1 IDENTIFIED BY DOT OR NOTCH.
LEADS ARE SOLDER-DIPPED OR TIN-PLATED KOVAR OR ALLOY 42.

MECHANICAL INFORMATION

Die Dimensions	84 × 104 × 18 (max) mils
Pad Dimensions	4 × 4 (min) mils
Metalization	Aluminum
Backing	None
Substrate Potential	$-V_S$
Passivation	Oxynitride
Die Attach	Gold Eutectic
Bond Wire	1.25 mil, Aluminum; Ultrasonic Bonding or 1 mil, Gold; Gold Ball Bonding

20-Pin LCC (E) Package

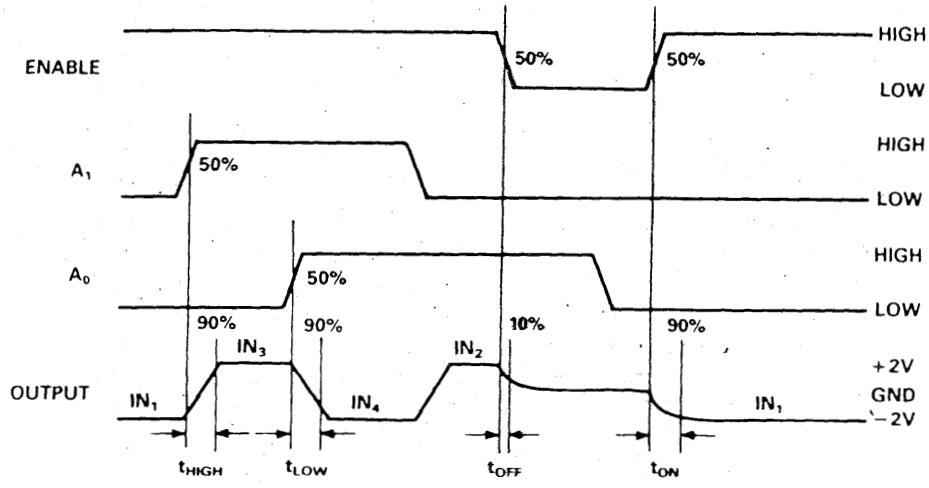


FUNCTIONAL DESCRIPTION

$IN_1 - IN_4$	Four analog input channels.
GROUND	Analog input shielding grounds, not internally connected. Connect each to external low-impedance ground as close to device as possible.
A_0	One of two TTL decode control lines required for channel selection. See Logic Truth Table.
A_1	One of two TTL decode control lines required for channel selection. See Logic Truth Table.
ENABLE	TTL-compatible chip enable. In enabled mode (logic HIGH), output signal tracks selected input channel; in disabled mode (logic LOW), output is high impedance and no signal appears at output.
$-V_S$	Negative supply voltage; nominally -10V dc to -15V dc.
$+V_S$	Positive supply voltage; nominally $+10$V dc to $+15$V dc.
OUTPUT	Analog output. Tracks selected input channel when enabled.
BYPASS	Bypass terminal for internal bias line; must be decoupled externally to ground through 0.1μF capacitor.
GROUND RETURN	Analog signal and power supply ground return.

LOGIC TRUTH TABLE

ENABLE	A_1	A_0	OUTPUT
0	X	X	High Z
1	0	0	IN_1
1	0	1	IN_2
1	1	0	IN_3
1	1	1	IN_4



AD9300 Timing

THEORY OF OPERATION

Refer to the functional block diagram of the AD9300.

As shown on the drawing, this diagram is based on the pinouts of the DIP packaging of the models AD9300KQ and AD9300TQ. The AD9300TE is packaged in a 20-pin leadless chip carrier (LCC), but the extra pins are used for ground connections; the theory of operation remains the same.

The AD9300 Video Multiplexer allows the user to connect any one of four analog input channels ($IN_1 - IN_4$) to the output of the device, and to switch between channels at megahertz rates.

The input channel which is connected to the output is determined by a 2-bit TTL digital code applied to A_0 and A_1. The selected input will not appear at the output unless a digital "1" is also applied to the ENABLE input pin; unless the output is enabled, it is a high impedance. Necessary combinations to accomplish channel selection are shown in the Logic Truth Table.

Bipolar construction used in the AD9300 insures that the input impedance of the device remains high, and will not vary with power supply voltages. This characteristic makes the AD9300, in effect, a switchable-input buffer. An on-board bias network makes the performance of the AD9300 independent of applied supply voltages, which can have any nominal value from ± 10V dc to ± 15V dc.

Although the primary application for the AD9300 is the routing of video signals, the harmonic and dynamic attributes of the device make it appropriate for other applications. The AD9300 has exceptional performance when switching video signals, but can also be used for switching other analog signals requiring greater dynamic range and/or precision than those in video.

As shown in Figure 1, Input and Output Equivalent Circuits, each analog input is connected to the base of a bipolar transistor. If Channel 1 is selected, a current switch is closed and routes current through the input transistor for Channel 1.

If Channel 2 is then selected by the digital inputs, the current switch for Channel 1 is opened and the current switch for Channel 2 is closed. This causes current to be routed away from the Channel 1 transistor and into the Channel 2 input transistor. Whenever a channel's input device is carrying current, the analog input applied to that channel is passed to the output stage.

The operation of the output stage is similar to that of the input stages. Whenever the output stage is enabled with a HIGH digital "1" signal at the ENABLE pin, the output transistor will carry current and pass the selected analog input.

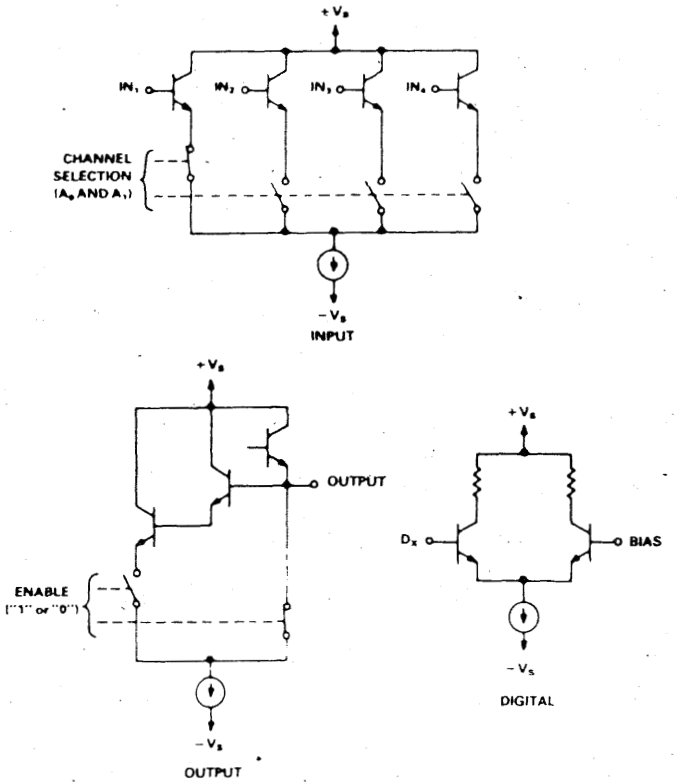


Figure 1. Input and Output Equivalent Circuits

When the output stage is disabled (by virtue of the ENABLE pin being driven LOW with a digital "0"), the output current switch is opened. This routes the current to other circuits within the AD9300 which keep the output transistor biased "off". These circuits require approximately 1μA of bias current from the load connected to the output of the multiplexer. In the absence of a terminating load and the resulting dc bias, the output of the AD9300 "floats" at −2.5V.

In summary, when the AD9300 is enabled by the ENABLE pin being driven HIGH with a digital "1", the selected analog input channel acts as a buffer for the input; and the output of the multiplexer is a low impedance. When the AD9300 is disabled with a digital "0" LOW signal, the selected channel acts as an open switch for the input; and the output of the unit becomes a high impedance. This characteristic allows the user to wire-or several AD9300 Analog Multiplexers together to form switch matrices.

AD9300 APPLICATIONS

To ensure optimum performance from circuits using the AD9300, it is important to follow a few basic rules which apply to all high-speed devices.

A large, low-impedance ground plane under the AD9300 is critical. Generally, GROUND and GROUND RETURN connections should be connected solidly to this plane. GROUND pin connections are signal isolation grounds which are not connected internally; they can be left unconnected, but there may be some degradation in crosstalk rejection. GROUND RETURN, on the other hand, serves as the internal ground reference for the AD9300 and should be connected to the ground plane *without exception*.

It is recommended that the AD9300 be soldered directly into circuit boards, rather than using socket assemblies. If sockets must be used, individual pin sockets are the preferred choice, rather than a socket assembly. A second requirement for proper high-speed design involves decoupling the power supply and internal bias supply lines from ground to improve noise immunity. Chip capacitors are recommended for connecting 0.1μF and 0.01μF capacitors between ground and the $\pm V_S$ supplies (Pins 9 and 14), and the BYPASS connection (Pin 15).

The output stage of the unit is capable of driving a 2kΩ,10pF load. Larger capacative loads may limit full power bandwidth and increase t_{OFF} (the interval between the 50% point of the ENABLE high-to-low transition and the instant the output becomes a high impedance.)

For applications such as driving cables (See Figure 2), output buffers are recommended.

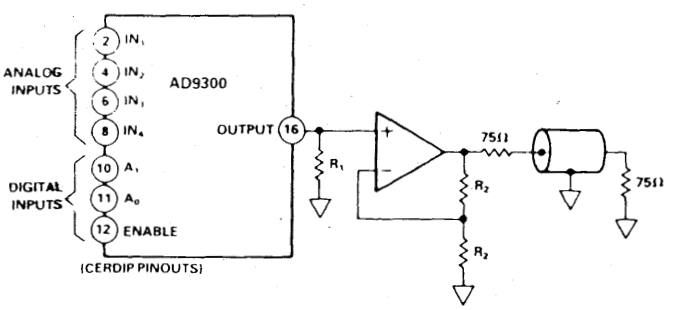


Figure 2. 4×1 AD9300 Multiplexer with Buffered Output Driving 75Ω Coaxial Cable

ANALOG DEVICES

Ultrahigh Speed Monolithic Track-and-Hold

AD9100

FEATURES

Excellent Hold Mode Distortion
- **−88 dB @ 30 MSPS (2.3 MHz V_{IN})**
- **−83 dB @ 30 MSPS (12.1 MHz V_{IN})**
- **−74 dB @ 30 MSPS (19.7 MHz V_{IN})**

16 ns Acquisition Time to 0.01%
<1 ps Aperture Jitter
250 MHz Tracking Bandwidth
83 dB Feedthrough Rejection @ 20 MHz
3.3 nV/$\sqrt{Hz}$ Spectral Noise Density

APPLICATIONS

A/D Conversion
Direct IF Sampling
Imaging/FLIR Systems
Peak Detectors
Radar/EW/ECM
Spectrum Analysis
CCD ATE

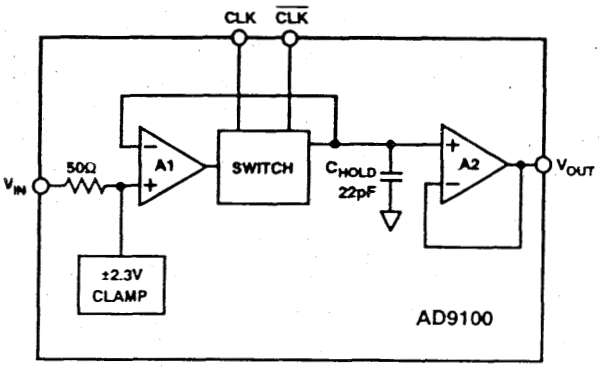
GENERAL DESCRIPTION

The AD9100 is a monolithic track-and-hold amplifier which sets a new standard for high speed and high dynamic range applications. It is fabricated in a mature high speed complementary bipolar process. In addition to innovative design topologies, a custom package is utilized to minimize parasitics and optimize dynamic performance.

Acquisition time (hold to track) is 13 ns to 0.1% accuracy, and 16 ns to 0.01%. The AD9100 boasts superlative hold-mode frequency domain performance; when sampling at 30 MSPS hold mode distortion is less than −83 dBfs for analog frequencies up to 12 MHz; and −74 dBfs at 20 MHz. The AD9100 can also drive capacitive loads up to 100 pF with little degradation in acquisition time; it is therefore well suited to drive 8- and 10-bit flash converters at clock speeds to 50 MSPS. With a spectral noise density of 3.3 nV/$\sqrt{Hz}$ and feedthrough rejection of 83 dB at 20 MHz, the AD9100 is well suited to enhance the dynamic range of many 8- to 16-bit systems.

*Patent pending.

AD9100 BLOCK DIAGRAM



The AD9100 is "user friendly" and easy to apply: (1) it requires +5 V/−5.2 V power supplies; (2) the hold capacitor and switch power supply decoupling capacitors are built into the DIP package; (3) the encode clock is differential ECL to minimize clock jitter; (4) the input resistance is typically 800 kΩ; (5) the analog input is internally clamped to prevent damage from voltage transients.

The AD9100 is available in a 20-lead side-brazed "skinny DIP" package. Commercial, industrial, and military temperature grade parts are available. Consult the factory for information about the availability of surface mount packages and 883-qualified devices.

PRODUCT HIGHLIGHTS

1. Hold Mode Distortion is guaranteed.
2. Monolithic construction.
3. Analog input is internally clamped to protect against overvoltage transients and ensure fast recovery.
4. Output is short circuit protected.
5. Drives capacitive loads to 100 pF.
6. Differential ECL clock inputs.

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
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AD9100—SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltages ($\pm V_S$) . . . . . ±6 V
Continuous Output Current . . . . . 70 mA
Analog Input Voltage[2] . . . . . ±5 V
Junction Temperature . . . . . +175°C
Storage Temperature . . . . . −65°C to +150°C
Lead Soldering Temperature (10 sec) . . . . . +300°C

ELECTRICAL CHARACTERISTICS (unless otherwise noted, $+V_S = +5$ V; $-V_S = -5.2$ V; $R_{LOAD} = 100\ \Omega$; $R_{IN} = 50\ \Omega$)

Parameter	Conditions	Temp	Test Level	Mil Sub	AD9100JD/AD/SD[3] Min	Typ	Max	Units
DC ACCURACY								
Gain	$\Delta V_{IN} = 2$ V	Full	VI	1, 2, 3	0.989	0.994		V/V
Offset	$V_{IN} = 0$ V	Full	VI	1, 2, 3	−5	±1	+5	mV
Output Resistance		25°C	V			0.4		Ω
Output Drive Capability		Full	VI	1, 2, 3	±40	±60		mA
PSRR	$\Delta V_S = 0.5$ V p–p	Full	VI	7, 8	48	55		dB
Pedestal Sensitivity to Supply	$\Delta V_S = 0.5$ V p–p	Full	VI	7, 8		0.9	2	mV/V
ANALOG INPUT/OUTPUT								
Output Voltage Range		Full	VI	1, 2, 3	+2	±2.2	−2	V
Input Bias Current		25°C	VI	1	−8	±3	+8	μA
		Full	VI	2, 3	−16		+16	μA
Input Overdrive Current[4]	$V_{IN} = \pm 4$ V	25°C	V			±22		mA
Input Capacitance		25°C	V			1.2		pF
Input Resistance		25°C, T_{max}	VI	1, 2	350	800		kΩ
		T_{min}	VI	3	200			kΩ
CLOCK/$\overline{\text{CLOCK}}$ INPUTS								
Input Bias Current	CL/$\overline{\text{CL}}$ = −1.0 V	Full	VI	1, 2, 3		4	5	mA
Input Low Voltage (V_{IL})		Full	VI	1, 2, 3	−1.8		−1.5	V
Input High Voltage (V_{IH})		Full	VI	1, 2, 3	−1.0		−0.8	V
TRACK MODE DYNAMICS								
Bandwidth (−3 dB)	$V_{OUT} \leq 0.4$ V p–p	Full	IV	4, 5, 6	160	250		MHz
Slew Rate	4-Volt Step	Full	IV	4, 5, 6	550	850		V/μs
Overdrive Recovery Time[4] (to 0.1%)	$V_{IN} = \pm 4$ V to 0 V	25°C	V			21		ns
2nd Harm. Dist. (20 MHz, 2 V p–p)		Full	V			−65		dBc
3rd Harm. Dist. (20 MHz, 2 V p–p)		Full	V			−75		dBc
Integrated Output Noise (1–200 MHz)		25°C	V			45		μV
RMS Spectral Noise @ 10 MHz		25°C	V			3.3		nV/$\sqrt{\text{Hz}}$
HOLD MODE DYNAMICS								
Worst Harmonic (2.3 MHz, 30 MSPS)	$V_{OUT} = 2$ V p–p	25°C	V			−83		dBfs
Worst Harmonic (12.1 MHz, 30 MSPS)	$V_{OUT} = 2$ V p–p	25°C, T_{max}	IV	4, 5		−81	−72	dBfs
Worst Harmonic (12.1 MHz, 30 MSPS)	$V_{OUT} = 2$ V p–p	T_{min}	IV	6		−77	−70	dBfs
Worst Harmonic (19.7 MHz, 30 MSPS)	$V_{OUT} = 2$ V p–p	25°C	V			−74		dBfs
Hold Noise[5]		25°C	V			300 × t_H		V/s rms
Droop Rate[6]	$V_{IN} = 0$ V	25°C	VI	4		1	6	±mV/μs
		T_{min}	VI	6		7	40	±mV/μs
		T_{max}	VI	5		5	30	±mV/μs
Feedthrough Rejection (20 MHz)	$V_{IN} = 2$ V p–p	Full	V			83		dB
TRACK-TO-HOLD SWITCHING								
Aperture Delay		25°C	V			+800		ps
Aperture Jitter		25°C	V			<1		ps
Pedestal Offset	$V_{IN} = 0$ V	25°C	VI	4	−5	±1	+5	mV
		Full	VI	5, 6	−10		+10	mV
Transient Amplitude	$V_{IN} = 0$ V	Full	V			±6		mV
Settling Time to 1 mV		Full	VI	7, 8		7	11	ns
Glitch Product	V_{IN} 0 V	25°C	V			15		pV-s
HOLD-TO-TRACK SWITCHING								
Acquisition Time to 0.1%	2 V Step	25°C	V			13		ns
Acquisition Time to 0.01%	2 V Step	Full	IV	7, 8		16	23	ns
Acquisition Time to 0.01%	4 V Step	25°C	V			20		ns

Parameter	Conditions	Temp	Test Level	Mil Sub	AD9100JD/AD/SD[3] Min	Typ	Max	Units
POWER SUPPLY								
Power Dissipation		Full	VI	1, 2, 3		1.05	1.25	W
$+V_S$ Current		Full	VI	1, 2, 3		96	118	mA
$-V_S$ Current		Full	VI	1, 2, 3		116	132	mA

NOTES

[1]Absolute maximum ratings are limiting values to be applied individually, and beyond which the serviceability of the circuit may be impaired. Functional operability is not necessarily implied. Exposure to absolute maximum rating conditions for an extended period of time may affect device reliability.

[2]Analog input voltage should not exceed $+V_S$.

[3]The "Full" temperature specifications refer to the ambient temperature for the DIP package only after a power soak. AD9100JD: 0°C to +70°C. AD9100AD: −40°C to +85°C. AD9100SD: −55°C to +125°C. θ_{JA} = 38°C/W; this is valid with the device mounted flush to a grounded 2-oz copper clad board with 16 sq. inches of surface area and no air flow.

[4]The input to the AD9100 is internally clamped at ±2.3 V. The internal input series resistance is nominally 50 Ω.

[5]Hold mode noise is proportional to the length of time a signal is held. For example, if the hold time (t_H) is 20 ns, the accumulated noise is typically 6 μV (300 V/s × 20 ns). This value must be combined with the track mode noise to obtain total noise.

[6]Min and max droop rates are based on the military temperature range (−55°C to +125°C). Refer to the "Droop Rate vs Temperature" chart for min/max limits over the commercial and industrial ranges.

Specifications subject to change without notice.

EXPLANATION OF TEST LEVELS

Test Level

I — 100% production tested.

II — 100% production tested at +25°C, and sample tested at specified temperatures.

III — Periodically sample tested.

IV — Parameter is guaranteed by design and characterization testing.

V — Parameter is a typical value only.

VI — All devices are 100% production tested at +25°C. 100% production tested at temperature extremes for extended temperature devices; sample tested at temperature extremes for commercial/industrial devices.

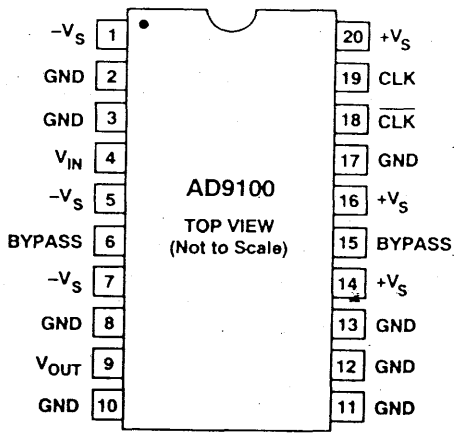
EXPLANATION OF MILITARY SUBGROUPS

Subgroup 1 – Static tests at +25°C.
(5% PDA calculated against Subgroup 1 for high-rel versions)
Subgroup 2 – Static tests at maximum rated operating temperature.
Subgroup 3 – Static tests at minimum rated operating temperature.
Subgroup 4 – Dynamic tests at +25°C.
Subgroup 5 – Dynamic tests at maximum rated operating temperature.
Subgroup 6 – Dynamic tests at minimum rated operating temperature.
Subgroup 7 – Functional tests at +25°C.
Subgroup 8 – Functional tests at maximum and minimum temperatures.
Subgroup 9 – Switching tests at +25°C.
Subgroup 10 – Switching tests at maximum rated operating temperature.
Subgroup 11 – Switching tests at minimum rated operating temperature.
Subgroup 12 – Periodically sample tested.

AD9100 PIN DESCRIPTIONS/CONNECTIONS

Pin No.	Description	Connection
1	$-V_S$	−5.2 V Power Supply
2	GND	Common Ground Plane
3	GND	Common Ground Plane
4	V_{IN}	Analog Input Signal
5	$-V_S$	−5.2 V Power Supply
6	BYPASS	0.1 μF to Ground
7	$-V_S$	−5.2 V Power Supply
8	GND	Common Ground Plane
9	V_{OUT}	Track and Hold Output
10	GND	Common Ground Plane
11	GND	Common Ground Plane
12	GND	Common Ground Plane
13	GND	Common Ground Plane
14	$+V_S$	+5 V Power Supply
15	BYPASS	0.1 μF to Ground
16	$+V_S$	+5 V Power Supply
17	GND	Common Ground Plane
18	$\overline{CLK}$	Complement ECL Clock
19	CLK	"True" ECL Clock
20	$+V_S$	+5 V Power Supply

AD9100 PINOUTS



Acquisition Time is the amount of time it takes the AD9100 to reacquire the analog input when switching from hold to track mode. The interval starts at the 50% clock transition point and ends when the input signal is reacquired to within a specified error band at the hold capacitor.

Analog Delay is the time required for an analog input signal to propagate from the device input to output.

Aperture Delay tells when the input signal is actually sampled. It is the time difference between the analog propagation delay of the front-end buffer and the control switch delay time. (The time from the hold command transition to when the switch is opened.) For the AD9100, this is a positive value which means that the switch delay is longer than the analog delay.

Aperture Jitter is the random variation in the aperture delay. This is measured in ps-rms and results in phase noise on the held signal.

Droop Rate is the change in output voltage as a function of time (dV/dt). It is measured at the AD9100 output with the device in hold mode and the input held at a specified dc value; the measurement starts immediately after the T/H switches from track to hold.

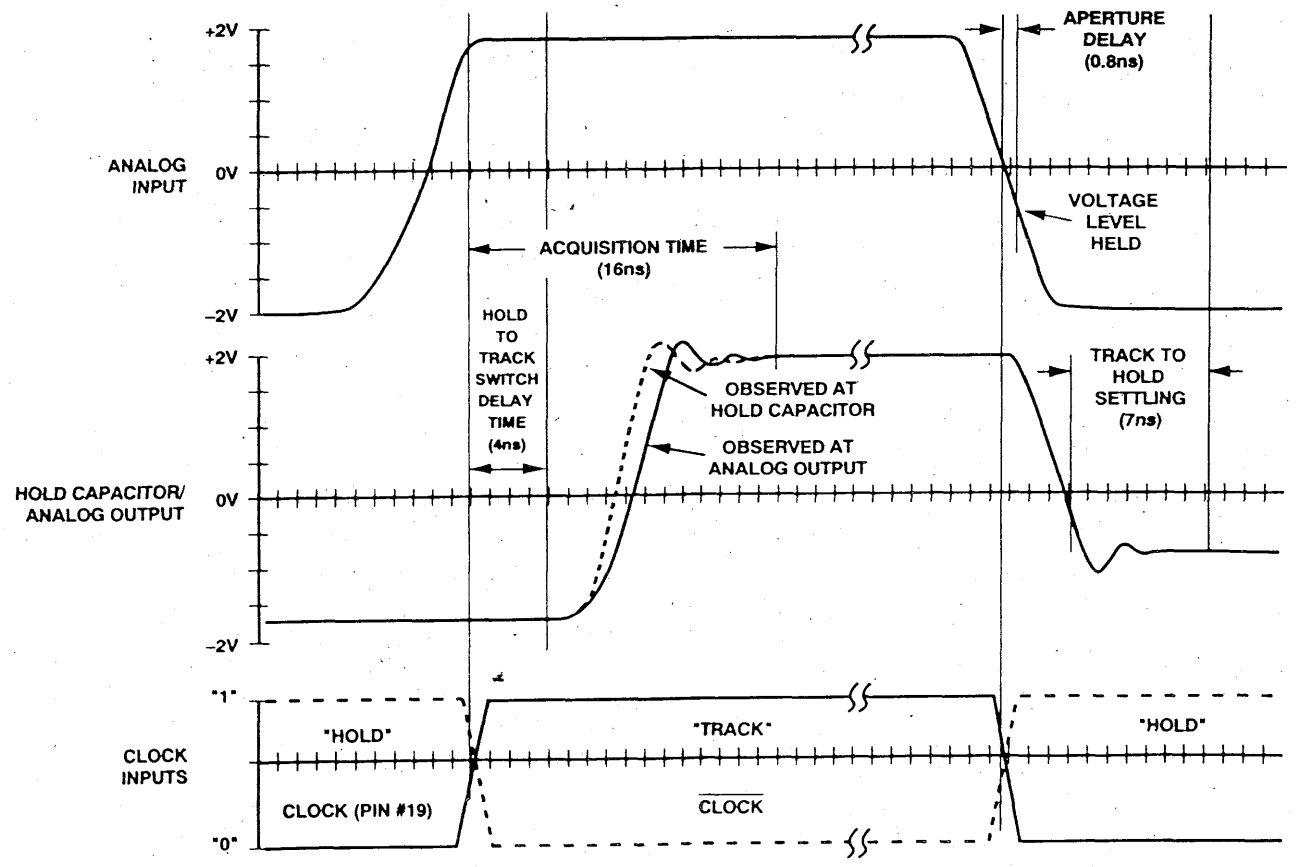
Feedthrough Rejection is the ratio of the input signal to the output signal when in hold mode. This is a measure of how well the switch isolates the input signal from feeding through to the output.

Hold to Track Switch Delay is the time delay from the track command to the point when the output starts to change and acquire a new signal.

Pedestal Offset is the offset voltage step measured immediately after the AD9100 is switched from track to hold with the input held at zero volts. It manifests itself as an added offset during the hold time.

Track to Hold Settling Time is the time necessary for the track to hold switching transient to settle to within 1 mV of its final value.

Track to Hold Switching Transient is the maximum peak switch induced transient voltage which appears at the AD9100 output when it is switched from track to hold.



AD9100 Timing Diagram

THEORY OF OPERATION

The AD9100 utilizes a new track and hold architecture. Previous commercially available high speed track and holds used a front end open loop input buffer, followed by a diode bridge, hold capacitor, and output buffer (closed or open loop) with a FET device connected to the hold capacitor. This architecture required mixed device technology and, usually, hybrid construction. The sampling rate of these hybrids has been limited to 20 MSPS for 12-bit accuracy. Distortion generated in the front-end amplifier/bridge limited the dynamic range performance to the "mid-70 dBfs" for analog input signals of less than 10 MHz. Broadband and switch-generated noise limited the SNR of previous track and holds to about 70 dB.

The AD9100 is a monolithic device using a high frequency complementary bipolar process to achieve new levels of high speed precision. Its patent pending architecture breaks from the traditional architecture described above. (See the block diagram on the first page.) The switching type bridge has been integrated into the first stage closed loop input amplifier. This innovation provides error (distortion) correction for both the switch and amplifier, while still achieving slew rates representative of an open-loop design. In addition, acquisition slew current for the hold capacitor is higher than standard diode bridge and switch configurations, removing a main contributor to the limits of maximum sampling rate and input frequency.

Switching circuits in the device use current steering (versus voltage switching) to provide improved isolation between the switch and analog sections. This results in low aperture time sensitivity to the analog input signal, and reduced power supply and analog switching noise. Track to hold peak switching transient is typically only 6 mV and settles to less than 1 mV in 7 ns. In addition, pedestal sensitivity to analog input voltage is very low (0.6 mV/V) and being first order linear does not significantly affect distortion.

The closed-loop output buffer includes zero voltage bias current cancellation, which results in high-temperature droop rates equivalent to those found in FET type inputs. The buffer also provides first order quasistatic bias correction resulting in an extremely high input resistance and very low droop sensitivity vs. input voltage level (typically less than 1.5 mV/V−μs.) This closed-loop architecture inherently provides high speed loop correction and results in low distortion under heavy loads.

The extremely fast time constant linearity (7 ns to 0.01% for a 2 V step) ensures that the output buffer does not limit the AD9100 sampling rate or analog input frequency. (The acquisition and settling time are primarily limited only by the input amplifier and switch.) The output is transparent to the overall AD9100 hold mode distortion levels for loads as low as 250 Ω.

Full-scale track and acquisition slew rates achieved by the AD9100 are 800 and 1000 V/μs, respectively. When combined with excellent phase margin (typically 5% overshoot), wide bandwidth, and dc gain accuracy, acquisition time to 0.01% is only 16 ns. Though not tested, settling to 14-bit accuracy (−88 dB distortion @ 2.3 MHz) can be inferred to be 20 ns

Acquisition Time

Acquisition time is the amount of time it takes the AD9100 to reacquire the analog input when switching from hold to track mode. The interval starts at the 50% clock transition point and ends when the input signal is reacquired to within a specified error band at the hold capacitor.

The hold to track switch delay ($t_{DH}t$) can not be subtracted from this acquisition time because it is a charging time delay that occurs when moving from hold to track; this is typically 4 to 6 ns and is the longest delay. Therefore, the track time required for the AD9100 is the acquisition time, which includes t_{DHT}. Note that the acquisition time is defined as the settled voltage at the hold capacitor and does not include the delay and settling time of the output buffer. The example below illustrates why the output buffer amplifier does not contribute to the overall AD9100 acquisition time.

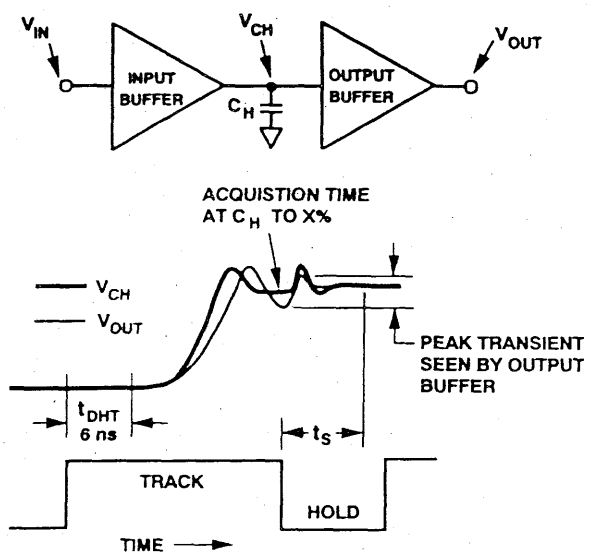


Figure 1. Acquisition Time Diagram

The exaggerated illustration in Figure 1 shows that V_{CH} has settled to within x% of its final value, but V_{OUT} (due to slew rate limitations, finite BW, power supply ringing, etc.) has not settled during the track time. However, since the output buffer always "tracks" the front end circuitry, it "catches up" during the hold time and directly superimposes itself (less about 600 ps of analog delay) to V_{CH}. Since the small-signal settling time of the output buffer is about 1.8 ns to ±1 mV and is significantly less than the specified hold time, acquisition time should be referenced to the hold capacitor.

Note that most of the hold settling time and output acquisition time are due to the input buffer and the switch network. For output acquisition time, the output buffer contributes only about 5 ns of the total; in hold mode, it contributes only 1.8 ns (as stated above).

A stricter definition of acquisition time would total the acquisition and hold times to a defined accuracy. To obtain 12 bit + distortion levels and 30 MSPS operation, the recommended track and hold times are 20 ns and 13.5 ns, respectively. To drive an 8-bit flash converter with a 2 V p–p full-scale input, hold time to 1 LSB accuracy will be limited primarily by the encoder, rather than by the AD9100. This makes it possible to reduce track time to approximately 13 ns, with hold time chosen to optimize the encoder's performance.

Hold vs. Track Mode Distortion

In many traditional high speed, open loop track-and-holds, track mode distortion is often much better than hold mode distortion. Track mode distortion does not include nonlinearities due to the switch network, and does not correlate to the relevant hold mode distortion. But since hold mode distortion has traditionally been omitted from manufacturer's specification tables, users have had to discover for themselves the effective overall hold mode distortion of the combined T/H and encoder.

The architecture of the AD9100 minimizes hold mode distortion over its specified frequency range. As an example, in track mode the worst harmonic generated for a 20 MHz input tone is typically −65 dBfs. In hold mode, under the same conditions and sampling at 30 MSPS, the worst harmonic generated is −74 dBfs. The reason is the output buffer in hold mode has only dc distortion relevancy. With its inherent linearity (7 ns settling to 0.01%), the output buffer has essentially settled to its dc distortion level even for track plus hold times as short as 30 ns. For a traditional open-loop output buffer, the ac (track mode) and dc (hold mode) distortion levels are often the same.

Droop Rate

Droop rate does not necessarily affect a track and hold's distortion characteristics. If the droop rate is constant versus the input voltage for a given hold time, it manifests itself as a dc offset to the encoder. For the AD9100, the droop rate is typically ±1 mV/μs. If a signal is held for 1 μs, a subsequent encoder would see a 1 mV offset voltage. If there is no droop sensitivity to the held voltage value, the 1 mV offset would be constant and "ride" on the input signal and introduce no hold-mode nonlinearities.

In instances in which droop rate varies proportionately to the magnitude of the held voltage signal level, a gain error only is introduced to the A/D encoder. The AD9100 has a droop sensitivity to the input level of 1.5 mV/V−μsec. For a 2 V p-p input signal, this translates to a 0.15%/μs gain error and does not cause additional distortion errors.

For the AD9100, droop sensitivity to input level is insignificant. However, *hold times longer than about 2 μs can cause distortion* due to the $R \times C_H$ time constant at the hold capacitor. In addition, hold mode noise will increase linearly vs. hold time and thus degrade SNR performance.

Layout Considerations

For best performance results, good high speed design techniques must be applied. The component (top) side ground plane should be as large as possible; two-ounce copper cladding is preferable. All runs should be as short as possible, and decoupling capacitors must be used.

Figure 2 is the schematic of a recommended AD9100 evaluation board. (Contact factory concerning availability of assembled boards.) All 0.01 μF decoupling capacitors should be low inductance surface mount devices (P/N 05085C103MT050 from AVX) and connected on the component side within 30 mils of the designated pins, with the other sides soldered directly to the top ground plane.

The 10 μF low frequency power supply tantalum decoupling capacitors should be located within 1.5 inches of the AD9100. The common 0.01 μF supply capacitors can be wired together. The common power supply bus (connected to the 10 μF capacitor and power supply source) can be routed to the underside of the board to the daisy chain wired 0.01 μF supply capacitors.

For remote input and/or output drive applications, controlled impedances are required to minimize line reflections which will reduce signal fidelity. When capacitive and/or high impedance levels are present, the load and/or source should be physically located within approximately one inch of the AD9100. Note that a series resistance, R_S, is required if the load is greater than 6 pF. (The Recommended R_S vs. CL chart in the "Typical Performance Section" shows values of R_S for various capacitive loads which result in no more than a 20% increase in settling time for loads up to 80 pF.) As much of the ground plane as possible should be removed from around the V_{IN} and V_{OUT} pins to minimize coupling onto the analog signal path.

While a single ground plane is recommended, the analog signal and differential ECL clock ground currents follow a narrow path directly under their common voltage signal line. To reduce reflections, especially when terminations are used for transmission line efficiency, the clock, V_{IN}, and V_{OUT} signals and respective ground paths should not cross each other; if they do, unwanted coupling can result.

High current ground transients via the high frequency decoupling capacitors can also cause unwanted coupling to the V_{IN} and V_{OUT} current loops. Therefore, these analog terminations should be kept as far as possible from the power supply decoupling capacitors to minimize feedthrough.

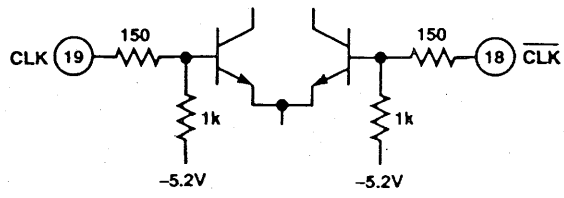
Using Sockets

Pin sockets (P/N 6-330808-3 from AMP) should be used if the device can not be soldered directly to the PCB. High profile or wire wrap type sockets will dramatically reduce the dynamic performance of the device in addition to increasing the case-to-ambient thermal resistance.

Driving the Encode Clock

The AD9100 requires a differential ECL clock command. Due to the high gain bandwidth of the AD9100 internal switch, the input clock should have a slew rate of at least 100 V/μs.

To obtain maximum signal to noise performance, especially at high analog input frequencies, a low jitter clock source is required. The AD9100 clock can be driven by an AD96685, an ultrahigh speed ECL comparator with very low jitter.



Clock/$\overline{\text{Clock}}$ Input Stage

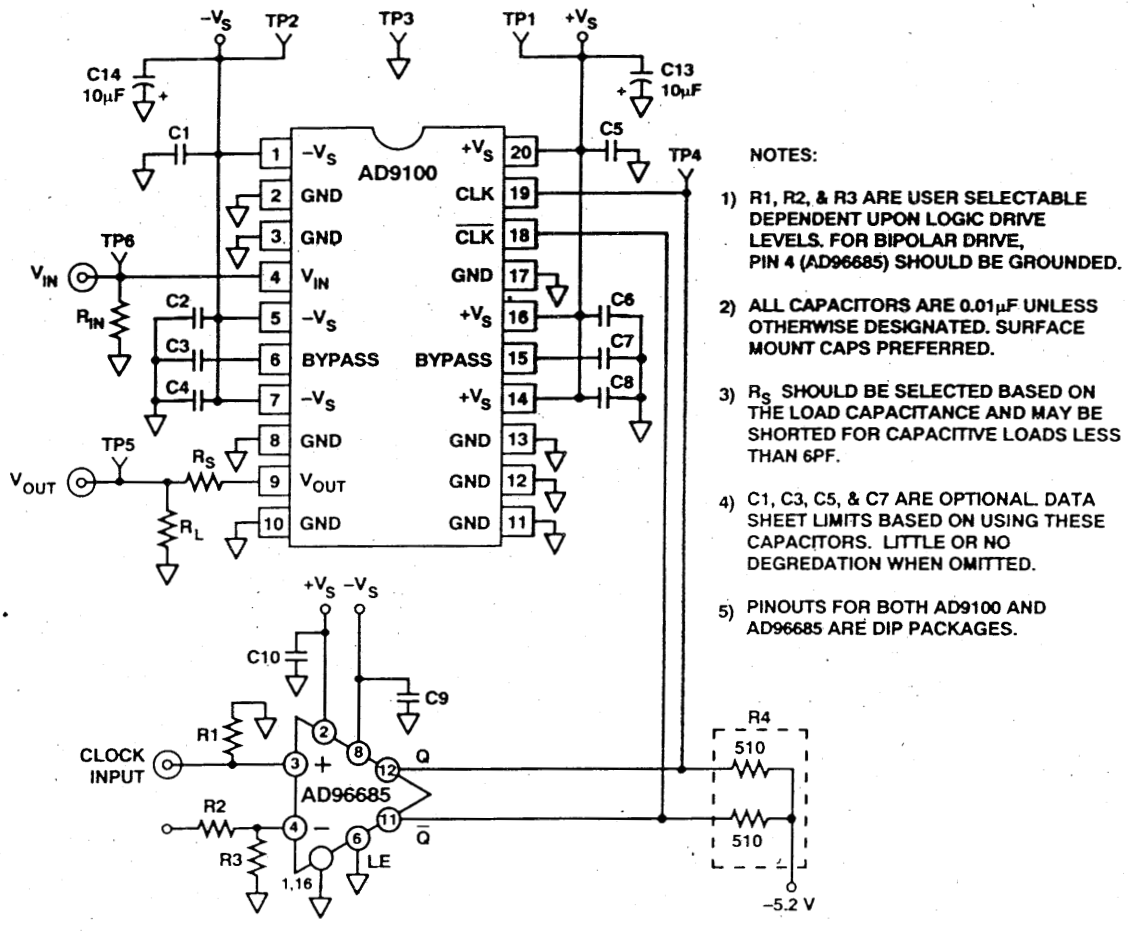


Figure 2. AD9100 Application Diagram

Driving the Analog Input

Special care must be taken to ensure that the analog input signal is not compromised before it reaches the AD9100. To obtain maximum signal to noise performance, a very low phase noise analog source is required. In addition, input filtering and/or a low harmonic signal source is necessary to maximize the spurious free dynamic range. Any required filtering should be done close to the AD9100 and away from any digital lines.

Overdriving the Analog Input

The AD9100 has input clamps that prevent hard saturation of the output buffer, thereby providing fast over-voltage recovery when the analog input transitions to the linear region (±2 V). The clamps are set internally at ±2.3 V and cannot be altered by the user. The output settles to 0.1% of its value 21 ns after the over-voltage condition is alleviated. When the analog input is outside the linear region, the analog output will be at either +2.2 V or −2.2 V.

Matching the AD9100 to A/D Encoders

The AD9100's analog output level may have to be offset or amplified to match the full-scale range of a given A/D converter. This can generally be accomplished by inserting an amplifier after the AD9100. For example, the AD671 is a 12-bit 500 ns monolithic ADC encoder that requires a 0 to +5 V full-scale analog input. An AD84X series amplifier could be used to condition the AD9100 output to match the full-scale range of the AD671.

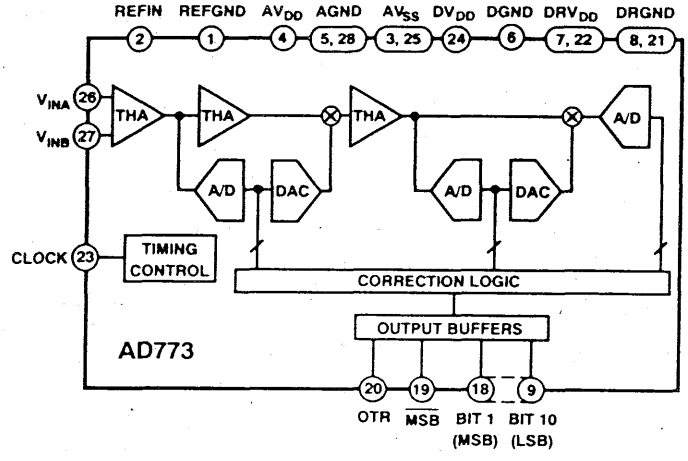
10-Bit 18 MSPS Monolithic A/D Converter

AD773

FEATURES

Monolithic 10-Bit 18 MSPS A/D Converter
Low Power Dissipation: 1.2 W
Signal-to-Noise Plus Distortion Ratio
f_{IN} = 1 MHz: 56 dB
f_{IN} = 8 MHz: 53 dB
Guaranteed No Missing Codes
On-Chip Track-and-Hold Amplifier
100 MHz Full Power Bandwidth
High Impedance Reference Input
Out of Range Output
Twos Complement and Binary Output Data
Available in Commercial and Military Temperature Ranges

FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTION

The AD773 is a monolithic 10-bit, 18 MSPS analog-to-digital converter incorporating an on-board, high performance track-and-hold amplifier (THA). The AD773 converts video bandwidth signals without the use of an external THA. The AD773 implements a multistage differential pipelined architecture with output error correction logic. The AD773 offers accurate performance and guarantees no missing codes over the full operating temperature range.

Output data is presented in binary and twos complement format. An out of range (OTR) signal indicates the analog input voltage is beyond the specified input range. OTR can be decoded with the MSB/$\overline{\text{MSB}}$ pins to signal an underflow or overflow condition. The high impedance reference input allows multiple AD773s to be driven in parallel from a single reference.

The combined dc precision and dynamic performance of the AD773 is useful in a variety of applications. Typical applications include: video enhancement, HDTV, ghost cancellation, ultrasound imaging, radar and high speed data acquisition.

The AD773 was designed using Analog Devices' ABCMOS-1 process which utilizes high speed bipolar and 2-micron CMOS transistors on a single chip. High speed, precision analog circuits are now combined with high density logic circuits. Laser trimmed thin film resistors are used to optimize accuracy and temperature stability.

The AD773 is packaged in a 28-pin ceramic DIP and is available in commercial (0°C to +70°C) and military (−55°C to +125°C) grades.

PRODUCT HIGHLIGHTS

1. On-board THA
   The high impedance differential input THA eliminates the need for external buffering or sample and hold amplifiers. The THA offers the choice of differential or single-ended inputs. Input current is typically 5 μA.
2. High Impedance Reference Input
   The high impedance reference input (200 kΩ) allows direct connection with standard +2.5 V references, such as the AD680, AD580 and REF43.
3. Output Data Flexibility
   Output data is available in bipolar offset and bipolar twos complement binary format.
4. Out of Range (OTR)
   The OTR output bit indicates when the input signal is beyond the AD773's input range.

REV. 0

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 617/329-4700 Fax: 617/326-8703 Twx: 710/394-6577
Telex: 924491 Cable: ANALOG NORWOODMASS

AD773—SPECIFICATIONS

DC SPECIFICATIONS

(T_{MIN} to T_{MAX} with AV_{DD} = +5 V ± 5%, AV_{SS} = −5 V ± 5%, DV_{DD} = +5 V ± 5%, DRV_{DD} = +5 V ± 5%, V_{REF} = +2.500 V unless otherwise indicated)

Parameter	AD773J			AD773K			Units
	Min	Typ	Max	Min	Typ	Max	
RESOLUTION	10			10			Bits
DC ACCURACY (+25°C)							
Integral Nonlinearity							LSB
T_{MIN} to T_{MAX}		±0.75			±0.75	±2	LSB
Differential Linearity Error							LSB
T_{MIN} to T_{MAX}		±0.75			±0.75	±1	LSB
Offset		0.5			0.5	3.5	% FSR
Gain Error		0.5			0.5	2.0	% FSR
No Missing Codes					GUARANTEED		
ANALOG INPUT							
Input Range		1			1		V p–p
Input Current		5	20		5	20	μA
Input Capacitance			10			10	pF
REFERENCE INPUT							
Reference Input Resistance	50	200		50	200		kΩ
Reference Input		2.5			2.5		Volts
LOGIC INPUT							
High Level Input Voltage	+3.5			+3.5			V
Low Level Input Voltage			+1.0			+1.0	V
High Level Input Current (V_{IN} = DV_{DD})	−10		+10	−10		+10	μA
Low Level Input Current (V_{IN} = 0 V)	−10		+10	−10		+10	μA
Input Capacitance		10			10		pF
LOGIC OUTPUTS							
High Level Output Voltage (I_{OH} = 0.5 mA)	+2.4			+2.4			V
Low Level Output Voltage (I_{OL} = 1.6 mA)			+0.4			+0.4	V
POWER SUPPLIES							
Operating Voltages							
AV_{DD}	+4.75		+5.25	+4.75		+5.25	Volts
AV_{SS}	−5.25		−4.75	−5.25		−4.75	Volts
DV_{DD}, DRV_{DD}	+4.75		+5.25	+4.75		+5.25	Volts
Operating Current							
IAV_{DD}		85	110		85	110	mA
IAV_{SS}		−140	−205		−140	−205	mA
IDV_{DD}		15	25		15	25	mA
$IDRV_{DD}$[1]		10	15		10	15	mA
POWER CONSUMPTION[2]		1.2	1.5		1.2	1.5	W
POWER SUPPLY REJECTION		6	16		6	16	mV/V
TEMPERATURE RANGE							
Specified (J/K)	0		+70	0		+70	°C

NOTES

[1] C_L = 15 pF typical.

[2] 100% production tested.

Specifications subject to change without notice. See Definition of Specifications for additional information.

AC SPECIFICATIONS

(T_{MIN} to T_{MAX} with AV_{DD} = +5 V ± 5%, AV_{SS} = −5 V ± 5%, DV_{DD} = +5 V ± 5%, DRV_{DD} = +5 V ± 5%, V_{REF} = +2.500 V unless otherwise indicated, f_{SAMPLE} = 18 MSPS, f_{IN} amplitude = −0.5 dB)

Parameter	AD773J Min	AD773J Typ	AD773J Max	AD773K Min	AD773K Typ	AD773K Max	Units
DYNAMIC PERFORMANCE[1]							
Signal-to-Noise plus Distortion (S/N+D) Ratio							
f_{IN} = 1 MHz	52	56		54	56		dB
f_{IN} = 8.1 MHz	45	53		47	53		dB
f_{IN} = 9 MHz		53			53		dB
Effective Number of Bits (ENOB)							
f_{IN} = 1 MHz		9.0			9.0		Bits
f_{IN} = 8.1 MHz		8.5			8.5		Bits
f_{IN} = 9 MHz		8.5			8.5		Bits
Total Harmonic Distortion (THD)							
f_{IN} = 1 MHz		−66	−57		−66	−59	dB
f_{IN} = 8.1 MHz		−58	−46		−58	−48	dB
f_{IN} = 9 MHz		−56			−56		dB
Spurious Free Dynamic Range[2]		67			67		dB
Full Power Bandwidth		100			100		MHz
Intermodulation Distortion (IMD)[3]							
Second Order Products		−69			−69		dB
Third Order Products		−61			−61		dB
Differential Phase		0.2			0.2		Degree
Differential Gain		0.4			0.4		%
Transient Response		25			25		ns
Overvoltage Recovery Time		25			25		ns

NOTES
[1]For typical dynamic performance curves at f_{SAMPLE} = 16.2 MSPS and 18 MSPS; see Figures 2 through 13.
[2]f_{IN} = 1 MHz.
[3]fa = 1.0 MHz, fb = 1.05 MHz.
Specifications subject to change without notice.

TIMING SPECIFICATIONS

(for all grades T_{MIN} to T_{MAX} with AV_{DD} = +5 V ± 5%, AV_{SS} = −5 V ± 5%, DV_{DD} = +5 V ± 5%, DRV_{DD} = +5 V ± 5%, V_{REF} = +2.500 V unless otherwise indicated, f_{SAMPLE} = 18 MSPS)

	Symbol	Min	Typ	Max	Units
Conversion Rate				18	MSPS
Clock Period	t_{CLK}	55			ns
Clock High	t_{CH}	27			ns
Clock Low	t_{CL}	27			ns
Output Delay	t_{OD}		20		ns
Aperture Delay			7		ns
Aperture Jitter			8		ps
Pipeline Delay (Latency)				4	Clock Cycles

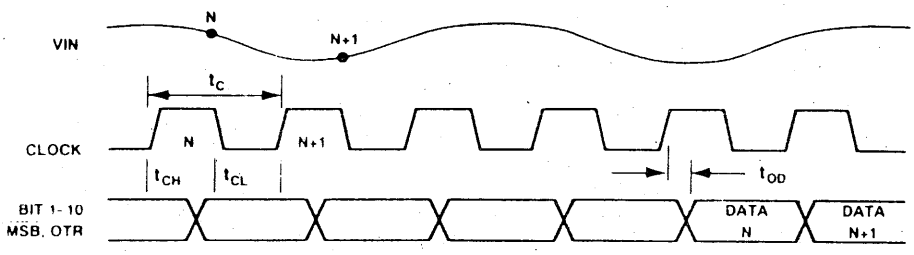


Figure 1. AD773 Timing Diagram

CAUTION

ESD (electrostatic discharge) sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are inserted.

ABSOLUTE MAXIMUM RATINGS*

Parameter	With Respect to	Min	Max	Units
AV_{DD}	AGND	−0.5	+6.5	V
AV_{SS}	AGND	−6.5	+0.5	V
V_{INA}, V_{INB}	AGND	−6.5	+6.5	V
DV_{DD}, DRV_{DD}	DGND, DRGND	−0.5	+6.5	V
AGND	DGND, DRGND	−1.0	+1.0	V
AV_{DD}, AV_{SS}	DV_{DD}, DRV_{DD}	−6.5	+0.5	V
CLK	DV_{DD}, DRV_{DD}	−6.5	+0.5	V
REFIN	REFGND, AGND	−0.5	+6.5	V
Junction Temperature			+150	°C
Storage Temperature		−65	+150	°C
Lead Temperature (10 sec)			+300	°C

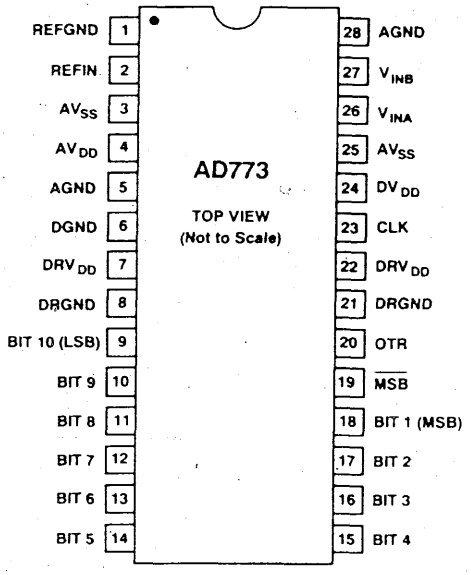
*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

ORDERING GUIDE

Model	Temperature Range	Description	Package Option*
AD773JD	0°C to +70°C	28-Pin Ceramic DIP	D-28
AD773KD	0°C to +70°C	28-Pin Ceramic DIP	D-28

*D = Ceramic DIP.

PIN CONFIGURATION



PIN DESCRIPTION

Symbol	Pin No.	Type	Name and Function
AGND	5, 28	P	Analog Ground.
AV_{DD}	4	P	+5 V Analog Supply.
AV_{SS}	3, 25	P	−5 V Analog Supply.
BIT 1 (MSB)	18	DO	Most Significant Bit.
BIT 2–BIT 9	17–10	DO	Data Bit 2 through Data Bit 9.
BIT 10 (LSB)	9	DO	Least Significant Bit.
CLK	23	DI	Clock Input. The AD773 will initiate a conversion on the falling edge of the clock input. See the Timing Diagram for details.
DV_{DD}	24	P	+5 V Digital Supply.
DRV_{DD}	7, 22	P	+5 V Digital Supply for the output drivers.
DGND	6	P	Digital Ground.
DRGND	8, 21	P	Digital Ground for the output drivers.
$\overline{MSB}$	19	DO	Inverted Most Significant Bit. Provides twos complement output data format.
OTR	20	DO	Out of Range is Active HIGH on the leading edge of Code 0 or the trailing edge of Code 1023. See Output Data Format Table II.
REF GND	1	AI	REF GND is connected to the ground of the external reference.
REF IN	2	AI	REF IN is the external 2.5 V reference input, taken with respect to REF GND.
V_{INA}	26	AI	(+) Analog input signal to the differential input THA.
V_{INB}	27	AI	(−) Analog input signal to the differential input THA.

Type: AI = Analog Input, DI = Digital Input, DO = Digital Output, P = Power.

EQUIVALENT REFERENCE INPUT CIRCUIT

The AD773 is designed to have a reference to analog input voltage ratio of 2.5:1. When the AD773 is configured for single-ended operation a 2.5 volt reference input establishes a full-scale analog input voltage of 1 V p–p (±500 mV with respect to V_{INB}). Although the AD773 is specified and tested with V_{REF} equal to 2.5 V and V_{IN} equal to ±500 mV the reference input voltage and analog input voltages can be changed. To optimize the AD773's performance the 2.5:1 ratio should be maintained. The simplified model of the AD773's reference input circuit is shown in Figure 22.

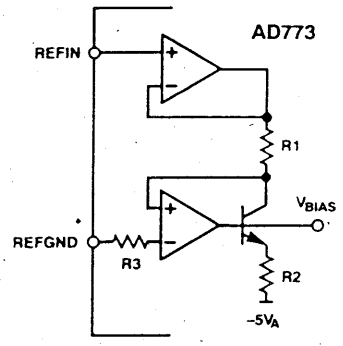


Figure 22. Typical Reference Input Circuit

The 2.5 V external reference is applied across resistor R1 producing a current which in turn generates a voltage V_{BIAS}. Multiple reference currents are generated from V_{BIAS} and are used throughout the converter. R3 is used to cancel errors induced by the input bias current of the REFGND buffer. Figure 23 shows the SNR performance as the reference voltage is varied from its nominal value of 2.5 V. The input full-scale voltage is defined by the following equation,

$$\textit{Input Full-Scale Voltage} = \frac{\textit{Reference Voltage}}{2.5}$$

The power dissipation is modulated by variations in the reference voltage. Figure 24 shows the variation in power dissipation versus reference voltage.

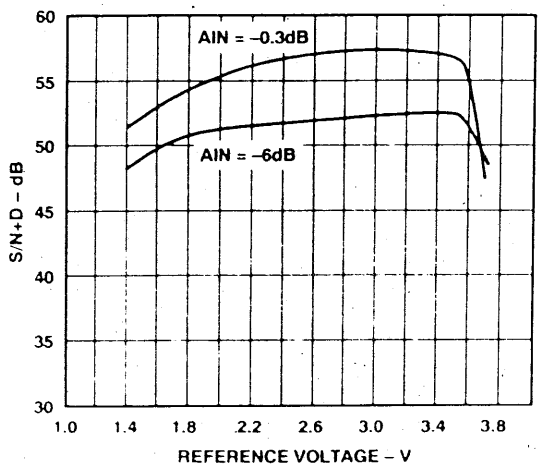


Figure 23. S/N + D vs. Reference Input Voltage. f_{CLK} 18 MSPS, f_{IN} 1 MHz

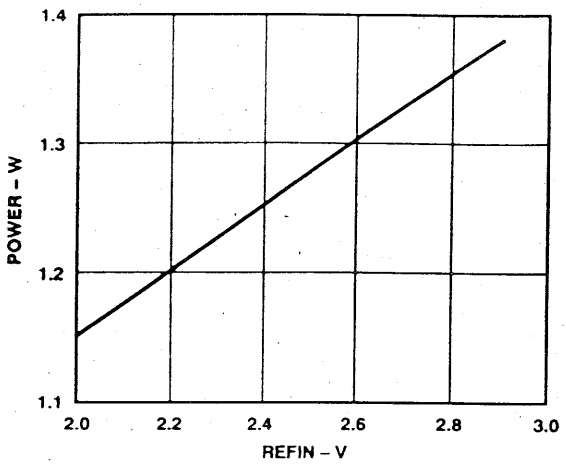


Figure 24. Power Dissipation vs. Reference Input Voltage

TRANSIENT RESPONSE

The fast settling input THA accurately converts full-scale input voltage swings in under one clock cycle. The THA's high impedance, fast slewing performance is critical in multiplexed or dc stepped (charge coupled devices, infrared detectors) systems. Figure 25 show the AD773's settling performance with an input signal stepped from −500 mV to 0V. As can be seen, the output code settles to its final value in under one clock cycle.

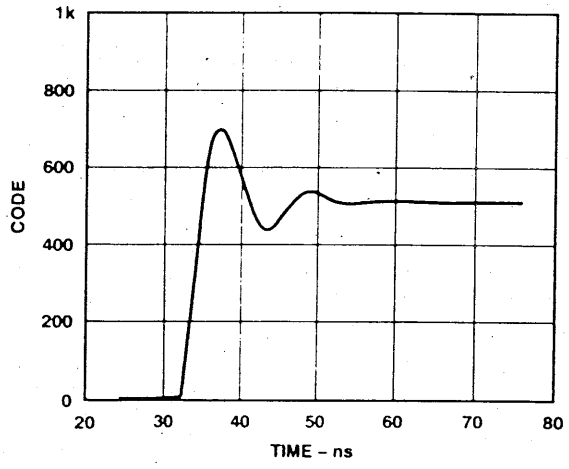


Figure 25. Typical AD773 Settling Time

OUTPUT DATA FORMAT

The AD773 provides both MSB and $\overline{MSB}$ outputs, delivering positive true offset binary and twos complement output data. Table II shows the AD773's output data format.

Table II. Output Data Format

Analog Input	Digital Output		
$V_{INA}-V_{INB}$	Offset Binary	Twos Complement	OTR
-499.5 mV	11 1111 1111	01 1111 1111	1
499 mV	11 1111 1111	01 1111 1111	0
0 mV	10 0000 0000	00 0000 0000	0
500 mV	00 0000 0000	10 0000 0000	0
-500.5 mV	00 0000 0000	10 0000 0000	1

OUT OF RANGE

An out-of-range condition exists when the analog input voltage is beyond the input range (±500 mV) of the converter. [Note the AD773 has a 4 clock cycle latency rating.] OTR (Pin 20) is set low when the analog input voltage is within the analog input range. OTR is set HIGH and will remain HIGH when the analog input voltage exceeds the input range by 1/2 LSB from the center of the full-scale output codes. OTR will remain HIGH until the analog input is within the input range. By logical ANDing OTR with the MSB and its complement, overrange high or underrange low conditions can be detected. Table III is a truth table for the over/under range circuit in Figure 26. Systems requiring programmable gain conditioning prior to the AD773 can immediately detect an out of range condition, thus eliminating gain selection iterations.

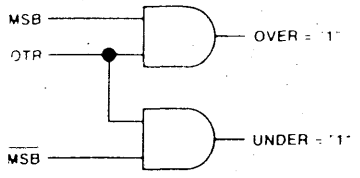


Figure 26. Overrange or Underrange Logic

Table III. Out-of-Range Truth Table

OTR	MSB	ANALOG INPUT IS
0	0	In Range
0	1	In Range
1	0	Underrange
1	1	Overrange

GROUNDING AND LAYOUT RULES

As is the case for any high performance device, proper grounding and layout techniques are essential in achieving optimal performance. (Note—Figures 28–32 are not to scale.) The analog and digital grounds on the AD773 have been separated to optimize the management of return currents in a system. It is recommended that a 4-layer printed circuit board (PCB) which employs ground planes and power planes be used with the AD773. The use of ground and power planes offers distinct advantages:

1. The minimization of the loop area encompassed by a signal and its return path.
2. The minimization of the impedance associated with ground and power paths.
3. The inherent distributed capacitor formed by the power plane, PCB insulation, and ground plane.

These characteristics result in both a reduction of electromagnetic interference (EMI) and an overall improvement in performance.

It is important to design a layout which prevents noise from coupling onto the input signal. The wide input bandwidth of the AD773 permits noise outside the desired Nyquist bandwidth to be digitized along with the desired signal. This can result in a higher overall level of spurious noise in the digitized spectrum. Digital signals should not be run in parallel with the input signal traces and should be routed away from the input circuitry. It is also suggested that the traces associated with V_{INA} and V_{INB} be the same length.

Separate analog and digital grounds should be joined together directly under the AD773 (see Figure 30). A solid ground plane under the AD773 is also acceptable if care is taken in the management of the power and ground return currents. A general "rule-of-thumb" for mixed signal layouts dictate that the return currents from digital circuitry should not pass through critical analog circuitry.

POWER SUPPLY DECOUPLING

The analog and digital supplies of the AD773 have been separated to prevent the typically large transients associated with digital circuitry from coupling into the analog supplies (AV_{DD}, AV_{SS}). Each analog power supply pin should be decoupled with a 0.1 μF capacitor located as close to the pin as possible. Additionally, 0.22 μF capacitors for the DRV_{DD} and DV_{DD} supplies are required to adequately suppress high frequency noise. For optimal performance, surface-mount capacitors are recommended. The inductance associated with the leads of through-hole ceramic capacitors typically render them ineffective at higher frequencies. A *complete* system will also incorporate tantalum capacitors in the 10–100 μF range to decouple low frequency noise and ferrite beads to limit high frequency noise.

The digital supplies have also been separated into DRV_{DD} and DV_{DD}. The DRV_{DD} pins provide power for the digital output drivers of the AD773 and are likely to contain high energy transients. Pin 22 should be decoupled directly to Pin 21 (DRGND) and Pin 7 should be decoupled directly to Pin 8 (DRGND) to minimize the length of the return path for these transients. A single +5 V supply is all that is required for DRV_{DD} and DV_{DD}, but decoupling DV_{DD} with an RC filter network is suggested (see Figure 27).

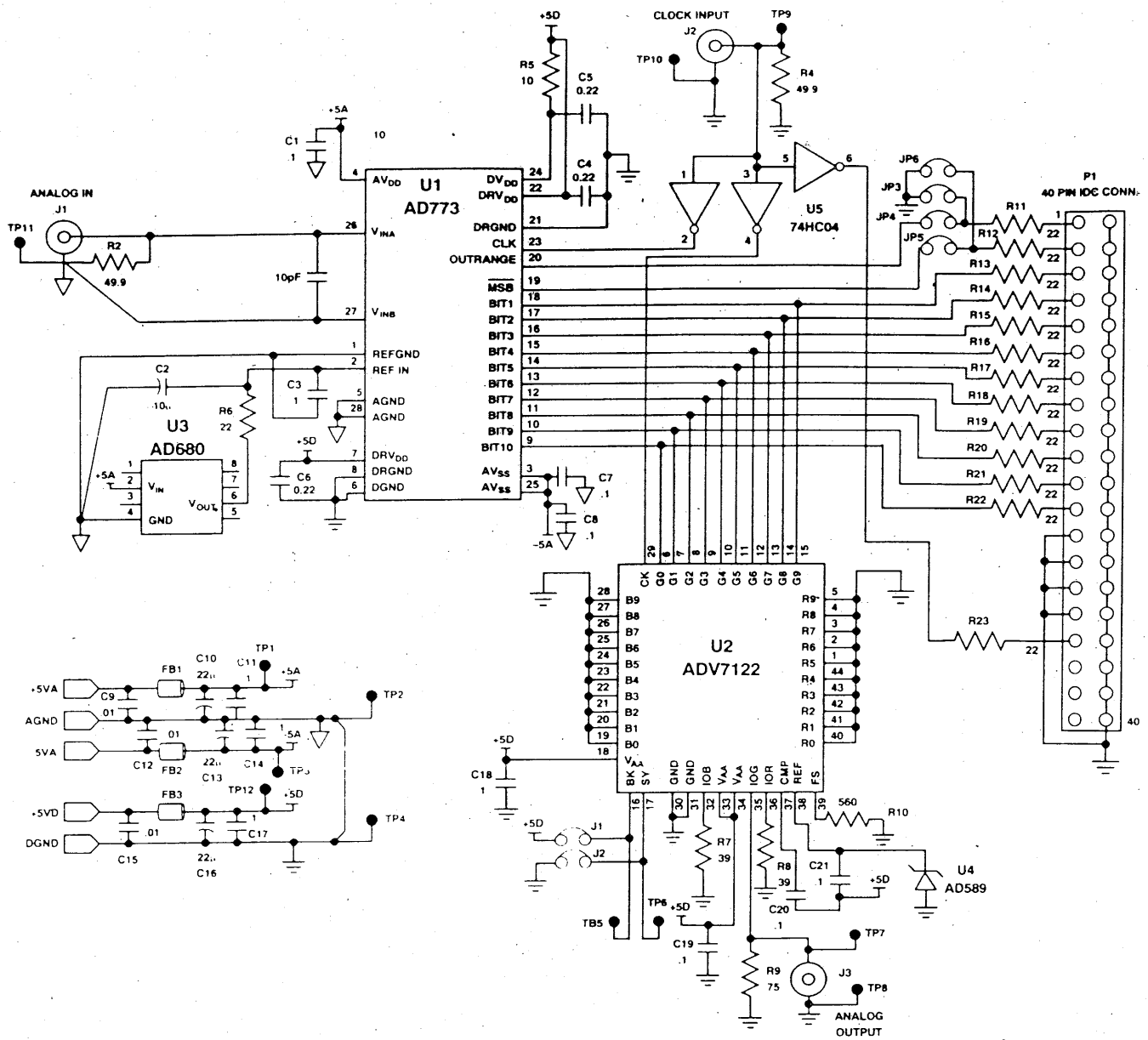


Figure 27. AD773 Evaluation Board Schematic

Table IV. Components List

Reference Designator	Description	Quantity
R2, R4	Resistor, 1%, 49.9 Ω	2
R5, R6, R11–R22	Resistor, 5%, 22 Ω	14
R7, R8	Resistor, 5%, 39 Ω	2
R9	Resistor, 5%, 75 Ω	1
R10	Resistor, 5%, 560 Ω	1
C1, C3–C8, C11, C14, C17–C21	Chip Cap, 0.1 µF	14
C2	Capacitor, Tantalum, 10 µF	1
C9, C12, C15	Chip Cap, 0.01 µF	3
C10, C13, C16	Capacitor, Tantalum, 22 µF	3
U1	AD773	1
U2	ADV7122	1
U3	AD680	1
U4	AD589	1
U5	74AS04	1
FB1–FB3	Ferrite Bead	3

National Semiconductor

54F/74F240•54F/74F241•54F/74F244
Octal Buffers/Line Drivers with TRI-STATE® Outputs

General Description

The 'F240, 'F241 and 'F244 are octal buffers and line drivers designed to be employed as memory and address drivers, clock drivers and bus-oriented transmitters/receivers which provide improved PC and board density.

Features

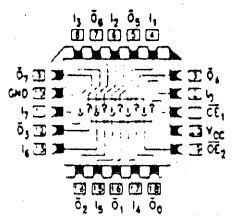
- TRI-STATE outputs drive bus lines or buffer memory address registers
- Outputs sink 64 mA (48 mA mil)
- 12 mA source current
- Input clamp diodes limit high-speed termination effects
- Guaranteed 4000V minimum ESD protection

Ordering Code: See Section 5

Connection Diagrams

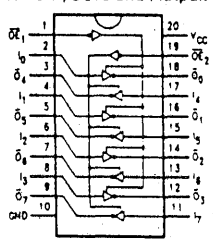
'F240

Pin Assignment for LCC



TL/F/9501-2

Pin Assignment for DIP, SOIC and Flatpak



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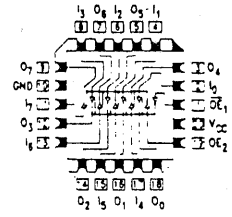
'F241



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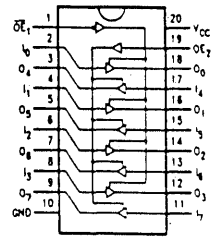

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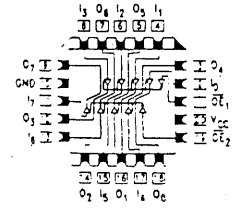
'F244



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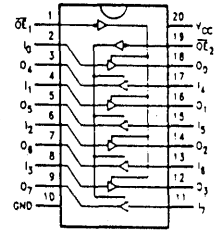
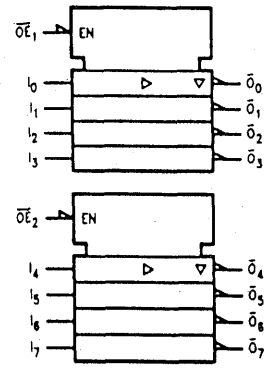


TL/F 9501-5

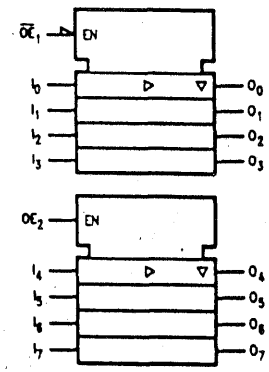
Logic Symbols

IEEE/IEC 'F240



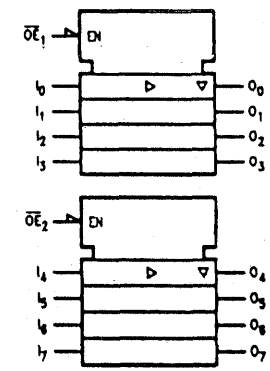
TL/F/9501-7

IEEE/IEC 'F241



TL/F/9501-8

IEEE/IEC 'F244



TL/F/950

Unit Loading/Fan Out: See Section 2 for U.L. Definitions

Pin Names	Description	54F/74F	
		U.L. HIGH/LOW	Input I_{IH}/I_{IL} Output I_{OH}/I_{OL}
$\overline{OE}_1$, $\overline{OE}_2$	TRI-STATE Output Enable Input (Active LOW)	1.0/1.667	20 μA/−1 mA
OE_2	TRI-STATE Output Enable Input (Active HIGH)	1.0/1.667	20 μA/−1 mA
I_0–I_7	Inputs ('F240)	1.0/1.667*	20 μA/−1 mA
I_0–I_7	Inputs ('F241, 'F244)	1.0/2.667*	20 μA/−1.6 mA
$\overline{O}_0$–$\overline{O}_7$, O_0–O_7	Outputs	600/106.6 (80)	−12 mA/64 mA (48 mA)

*Worst-case 'F240 enabled; 'F241, 'F244 disabled

Truth Tables

'F240

$\overline{OE}_1$	D_{1n}	O_{1n}	$\overline{OE}_2$	D_{2n}	O_{2n}
H	X	Z	H	X	Z
L	H	L	L	H	L
L	L	H	L	L	H

'F241

$\overline{OE}_1$	D_{1n}	O_{1n}	OE_2	D_{2n}	O_{2n}
H	X	Z	L	X	Z
L	H	H	H	H	H
L	L	L	H	L	L

'F244

$\overline{OE}_1$	D_{1n}	O_{1n}	$\overline{OE}_2$	D_{2n}	O_{2n}
H	X	Z	H	X	Z
L	H	H	L	H	H
L	L	L	L	L	L

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	−65°C to +150°C
Ambient Temperature under Bias	−55°C to +125°C
Junction Temperature under Bias	−55°C to +175°C
V_{CC} Pin Potential to Ground Pin	−0.5V to +7.0V
Input Voltage (Note 2)	−0.5V to +7.0V
Input Current (Note 2)	−30 mA to +5.0 mA
Voltage Applied to Output in HIGH State (with V_{CC} = 0V)	
Standard Output	−0.5V to V_{CC}
TRI-STATE Output	−0.5V to +5.5V
Current Applied to Output in LOW State (Max)	twice the rated I_{OL} (mA)
ESD Last Passing Voltage (Min)	4000V

Note 1: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Either voltage limit or current limit is sufficient to protect inputs.

Recommended Operating Conditions

Free Air Ambient Temperature	
Military	−55°C to +125°C
Commercial	0°C to +70°C
Supply Voltage	
Military	+4.5V to +5.5V
Commercial	+4.5V to +5.5V

DC Electrical Characteristics

Symbol	Parameter		54F/74F Min	54F/74F Typ	54F/74F Max	Units	V_{CC}	Conditions
V_{IH}	Input HIGH Voltage		2.0			V		Recognized as a HIGH Signal
V_{IL}	Input LOW Voltage				0.8	V		Recognized as a LOW Signal
V_{CD}	Input Clamp Diode Voltage				−1.2	V	Min	I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	54F 10% V_{CC}	2.4			V	Min	I_{OH} = −3 mA
		54F 10% V_{CC}	2.0					I_{OH} = −12 mA
		74F 10% V_{CC}	2.4					I_{OH} = −3 mA
		74F 10% V_{CC}	2.0					I_{OH} = −15 mA
		74F 5% V_{CC}	2.7					I_{OH} = −3 mA
V_{OL}	Output LOW Voltage	54F 10% V_{CC}			0.55	V	Min	I_{OL} = 48 mA
		74F 10% V_{CC}			0.55			I_{OL} = 64 mA
I_{IH}	Input HIGH Current	54F			20.0	μA	Max	V_{IN} = 2.7V
		74F			5.0			
I_{BVI}	Input HIGH Current Breakdown Test	54F			100	μA	μA	V_{IN} = 7.0V
		74F			7.0			
I_{CEX}	Output HIGH Leakage Current	54F			250	μA	Max	V_{OUT} = V_{CC}
		74F			50			
V_{ID}	Input Leakage Test	74F	4.75			V	0.0	I_{ID} = 1.9 μA All Other Pins Grounded
I_{OD}	Output Leakage Circuit Current	74F			3.75	μA	0.0	V_{IOD} = 150 mV All Other Pins Grounded
I_{IL}	Input LOW Current				−1.0	mA	Max	V_{IN} = 0.5V ($\overline{OE}_1$, $\overline{OE}_2$, OE_2, D_n ('F240'))
					−1.6			V_{IN} = 0.5V (D_n ('F241, 'F244'))
I_{OZH}	Output Leakage Current				50	μA	Max	V_{OUT} = 2.7V
I_{OZL}	Output Leakage Current				−50	μA	Max	V_{OUT} = 0.5V
I_{OS}	Output Short-Circuit Current		−100		−225	mA	Max	V_{OUT} = 0V
I_{ZZ}	Bus Drainage Test				500	μA	0.0V	V_{OUT} = 5.25V

DC Electrical Characteristics (Continued)

Symbol	Parameter	54F/74F Min	54F/74F Typ	54F/74F Max	Units	V_{CC}	Conditions
I_{CCH}	Power Supply Current ('F240)		19	29	mA	Max	V_O = HIGH
I_{CCL}	Power Supply Current ('F240)		50	75	mA	Max	V_O = LOW
I_{CCZ}	Power Supply Current ('F240)		42	63	mA	Max	V_O = HIGH Z
I_{CCH}	Power Supply Current ('F241, 'F244)		40	60	mA	Max	V_O = HIGH
I_{CCL}	Power Supply Current ('F241, 'F244)		60	90	mA	Max	V_O = LOW
I_{CCZ}	Power Supply Current ('F241, 'F244)		60	90	mA	Max	V_O = HIGH Z

AC Electrical Characteristics: See Section 2 for Waveforms and Load Configurations

Symbol	Parameter	74F T_A = +25°C, V_{CC} = +5.0V, C_L = 50 pF Min	Typ	Max	54F T_A, V_{CC} = Mil, C_L = 50 pF Min	Max	74F T_A, V_{CC} = Com, C_L = 50 pF Min	Max	Units	Fig. No.
t_{PLH}	Propagation Delay	3.0	5.1	7.0	3.0	9.0	3.0	8.0	ns	2-3
t_{PHL}	Data to Output ('F240)	2.0	3.5	4.7	2.0	6.0	2.0	5.7		
t_{PZH}	Output Enable Time ('F240)	2.0	3.5	4.7	2.0	6.5	2.0	5.7	ns	2-5
t_{PZL}		4.0	6.9	9.0	4.0	10.5	4.0	10.0		
t_{PHZ}	Output Disable Time ('F240)	2.0	4.0	5.3	2.0	6.5	2.0	6.3		
t_{PLZ}		2.0	6.0	8.0	2.0	12.5	2.0	9.5		
t_{PLH}	Propagation Delay	2.5	4.0	5.2	2.0	6.5	2.5	6.2	ns	2-3
t_{PHL}	Data to Output ('F241, 'F244)	2.5	4.0	5.2	2.0	7.0	2.5	6.5		
t_{PZH}	Output Enable Time	2.0	4.3	5.7	2.0	7.0	2.0	6.7	ns	2-5
t_{PZL}	('F241, 'F244)	2.0	5.4	7.0	2.0	8.5	2.0	8.0		
t_{PHZ}	Output Disable Time	2.0	4.5	6.0	2.0	7.0	2.0	7.0		
t_{PLZ}	('F241, 'F244)	2.0	4.5	6.0	2.0	7.5	2.0	7.0		

HY62C256/L

32K×8 CMOS Static RAM

DESCRIPTION

The HY62C256/L is a high speed low power, 32768-word by 8-bit CMOS static RAM fabricated using HYUNDAI's high performance twin tub CMOS process. This high reliability process coupled with innovative circuit design techniques, yields access times of 100ns maximum.

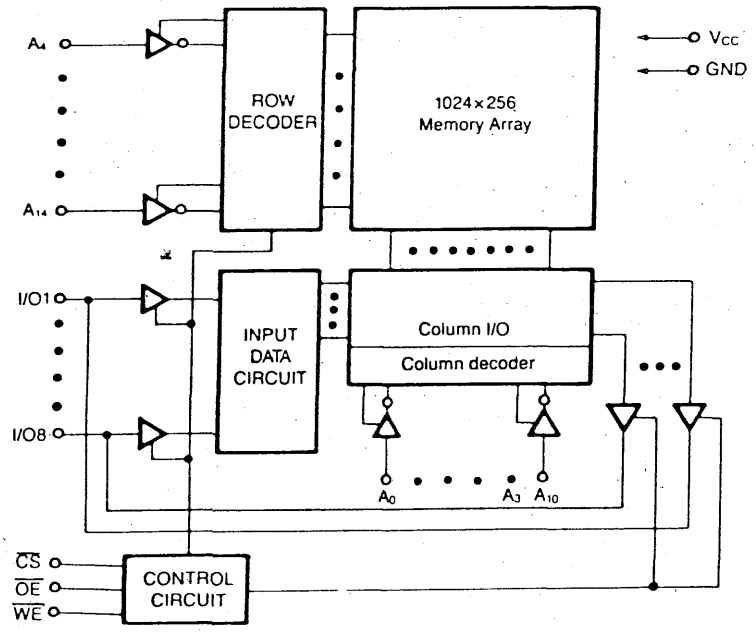
The HY62C256L has a data retention mode that guarantees data will remain valid at a minimum power supply voltages of 2.0 volts. Using twin tub CMOS technology, supply voltages from 2.0 to 5.5 volts have little effect on supply current in data retention mode. Reading the supply voltage to minimize current drain is unnecessary with the HY62C256/L family.

FEATURES

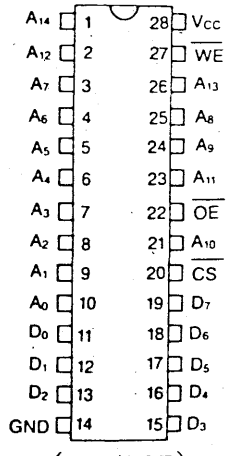
- **High speed — 100/120/150 ns (Max)**
- **Low Power dissipation.**
  -200 mW (Typ.) Operating
  -25 μW (Typ.) Standby (HY62C256L)
- **Data retention supply voltage: 2.0 — 5.5V**
- **Four transistor 2-Load Register memory cell**
- **Fully static operation**
  -No clock or refresh required
- **All inputs and outputs directly TTL compatible**
- **Tri-state outputs**
- **High reliability 28-pin 600 mil P-DIP**

	HY62C256/L-10	HY62C256/L-12	HY62C256/L-15
Maximum Access Time (ns)	100	120	150
Maximum Average Operating Current (mA)	70	70	70
Maximum Standby Current (mA)	1.0/0.1	1.0/0.1	1.0/0.1

FUNCTIONAL BLOCK DIAGRAM



PIN CONNECTIONS



(DIP/SOP)

PIN NAMES

A_0—A_{14}	ADDRESS
D_0—D_7	DATA INPUT/OUTPUT
$\overline{CS}$	CHIP SELECT
$\overline{WE}$	WRITE ENABLE
$\overline{OE}$	OUTPUT ENABLE
V_{CC}	POWER
GND	GROUND

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}, GND	Supply Voltage	−0.3 to 7	V
V_{IN}	Input Voltage	−0.3 to 7	
$V_{I/O}$	Input/Output Voltage Applied	−0.3 to 7	
T_{BIAS}	Temp Under Bias	−10 to 85	°C
T_A	Operating Temperature	0 to +70	°C
T_{STG}	Storage Temperature	−40 to +125	°C
P_T	Power Dissipation	1.0	W
I_{OUT}	DC Output Current	50	mA

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

RECOMMENDED DC OPERATING CONDITIONS

(T_A = 0°C to +70°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CC}	Supply voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.2	3.5	6.0	V
V_{IL}	Input Low Voltage	−0.3*	–	+0.8	V
C_L	Output Load	–	–	30	pF
TTL	Output Load	–	–	1	–

*−3.0V for 20ns pulse.

TRUTH TABLE

MODE	$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	I/O OPERATION
Standby	H	X	X	High Z
Read	L	L	H	D_{OUT}
Read	L	H	H	High Z
Write	L	X	L	D_{IN}

DC CHARACTERISTICS

(V_{CC} = 5V ± 10%, T_A = 0°C to +70°C).

SYMBOL	PARAMETER	TEST CONDITIONS	HY62C256			HY62C256L			UNIT
			MIN.	Typ[1]	MAX.	MIN.	TYP[1]	MAX.	
$\|I_{LI}\|$	Input Leakage Current	V_{IN} = GND to V_{CC}	–	–	2	–	–	2	μA
$\|I_{LO}\|$	Output Leakage Current	$\overline{CS}$ = V_{IH} or $\overline{OE}$ = V_{IH} or $\overline{WE}$ = V_{IL} $V_{I/O}$ = GND to V_{CC}	–	–	2	–	–	2	μA
I_{CC1}	Operating Power Supply Current	$\overline{CS}$ = V_{IL}, $I_{I/O}$ = 0mA	–	40	70	–	40	70	mA
I_{CC2}	Dynamic Operating Current	Min. Duty Cycle = 100%	–	35	70	–	35	70	mA
I_{SB}	Standby Power Supply Current	$\overline{CS}$ = V_{IH}	–	–	3	–	–	3	mA
I_{SB1}		$\overline{CS}$ ≥ V_{CC} – 0.2V,	–	–	1.0	–	–	0.1	mA
V_{OL}	Output Low Voltage	I_{OL} = 4mA	–	–	0.4	–	–	0.4	V
V_{OH}	Output High Voltage	I_{OH} = –1.0mA	2.4	–	–	2.4	–	–	V

1. V_{CC} = 5V, T_A = 25°C

AC CHARACTERISTICS

(V_{CC} = 5V ± 10%, T_A = 0°C to +70°C).

READ CYCLE

SYMBOL	PARAMETER	HY62C256/L-10		HY62C256/L-12		HY62C256/L-15		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{RC}	Read Cycle Time	100	–	120	–	150	–	ns
t_{AA}	Address Access Time	–	100	–	120	–	150	ns
t_{ACS}	Chip Select Access Time	–	100	–	120	–	150	ns
t_{CLZ}	Chip Selection to Output in Low Z	5	–	5	–	5	–	ns
t_{OE}	Output Enable to Output Valid	–	50	–	60	–	70	ns
t_{OLZ}	Output Enable to Output in Low Z	5	–	5	–	5	–	ns
t_{CHZ}	Chip Deselection to Output in High Z	0	35	0	40	0	50	ns
t_{OHZ}	Output Disable to Output in High Z	0	35	0	40	0	50	ns
t_{OH}	Output Hold from Address Change	10	–	10	–	10	–	ns

WRITE CYCLE

SYMBOL	PARAMETER	HY62C256/L-10		HY62C256/L-12		HY62C256/L-15		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{WC}	Write Cycle Time	100	–	120	–	150	–	ns
t_{CW}	Chip Selection to End of Write	80	–	85	–	100	–	ns
t_{AW}	Address Valid to End of Write	80	–	85	–	100	–	ns
t_{AS}	Address Set-up Time	0	–	0	–	0	–	ns
t_{WP}	Write Pulse Width	70	–	70	–	90	–	ns
t_{WR}	Write Recovery Time	0	–	0	–	0	–	ns
t_{OHZ}	Output Disable to Output in High Z	0	35	0	40	0	50	ns
t_{WHZ}	Write to Output in High Z	0	35	0	40	0	50	ns
t_{DW}	Data to Write Time Overlap	40	–	50	–	60	–	ns
t_{DH}	Data Hold from Write Time	0	–	0	–	0	–	ns
t_{OW}	Output Active from End of Write	0	–	0	–	0	–	ns

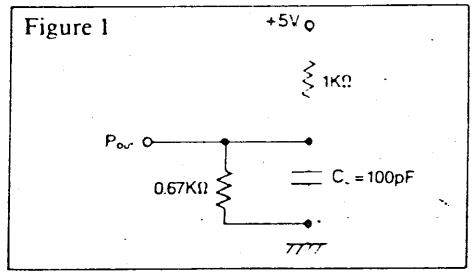
AC TEST CONDITIONS

(T_A = 0°C to +70°C)

Input Pulse Levels	0.8V to 2.4V
Input Rise and Fall Times	5 ns
Input and Output Timing Reference Levels	1.5V

OUTPUT LOAD

Figure 1



*Including scope and the Jig.

CAPACITANCE[1]

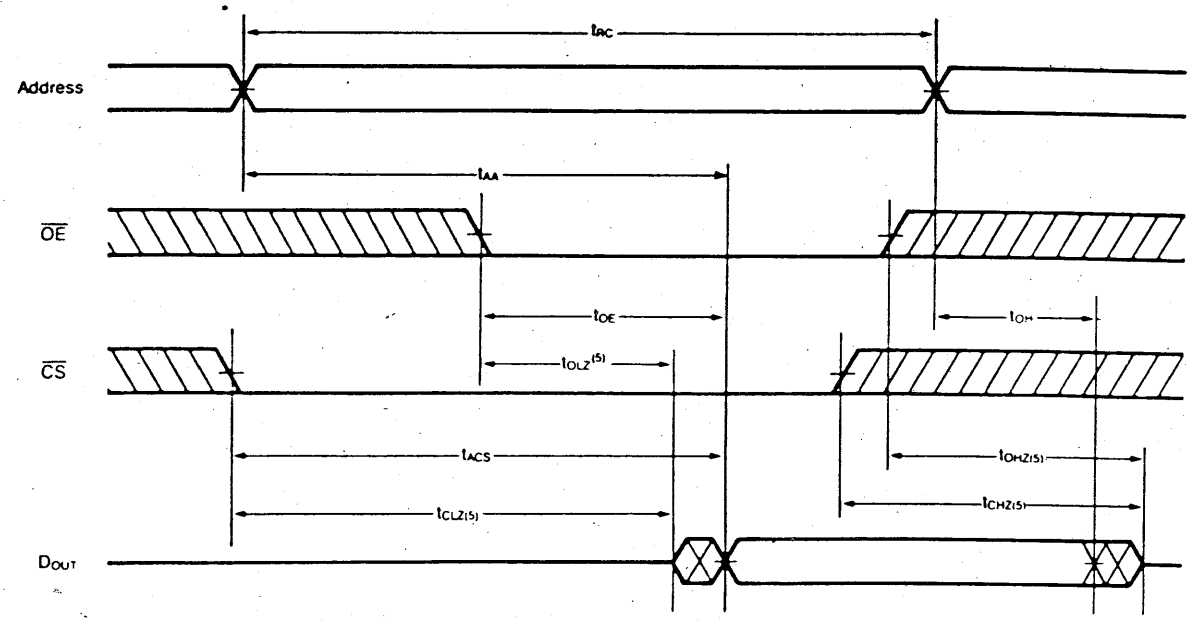
(T_A = 25°C f = 1.0 MHz)

SYMBOL	PARAMETER	CONDITIONS	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	5	pF
$C_{I/O}$	Input/Output Capacitance	$V_{I/O}$ = 0V	10	pF

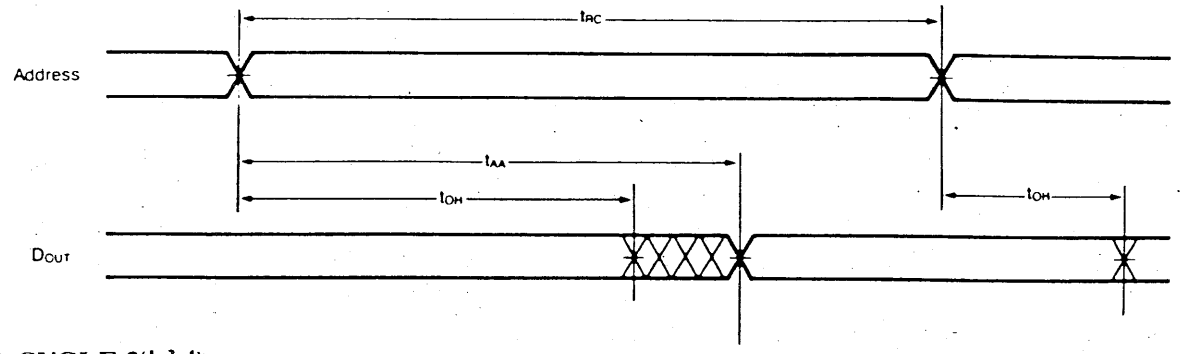
1. This parameter is sampled and not 100% tested.

TIMING DIAGRAMS

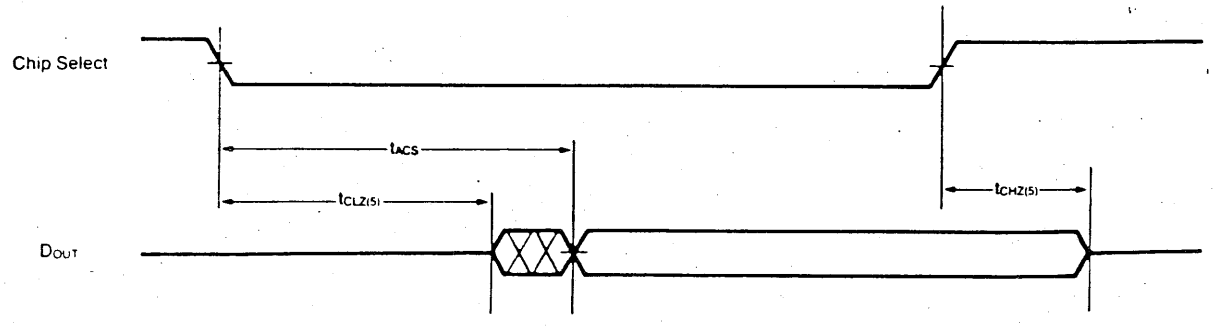
READ CYCLE 1[1]



READ CYCLE[1, 2, 4]

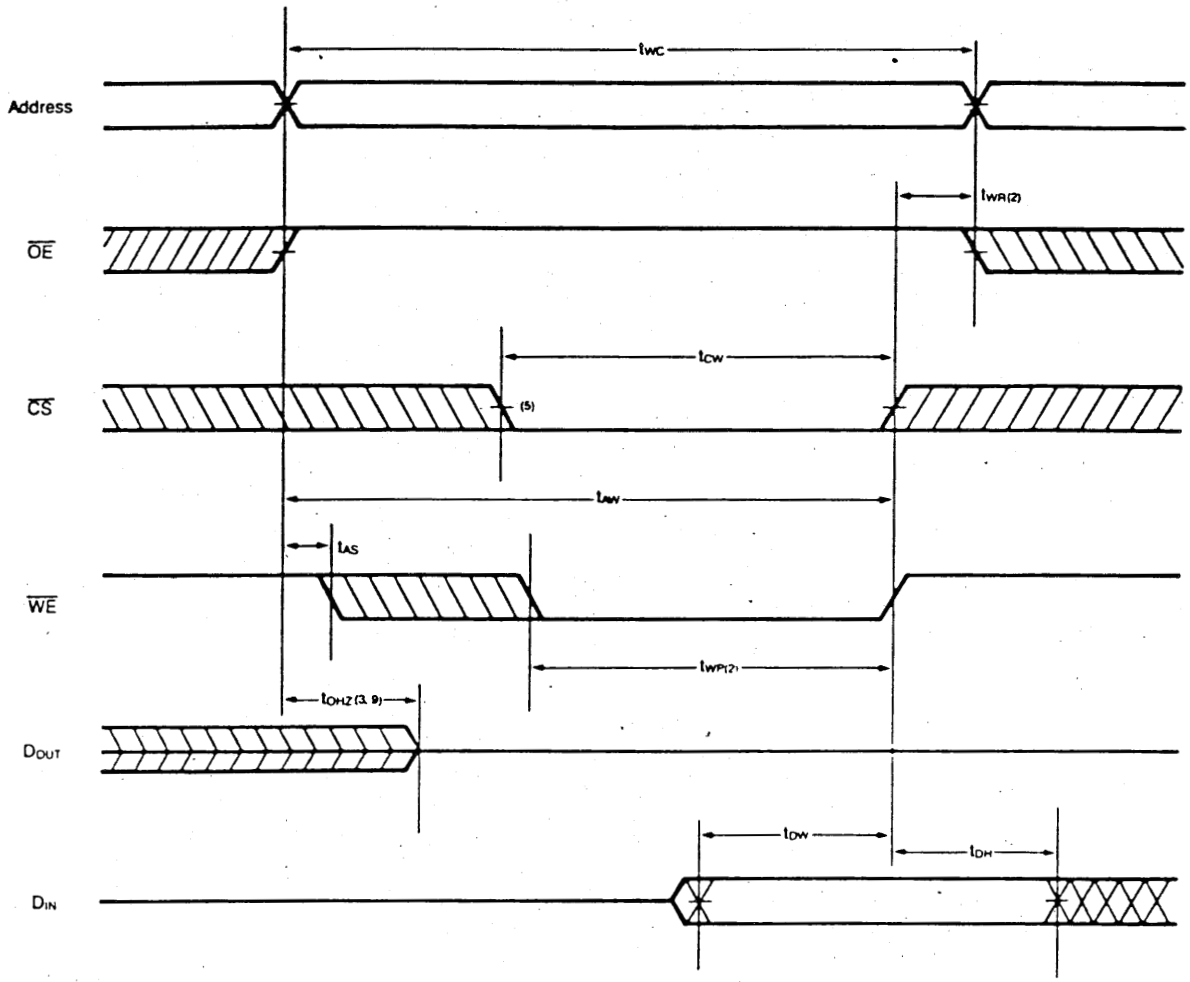


READ CYCLE 3[1, 3, 4]

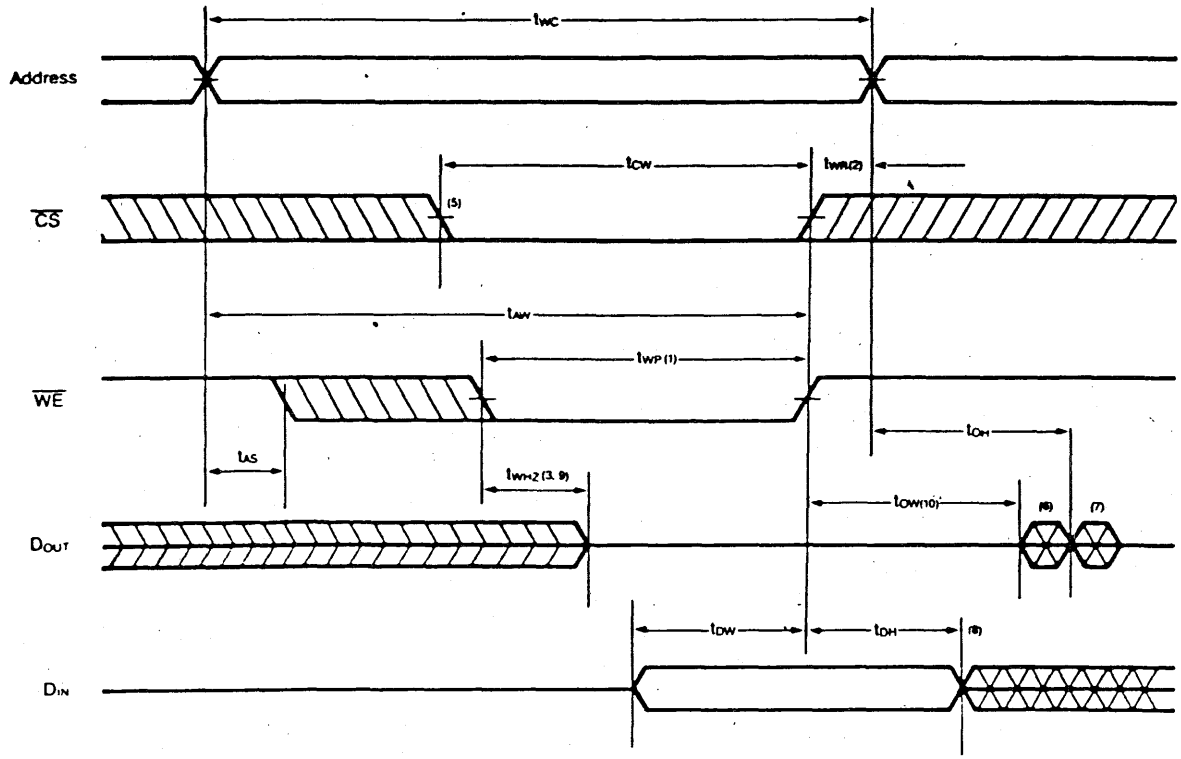


NOTES:
1. $\overline{WE}$ is High for Read Cycle.
2. Device is continuously selected. $\overline{CS} = V_{IL}$
3. Address valid prior to or coincident with $\overline{CS}$ transition low.
4. $\overline{OE} = V_{IL}$
5. Transition is measured ± 500mV from steady state. This parameter is sampled and not 100% tested.

WRITE CYCLE 1



WRITE CYCLE 2[5]



NOTES:

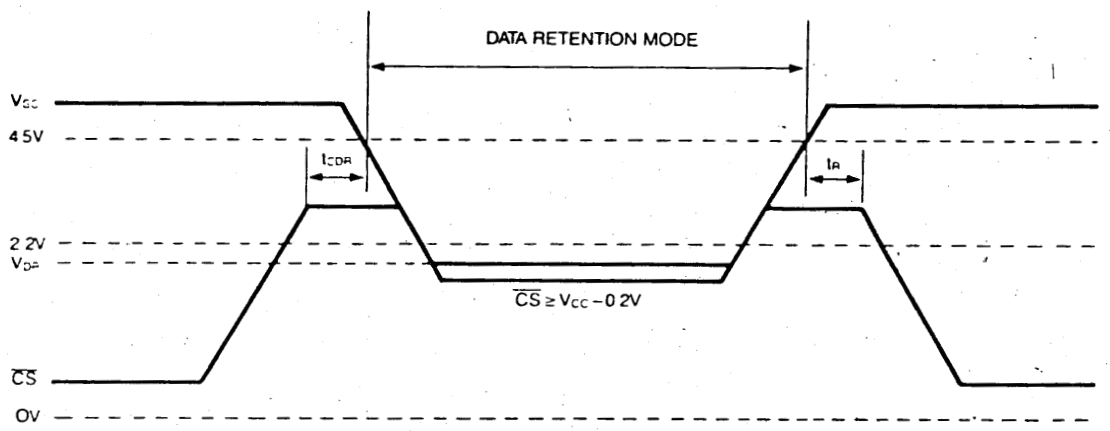
1. A write occurs during the overlap (t_{WP}) of a low $\overline{CS}$ and low $\overline{WE}$.
2. t_{WR} is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of write cycle.
3. During this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.
4. If the $\overline{CS}$ low transition occurs simultaneously with the $\overline{WE}$ low transitions or after the $\overline{WE}$ transition, outputs remain in a high impedance state.
5. $\overline{OE}$ is continuously low ($\overline{OE} = V_{IL}$).
6. D_{OUT} is the same phase of write data of this write cycle.
7. D_{OUT} is the read data of next address.
8. If $\overline{CS}$ is low during this period, I/O pins are in the output state. Then the data input signals of opposite phase to the outputs must not be applied to them.
9. Transition is measured ±500mV from steady state. This parameter is sampled and not 100% tested.

LOW V_{CC} DATA RETENTION CHARACTERISTICS

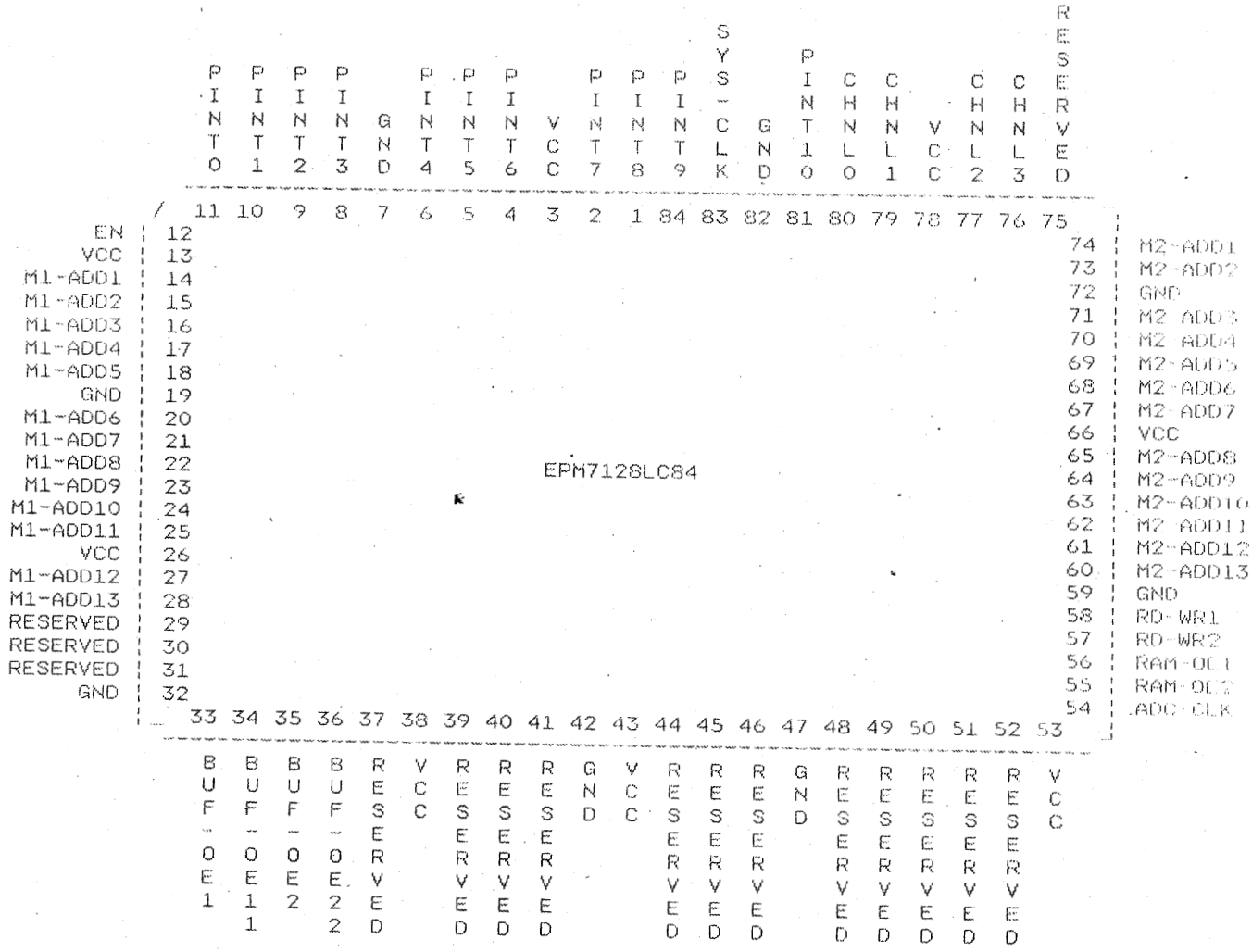
SYMBOL	PARAMETER	TEST CONDITIONS	MIN.	TYP	MAX.	UNIT
V_{DR}	Data Retention Supply Voltage	$\overline{CS}$>, V_{CC} − 0.2V	2.0	–	–	V
I_{CCDR}	Data Retention Current	V_{CC}=3.0V $\overline{CS}$>, V_{CC} − 0.2V	–	2	50	μA
t_{CDR}	Chip Deselect to Data Retention Time	See Data Retention Diagram	0	–	–	ns
t_R	Operation Recovery Time		t_{RC} (1)	–	–	ns

NOTES:
1. t_{RC} = Read Cycle Time

LOW V_{CC} DATA RETENTION DIAGRAM

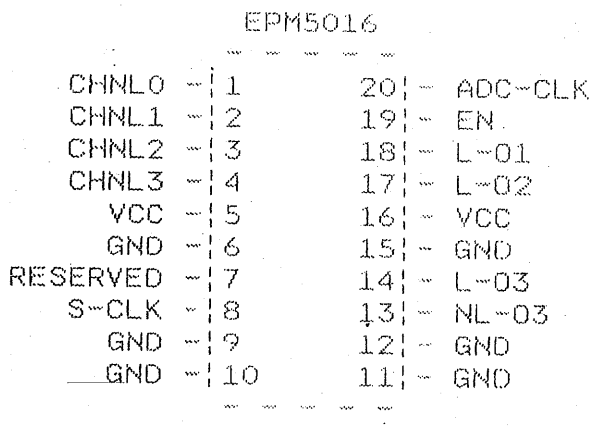


Device: EPM7128LC84
Turbo: ON
Security: OFF



N.C. = Not Connected.
VCC = Dedicated power pin, which MUST be connected to VCC.
GND = Dedicated ground pin or unused dedicated input, which MUST be connected to GND.
RESERVED = Unused I/O pin, which MUST be left unconnected.

Device: EPM5016
Security: OFF



N.C. = Not Connected.
VCC = Dedicated power pin, which MUST be connected to VCC.
GND = Dedicated ground pin or unused dedicated input, which MUST be connected to GND.
RESERVED = Unused I/O pin, which MUST be left unconnected.