A CONTROLLER COMPUTER INTERFACE AND DRIVER FOR A RADIO TELESCOPE

Bachelor of Engineering

in

ELECTRONICS & COMMUNICATION

by

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CERTIFICATE

THIS IS TO CERTIFY THAT THE FOLLOWING STUDENTS HAVE SATISFACTORILY COMPLETED THE PROJECT ENTITLED:

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Vihar R.Rai

Roque Nelson Pinto

Girish Krishnan

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A CONTROLLER
COMPUTER INTERFACE AND DRIVER FOR
A RADIO TELESCOPE CORRELATOR SYSTEM

A SYNOPSIS

INTRODUCTION

Radio Telescope is used to study the radiation from celestial objects in space, in the Radio frequency region. (Roughly in millimeter to meter long waves)

A Radio Telescope in its simplest form consists of three elements.

a) Antenna:

The antenna collects electromagnetic radiation from a selected region of the sky.

b) Receiver:

The output of the antenna is fed to the input of a receiver. A receiver amplifies a certain specified band of frequency and conditions it for further processing. In the simplest configuration the output of the receiver is fed to a detector

whose output is proportional to the power of the input radiations.

c) Indicator:

The indicator registers the detector reading and records it.

INTERFEROMETRY

A Radio Interferometer has two antennas separated by a distance and has their outputs multiplied in a correlator.

It is designed to give an output proportional to the average product of the voltages from the two antennas. In an interferometer the signal from the celestial source reaches the two elements with a small time difference. The delay is removed by a delay unit and then correlated to give a measure of one of the fourier components of the ratio brightness distribution.

A digital correlator system employs samplers each compromising of an orthogonal power splitter and two A/D converters. (one for each component) The sampler outputs are input to the delay units to suitably delay the signals. Then they are correlated in the correlators which is nothing but a process of multiplication and integration carried out in a multiplier and an accumulator.

This project describes the design of a 1024 channel

correlation receiver interface to a computer. The computer by an extensive decoding process selects and reads all the correlator outputs in a sequence via the interface.

DATA COLLECTOR

The computer interface serves the purpose of collecting and holding the correlator output data for the computer to read.

CONTROLLER - COMPUTER INTERFACE AND DRIVER OR MASTER CONTROLLER

It also enables the computer to output control signals to the correlator and delay circuits (and samplers).

A list of input to the master control board and their corresponding outputs are as follows.

Inputs : modify / reset code

Outputs : a) active resets

b) interrupt signals

c) reset signals

d) integration bank select signals

Inputs : A 48 MHz basic oscillator signal

Outputs : a) a four phase clock

b) a 5.46 ms timing pattern

c) update signals

d) blanking signals

INTRODUCTION

INTRODUCTION

Radio Telescope is used to study the radiation from celestial objects in space, in the Radio frequency region. (Roughy millimeter to meter long waves)

In 1932 a Bell Laboratories engineer, Karl Jansky, was investigating radio reception of an antenna system in order to design a Trans Atlantic telephone system. His antenna, about 100 feet long and pivoted so that the whole contraption could rotate, pinpointed a mysterious source of radiation. Surprisingly the radiation came from no where on earth, but from the centre of our galaxy, some 30,000 light years away. His study was much later continued by Grote Reber who on studing Jansky's report built his own Radio Telescope and studied the galactic nucleus, which hidden by a gas cloud could not be studied by optical means. Reber pinpointed some strong sources. Ever since Radio Telescope has contributed a lot to the progress in astronomy.

A Radio Telescope in its simplest form consists of three elements.

a) Antenna:

The antenna collects electromagnetic radiation from a selected region of the sky.

b) Receiver:

The output of the antenna is fed to the input of a

receiver. A receiver amplifies a certain specified band of frequency and conditions it for further processing. In the simplest configuration the output of the receiver is fed to a detector whose output is proportional to the power of the input radiation.

c) Indicator:

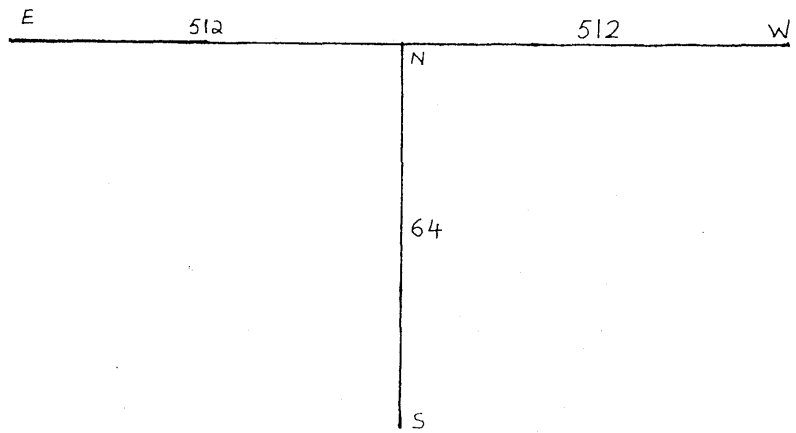
The indicator registers the detector reading and records it.

ANTENNAS

Radio waves from celestial objects are very weak and therefore the aperture of a radio telescope should be sufficiently large to get a clear image. A single telescope of very large aperture would be physically impractical to construct. Therefore radio telescopes of large apertures are built by using extended arrays of smaller telescopes which together make up a large aperture and are easily steerable.

The controller described in the present project was designed for a 1024 channel correlator system. This in turn is a receiver system for an array of helical antennas arranged in the form of a 'T'. The EW (east west) arm is two kilometres long and has 1024 antennas. The NS (north south) arm has 16 rows of 4 antennas each on movable trolleys. Before being fed into the samplers the outputs of every four antennas are combined in a four way power combiner. The outputs of eight such adjacent

combiners in the EW array are further combined in an eight way power combiner. The 48 group outputs after suitable amplification in the field are brought to a central receiver room. 32 outputs from EW array and 16 from NS array are further processed in a 16 X 32 = 512 channel complex correlation receiver.



These antenna outputs are passband signals and are mathematically to be regarded as vector signals containing both amplitude and phase information. The signals are split into two orthogonal signals by a phase splitter. In a complex correlator the signals are split into two orthogonal signals by a quadrature phase splitter Each sub matrix of 4 X 4 = 16 correlators form a correlator unit and are controlled by one microprocessor.

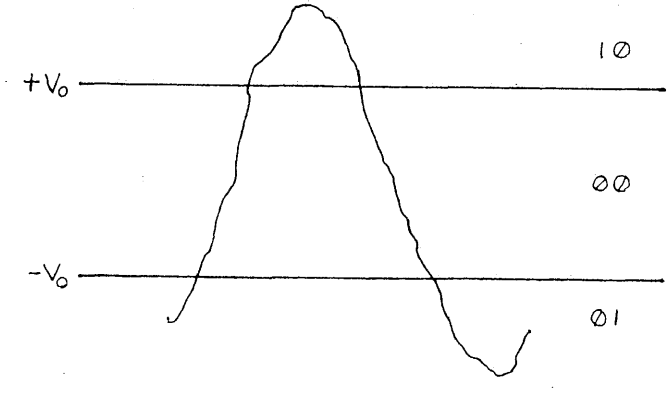
Inspite of carefully shielding the RF line-receivers and IF lines there is always a certain amount of cross talk between the individual channels. This causes spurious correlation over long integration intervals. To reduce Cross Talk a concept called Walsh Switching is used.

The Walsh function generator uses the same clock period as the system. (2^{16} / 12 micro seconds = 5.56 ms)

SAMPLER UNITS

The sampler units split analogue input signals into an in phase and a quadrature phase signal and then performs, in both paths, a two bit three level A/D conversion at a clock rate of 12 MHz. The analogue signal is compared with two levels, a +Vo and a -Vo, and a two bit code is generated which indicates if the analogue signal is above the upper level (+Vo), below the lower level (-Vo) or betweem them.

A/D Conversion in the Sampler



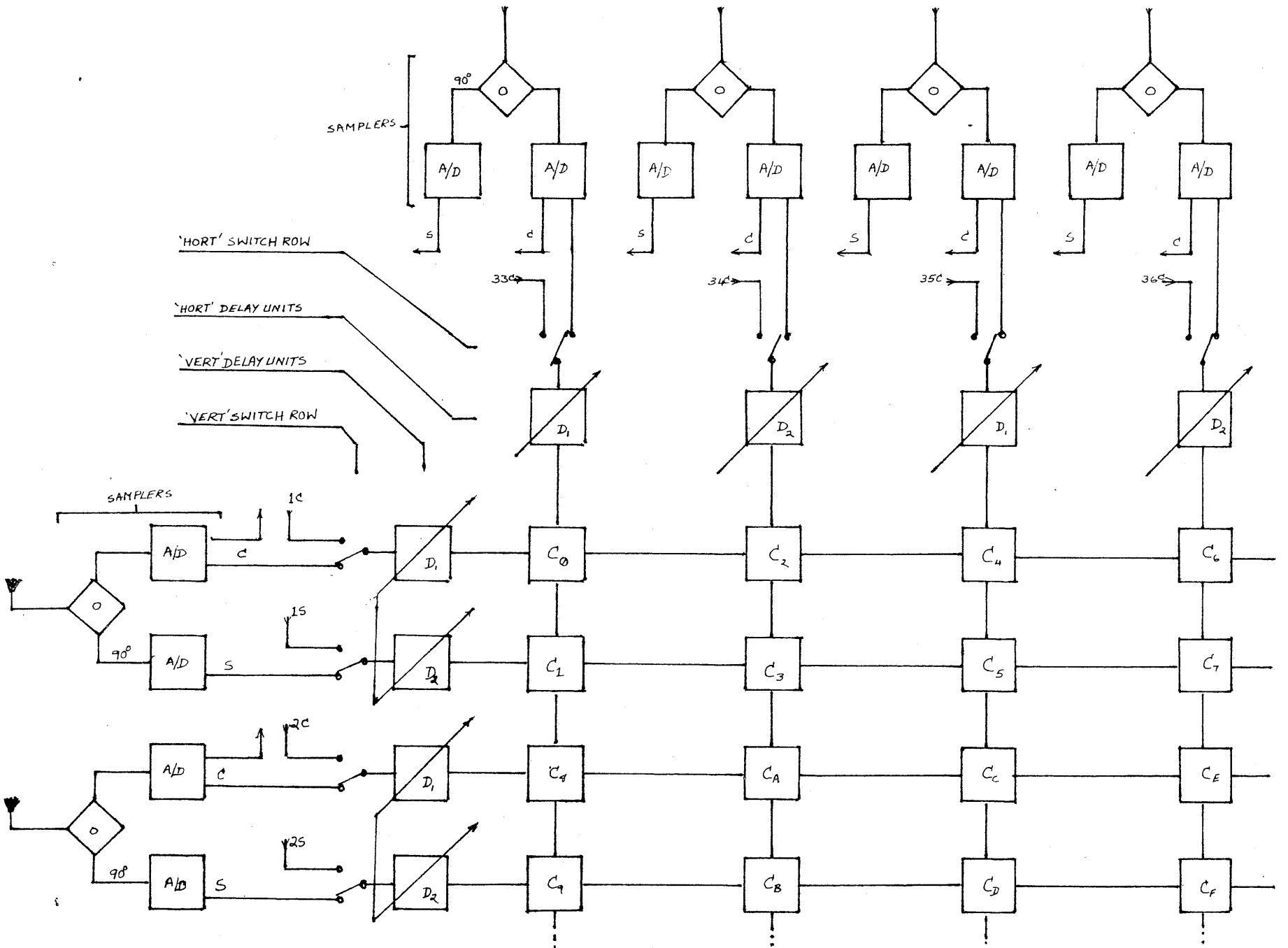
X^{+}	X^{-}	X
1	0	+1
0	0	0
0	1	-1

DELAY UNITS

The delay lines delay the two input bits X^{+} and X^{-} for the programmed number of clock intervals. The first phase switch is located at the delay line inputs and is used to synchronously demodulate the corresponding switch on the analogue end. It is called PS Walsh as the switch function will be a Walsh function. The second phase switch is located at one end of the two outputs of the delay line. It represents the synchronous modulation which is needed to get rid of the offset, in the correlators, provided for unidirectional counting.

The delays are individually programmable using the delay programming code.

Delay settings are stored on the delay line boards. All the delay line inputs are connected in parallel to the computer outputs. The same decoder is used to clock a delay setting into


SAMPLERS
90°
A/D
S
C
33C
34C
35C
36C
'HORT' SWITCH ROW
'HORT' DELAY UNITS
'VERT' DELAY UNITS
'VERT' SWITCH ROW
D1
D2
1C
1S
2C
2S
C0
C1
C2
C3
C4
C5
C6
C7
C8
C9
CA
CB
CC
CD
CE
CF

a specific delay line and to enable correlator outputs.

CORRELATORS

The correlators multiply outputs of the delay lines and integrate them over a certain period of time.

Two custom made chips VLA 1 and VLA2 constitute the heart of the correlators and are designed to perform two bit three level correlation.

The VLA 1 performs the multiplication and VLA 2 the addition.

Actual signal level	Symbolic notation	+ bit	- bit
Signal > +Vref	+1	1	0
-Vref < Signal < +Vref	0	0	0
Signal < -Vref	-1	0	1

The VLA 1 contain basically a multiplication logic and the VLA 2 is a 14 bit unidirectional counter.

Three level approach was chosen for it gives a good compromise between complexity of hardware and signal to noise ratio.

An appropriate multiplication table for the purpose is shown.

Output of delay line A: $X^{+}a$, $X^{-}a$, Xa

Output of delay line B: $X^{+}b$, $X^{-}b$, Xb

Xa	Xb		
	+1	0	-1
+1	+1	0	-1
0	0	0	0
-1	-1	0	+1

In the present correlator system the multiplication table is modified according to the table below.

(Xa)	(Xb)		
	+1 (10)	0 (00)	-1 (01)
+1 (10)	add 2	add 1	add 0
0 (00)	add 1	add 1	add 1
-1 (01)	add 0	add 1	add 2

The modification in the table is seen to be the addition of an offset of 1 to every product. The reason for this is that the VLA 2 consists of unidirectional counters only. The offset thus allows the counter to count up only and not down,which would be

necessary if there were to be a -1 output. However for correct integration, the data should be stripped of this offset before the computer reads it. This is done by using a concept called Phase switching, where data bits from the 'vert' delay outputs are periodically inverted and a corresponding inversion occurs to the data at the correlator outputs. One phase switch is included at one of the two delay line outputs. Another is present at the correlator output. An inversion at the delay line output is accompanied by an inversion in the microprocessors sign bit. When it accumulates the correlator outputs. The offset thus gets counted up in one switch interval and down in the other while only the information gets accumulated.

CENTRAL OUTPUT COLLECTOR

The central output collector interfaces the correlator output to the computer. The computer selects and reads all the correlators in sequence through the data collector. It serves the purpose of collecting and holding the correlator output data for the computer to read.

In an integration interval the correlators perform the integration after which the update causes an interrupt. Then the data in all 16 correlators of all 64 boards are sequentially read by the computer. The computer does not read directly from them. The update causes the correlator data to be outputed to intermediate data collectors (one for each 8 correlator rows).

And finally data stored in these intermediate storage are outputed to a central output collector through hardwired circuits. The computer then reads data from this collector.

The selection of correlator cards is done using a 6 : 64 decoder circuit comprising of two stages of 3 : 8 decoders. The first stage selects the row of cards to be read and the second stage which has eight 3 : 8 decoders, one for each row selects individual correlator cards on each row. Once a correlator card has been selected additional hardware allows the output data from every one of the 16 correlator (VLA 2) present on each card to be read sequentially into the collector.

This data collection process is performed for all the 64 cards once every update pulse occurs and data is stored in the central output collector. The computer then reads data from the central output collector before continuing the post integration.

CONTROLLER

a) It is the interface between the computer output and the inputs of the correlators, delays and samplers.

b) It provides the necessary timing signals and programming information to the system. c) It provides the necessary signals for the computer to read the correlator outputs.

The correlators and the delay lines need a clock, a phase switch signal and a stop switch signal at the end of each integration time. They are provided by the controller. The phase switch signal has a phase switch period of 10.92 ms.

The three phase switch signals are :

PHASE (CX) - Switches sign bit of the microprocessors.

PHASE (SQ) - Switches modulators at delay line outputs.

PHASE (Walsh) - Wired separetely to each delay line input. Orthogonal phase switch patterns (Walsh functions) can be provided for the delay line.

MODE OF OPERATION AND TIMING

The system is designed to operate with high time resolutions, therefore integration intervals have to be contiguous. This requires that different levels of operations such as - programming, system configuration, delays, integration, transfer of data, etc, have to run simultaneously. To meet this demand the microprocessors controlling the correlators need to have two seperate register sets. One for integration and the other for readout. This is controlled by integration bank select (IBS) signal which alternates between integration intervals. The system has to be programmable without immediately affecting current operations. The information has to be presorted and activated by an internally generated command (Activate signal) This signal is not only used internally to activate a new system configuration and new delays. It also controls external, intermediate memories where information is used to steer the antenna arrays, the first LO synthesized (observing) frequency etc, precisely between integration intervals.

To avoid integration of transient signals after a change in configuration, the delay outputs are reset by a blanking signal at the beginning of an integration interval - every 10.92 ms or every integration interval input. It is estimated that the longest transient interval occurs after steering the antenna array and changing the delays, an interval of approximately 20 micro seconds.

The following timing diagram shows the beginning of integration intervals where the configuration has to be changed after the second integration interval.

GROUP A

It consists of three fixed timing patterns synchronous to the basic timing pattern 2^{16} / 12 MHz = 5.46 ms.

UPDATE SIGNAL PULSE

Update signal pulse loads the state of the preintegrator counter into the shift register and resets the counter after that interrupts the microprocessors, which in turn reads all the shift registers and accumulates them into the 16 bit registers. The IBS signal determines which of the two register sets (integration bank 0 or 1) has to be used with a positive or negative sign.

WALSH SEQUENCES

Walsh sequences are produced in a separate generator depending on the system configuration(PB, FBNS, FBEW) clocked by the basic timing pattern. They control the inversion switch in the second LO inputs to the receivers and in the outputs of the sampler units.

BLANKING SIGNALS

To simplify the blanking concept a blanking interval is sent every 5.5 ms, synchronous to the basic timing pattern. This assures that the positive and negative phases are equally shortened and any possible transient phase is covered. The blanking interval is (256 / 12 micro seconds = 21.3 micro seconds) Therefore it only reduces the maximum possible integration interval by approximately 0.4%. This is in addition to a 0.1% reduction due to the gaps between the update intervals.

GROUP B

These consist of signals from the computer that affect the timing of the signals in group C

INITIALIZE

Initialize causes the system to generate a reset and activate pulse at the next clock of the basic timing pattern (within < 5.5 ms). It also causes the Phase and the IBS signal to go or to stay low. The reset pulse goes directly to the microprocessors directing it to clear all the accumulators. The Activate pulse brings the system configuration A (programmed anytime before the initialize signal) into effect. The phase signal will now regulary change with every clock of the basic timing pattern. The IBS signal stays low during the integration

interval. The shortest interval is choosen. At the end of each integration interval the system generates an interrupt signal telling the computer to read the data from the previous integration interval in the bank 0. The IBS signal changes the second integration interval which immediately starts accumulating in bank 1.

MODIFY

In order to run the third integration interval with a different configuration, the modify signal has to be sent during the second integration interval. This causes the system to generate an activate pulse at the end of the second integration interval which brings configuration B into effect, which was previously programmed sometime between start of the first integration interval and the modify signal.

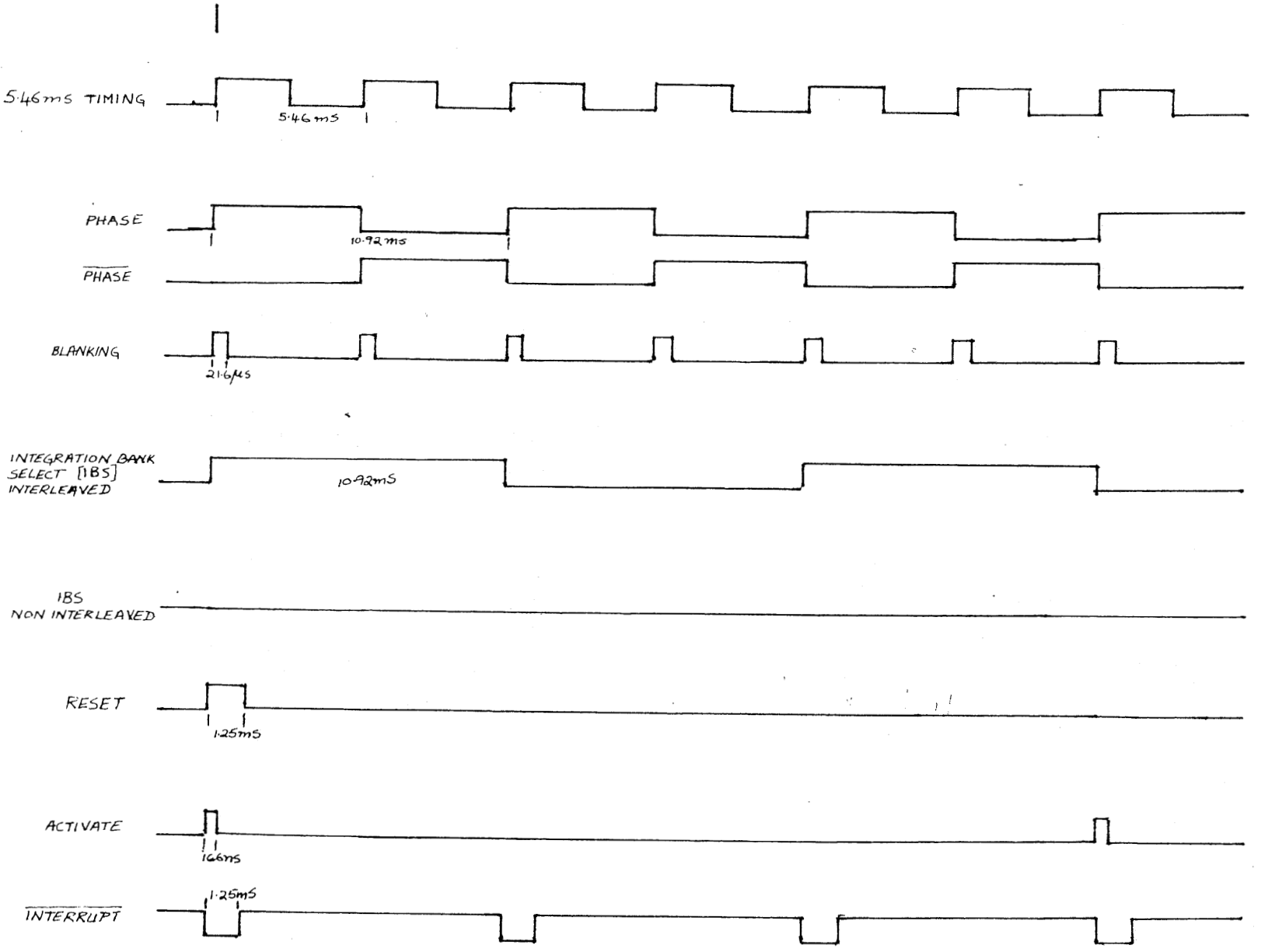
Reading the data from bank 0 or 1 always clears the accumulators. Therefore the reset pulse is only required at the beginning of the integration signals.

INTERLEAVED / NON-INTERLEAVED MODE

The mode of operation described is called interleaved. It requires a relatively fast data transfer to the computer, which for short integration intervals can only be acheived by direct

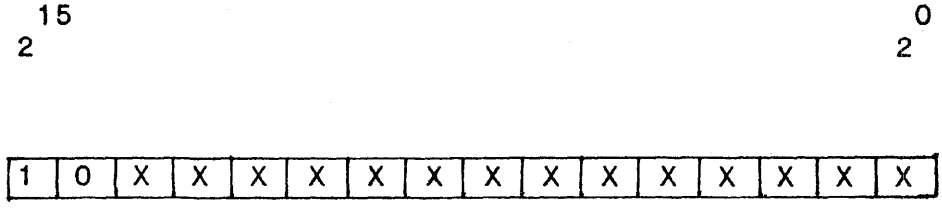
memory access (DMA).

To observe stationary radiating objects where high time-resolution is not required, in a simpler mode, the non-interleaved mode is used. To operate this mode, a special initialize signal is sent which causes the IBS signal to stay high after the first integration interval until after the next initialize signal is sent. No further interrupts are sent to the computer , therefore the computer can read the data from bank 0 at any desired speed.

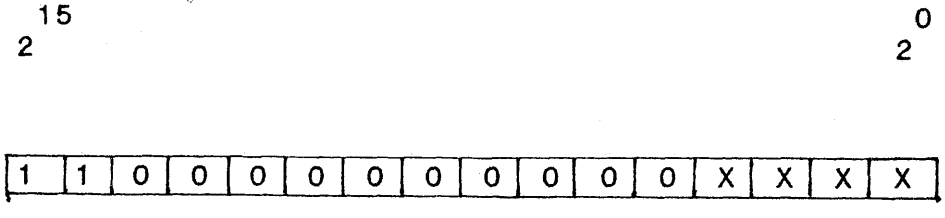

5·46ms TIMING
5·46ms
PHASE
10·92ms
PHASE
BLANKING
21·6µs
INTEGRATION BANK SELECT [IBS] INTERLEAVED
10·92mS
IBS NON INTERLEAVED
RESET
1·25mS
ACTIVATE
166ns
1·25mS
INTERRUPT

CODES

SYSTEM CONFIGURATION CODE



MODIFY/RESET CODE



THE EXISTING SYSTEM

BOARD VI A - Part(a)

Data lines which are connected to this board are numbered from 61 to 77. The data bits comes in from the input/output panel. DA is a signal which also comes in from the input/output panel. This signal is delayed and routed to enable the three line to eight line decoder (74LS138) to allow enough time for bits on the lines 61 to 76 to settle to their correct values, at the inputs of the octal D flip-flop (74LS374).

The working of the boards VI A - Part (b), VI A - Part (c) and VI B boards depends mainly on the programming and status words entered in the System configuration code. A list of all the codes appear in the introduction. It is observed that lines 75 and 76 (2^{15} and 2^{16}) play an extremely important part in the in the implementation of the various codes.

Since the output lines of the 74LS138 (Chip C3) are active low, the outputs from this chip - Y0 to Y3 are inverted outputs. Y3 goes noninverted to Board VI A - Part (b).

The delay programming code which is not handled in VI A and B are channelled to the delay control from the 74LS374 latch inputs.

When activated these circuits output a modify/reset enable bit or clocks Test mode selection data to the Sampler Controller.

If any one of the data inputs (2^{9} to 2^{13}) and Y3 are 1 then neither of the outputs are activated.

When all of the above mentioned data inputs are 0 then the 2^{8} input decides which of the two outputs to activate - A 0 value for 2^{8} enables the a modify/reset output and a 1 enables the test mode selection output, which in turn, outputs test mode selection data to sampler controller through a 74LS374 latch.

When a new system configuration code is to be sent, the 2^{14} and 2^{15} (pin no. 75 and 76) are entered with 0 and 1 respectively. This enables the rest of the data from pins 61 to 74 to be latched to the appropriate points of the various circuits. The latches being chips G4 and H4 on VI A - Part (a).

When both pins 75 and 76 (2^{14} and 2^{15}) are made 1 and pins 69 to 74 (2^{8} to 2^{13}) are made 0 then the resultant at Y3 (Chip C3 - 74LS138) is an active low signal and the 0's at pins 69 to 74 (2^{8} to 2^{13}) generate the modify/reset enable signal which in turn activates appropriate signals in board VI B.

Pins 61 to 68 (2^{4} to 2^{7}) are also 0's and are gated to the Sampler control (Board VI B - Part (f)).

BOARD VI B - Part (a)

The programmable integration interval timer sets the timing interval for the integration taking place in the correlator.

A rising edge at clock input of Chip K4 outputs the integration interval data on lines 91 to 94. The 74138's (Chip J4 and K3) are so connected that Chip J4 is activated for all integration values from 0000 to 0111.

The 'Clear integration interval counter' - line X should be at 0 for 74LS138's to be enabled. Both X and $\overline{rc}$ (ripple carry out pin 15) of Chip G1 are at 1 during counting. This disables the load inputs to the 74169's and enables count operation to go on.

The actual integration interval (Z) is decoded from the integration interval code (n), using the formula

$$Z = (2^{n+1} - 1) \times 10.92 \text{ ms.}$$

where n = 0, 1, 2, ...,14.

Thus the smallest integration interval is 10.92 ms. For non zero values of n the counters count down the decoded integration interval with the 5.46 ms clock.

At terminal count when chips G1-G4 reach 0000 the $\overline{rc}$ output pin 15 of G1 disables the counters and chip F2 the flip-flop converts the negative going $\overline{rc}$ (ripple carry-out pin 15) to a

positive pulse after sufficient delay (5.46 ms). This signal is called integration interval elapsed (IIE).

Should a modify signal occur between two IIE's, the line X goes low disabling the counters from counting and loading the new integration interval into the counters from the adder outputs. At the occurence of the $\overline{rc}$ output the IIE is signalled and the count down process for the new integration interval begins.

When no modify signal occurs the ripple carry output reloads the unchanged integration interval from the adder output into the counters and when rc goes high count is enabled.

BOARD VI B - Part (b)

A basic clock frequency of 12 MHz clocks the 4 counter cascade (74LS169 - Chips L1 - L4).

The basic integration clock is tapped at pin 11 of chip L1 (the MSB of cascade). This pin 11 corresponds to the divide by 2^{16} output which yields a 5.46 ms clock.

As the multiplication and accumulation involved in the correlation involves repeated addition by an offset value of 1, a counter is necessary whose value is incremented by 0,1 or 2 depending on the product of 2 bits.

This preintegration counter has a maximum capacity of 14

bits. If a worse case is imagined where 2 is added to the counter value, the counter would overflow at the 2^{14} clock pulse.

Therefore after every 2^{13} th clock pulse, the value of the counter must be stored, before the 2^{14} th clock pulse occurs an overflow would occur. This value is moved into a string of shift registers and the counters are reset with an update pulse of width 2 x 83.3 ns = 166.6 ns. This pulse also causes an interrupt to the microprocessor which the contains the integrated data and then reads the 12 bit shift register whuch holds the result of an integration over an interval and further integrates them into 16 bit values. and accumulates them into 16 bit registers.

BOARD VI B - Part (c)

A 48 MHz oscillator output is available from a 1:1 transformer. The oscillator is located on the input output panel.

The 48 MHz output is used to generate 12 MHz clocks which clock the various circuits on VI A and VI B and also on the various controller boards.

This is done by dividing the 48 MHZ into four, 12 MHz signals. Now each 12 MHZ clock is 90 degrees out of phase with respect to each other, resulting in a 4 phase clock.

The output of the transformer is fed to Chip 03 (HC 10116) and later to ECL D-flip-flops HC 10176 (Chip 02) These pulses

are then converted from ECL levels to TTL levels with the help of Chip O1 (MC 10125). After this four JK flip-flops which are interconnected as in the circuit and generate the clocks in four phases.

Further chip N3 (MC 10124) converts TTL levels to ECL levels, this conversion is necessary as clocks in ECL levels are also required for the samplers, delays and correlators.

BOARD VI B - Part (d)

The three key bits that control the operation of the correlator system are the initialize (2^0), the interleaved/noninterleaved (2^1) and the reset (2^2).

This circuit receives these latched bits and generates appropriate signals to control the mode of functioning of the correlator. These signals are the interrupt, the IBS, the reset and the activate.

A change in system configuration made in between two integration intervals is implimented by the system only at the end of the current integration interval. The integration interval elapsed signal from VI B Part (a) (which signals the end of every integration interval) is therefore used to actually generate appropriate signals for the bits 2^0, 2^1 and 2^2. These bits are latched into the circuit whenever there is a change in modify/reset code through the m/r enable. The difference

between initialize signal and reset signal is that initialize causes reset, activate to be generated and causes IBS to go low before integration interval elapsed occurs. When reset is 1 integration elapsed signal is generated.

$2^0 - 2^2$ of m/r	IBS goes low activate & reset generated	interrupt generated & IBS switched
Initialize = 1	generated immediately	generated by IIE 1 & all other subsequent IIE'S
noninterleaved = 1	generated by IIE 1	generated by IIE 2 only
reset = 1	generated by IIE 1	generated by IIE 2 &-by all subsequent IIE's

BOARD VI B - Part (e)

The smallest integration interval is 10.92 ms. The phase switch inverts once every 10.92 ms, and phase switching takes place every 5.46 ms.

Any change in system configuration may give rise to

transient signals and care must be taken to see that these signals are not integrated. Again transient signals may also arise after every phase inversion which occurs every 5.46 ms as both + ve and - ve phases must be symmetrically blanked so that the amount of data accumulated (in the microprocessor) during +ve and -ve phases are the same. the 2 phases.

To avoid such an integration of spurious signals, the blanking pulse is generated every 5.46 ms which zeros the delay outputs so that (although the integration interval clock is on) the integration does not take place during this time. As the longest interval for which transients can occur is about 20 micro seconds, in the circuit the blank pulse is 21.6 micro seconds long.

The basic 5.46 ms pulse clocks a high to the output which through a counter cascade selects the blanking interval forces down the high after 21.6 micro seconds (by a divide by 8 configuration 12 MHz / 2^8). The blanking pulse therefore lasts 21.6 micro seconds and occurs every 5.46 ms.

A pulse synchroniser circuit synchronises the programable delays input and Clr.rdy input with the basic 12 MHz clock.

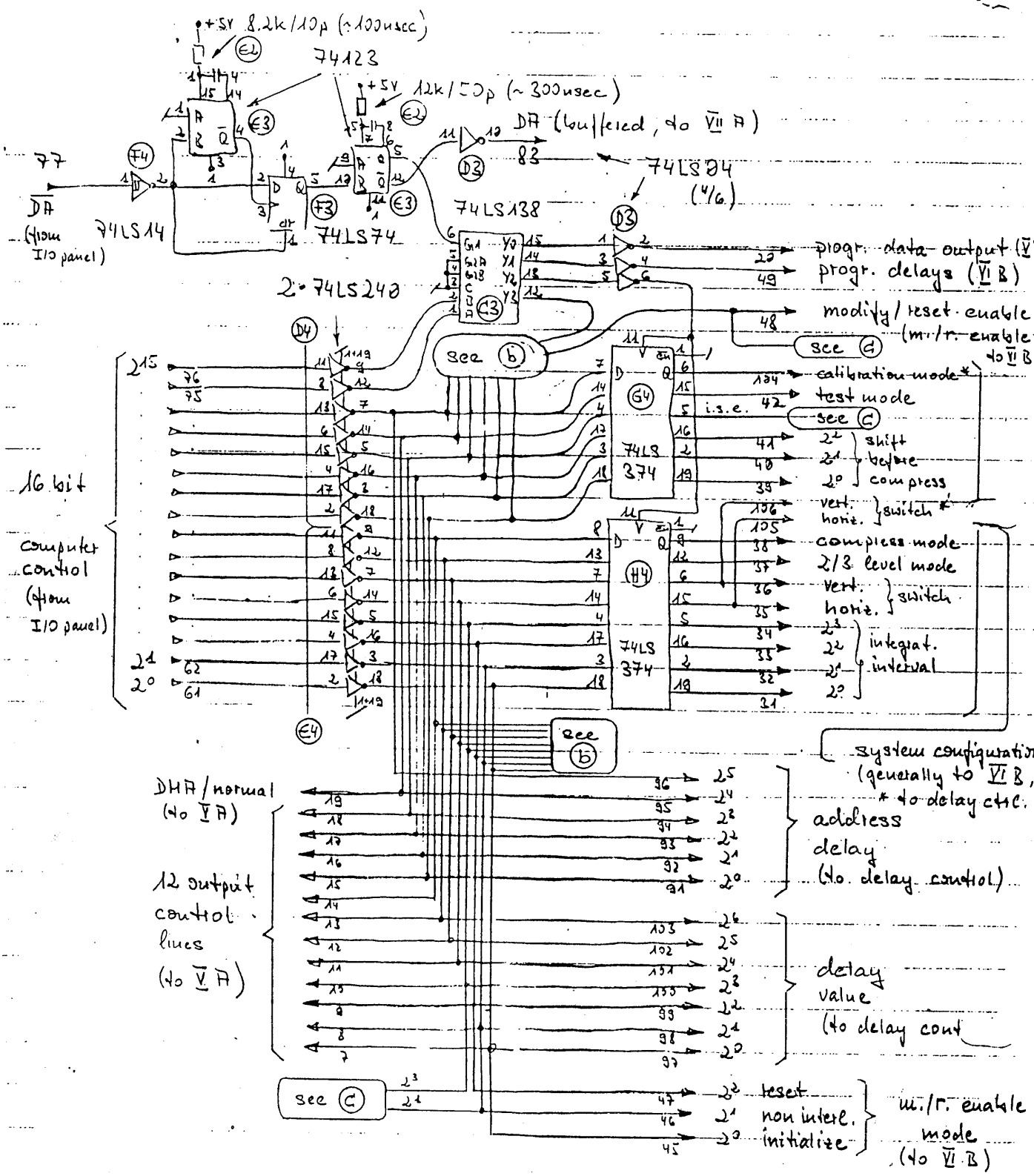
BOARD VI B - Part (f)

Bits 2^4 , 2^5 , 2^6 and 2^{12} of system configuration code are

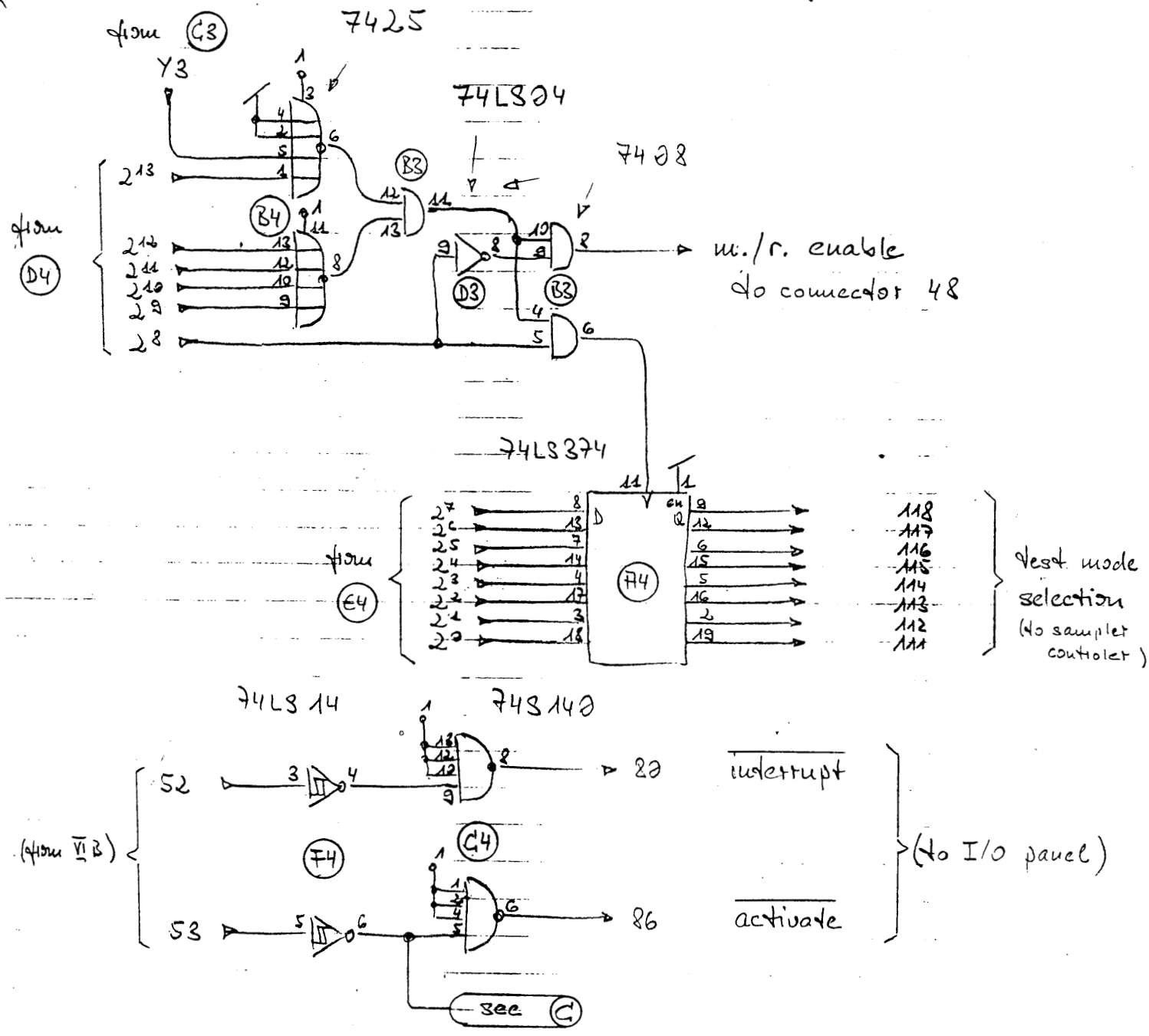
channelled for sampler ane delay control.

The outputs to the sampler control are 2^4, 2^5, 2^6 and 2^{12} which are latched out only on the arrival of the ACTINT signal from VI B - Part (d). 2^4 and 2^5 are also output to the delay control. In addition to this the delay control also receives an AND'ed output of 2^4 and 2^5 which specifies whether the system should work in fan beam or pencil beam mode.

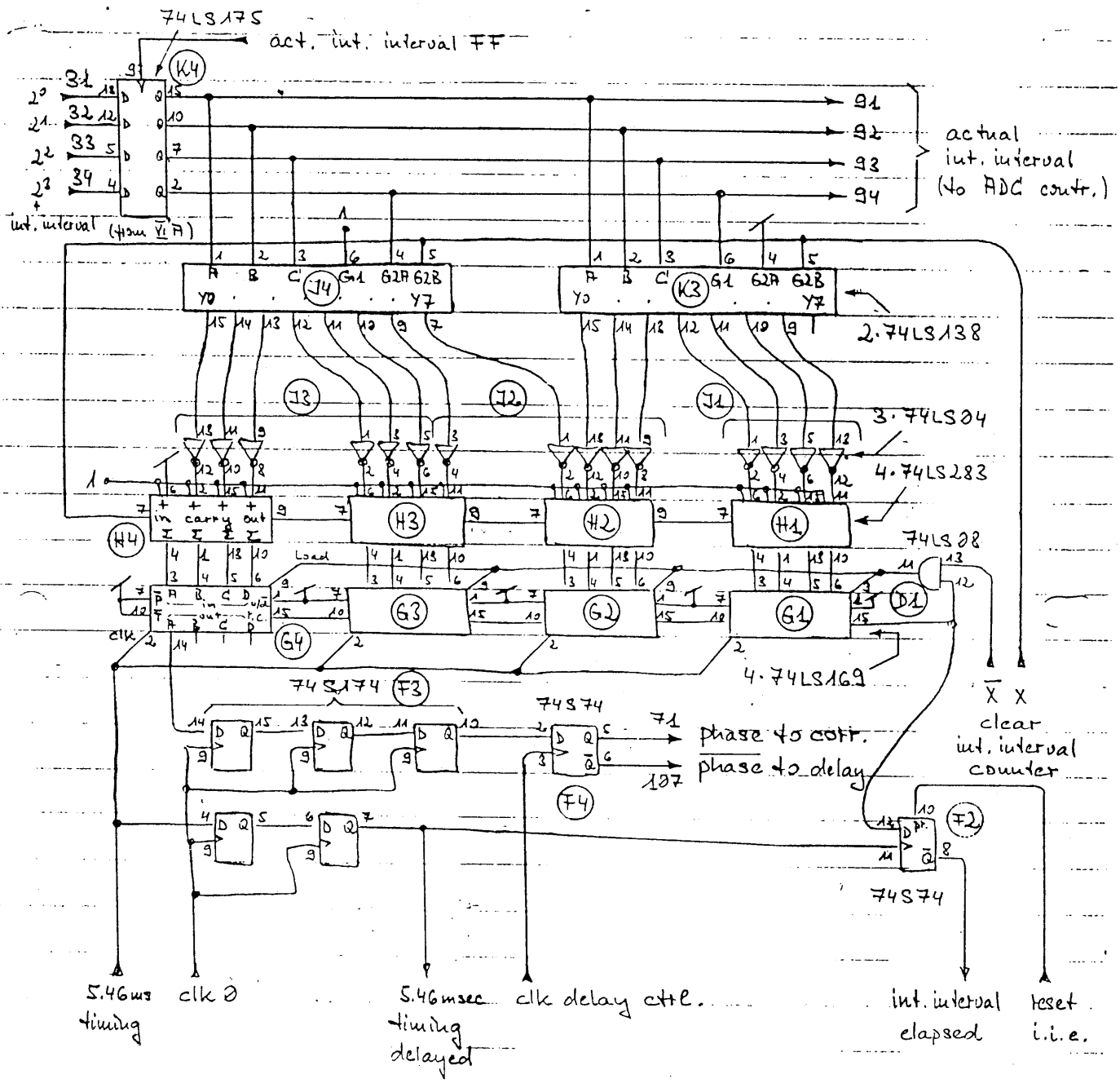
board VI A : computer control signal buffering and decoding (a)



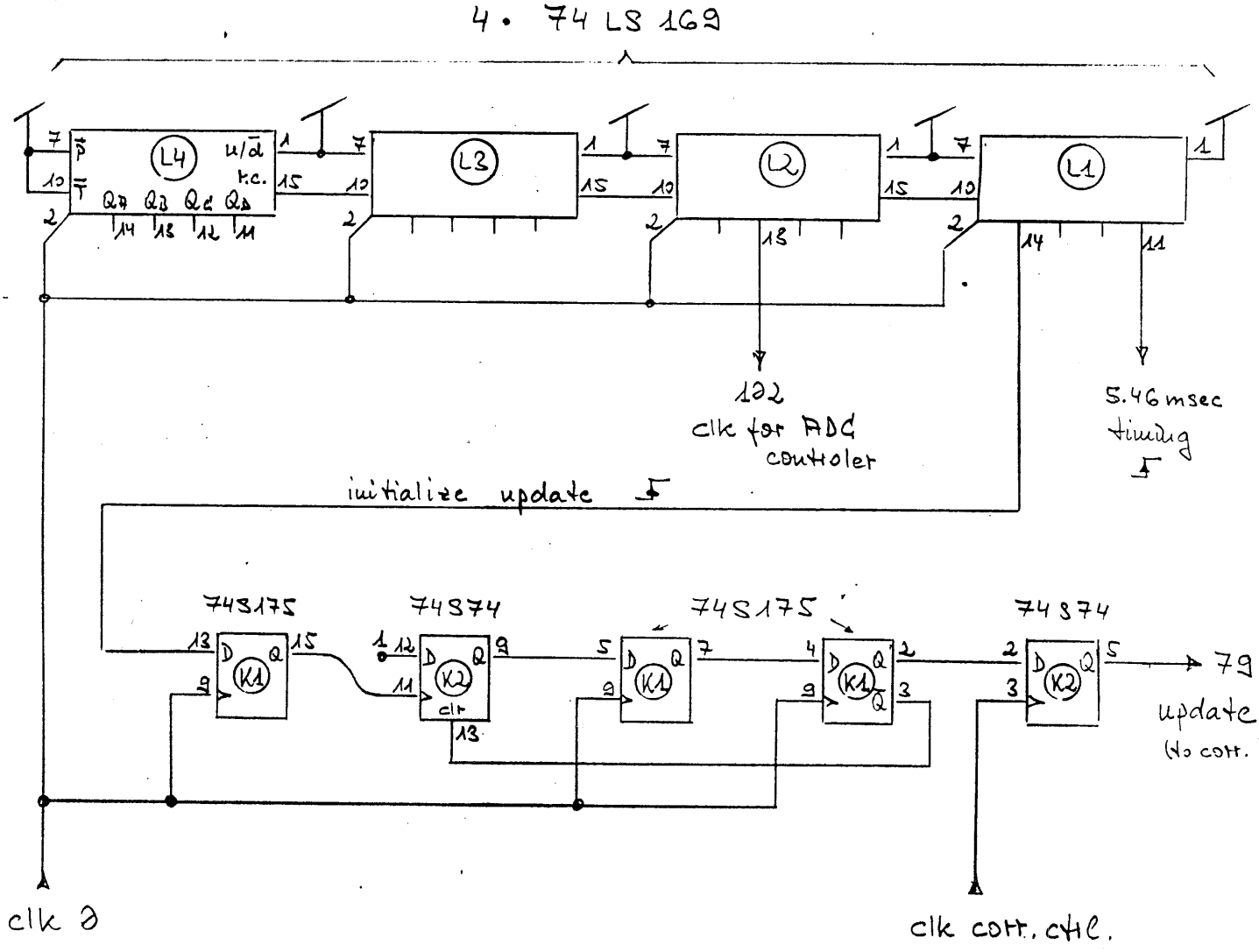
board VI 7 : computer control signal buffering and decoding (b)



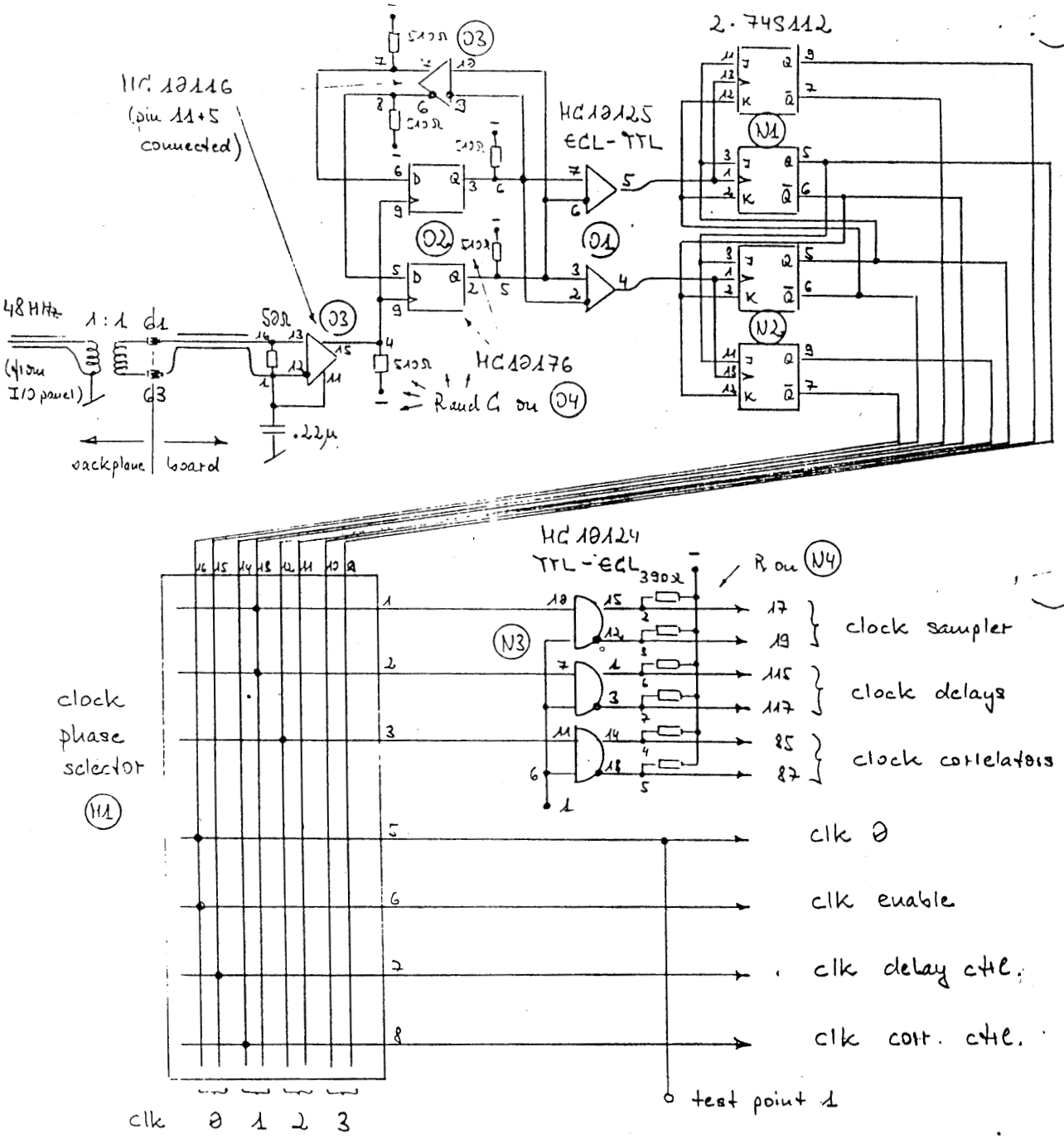
board VI B : programmable integration interval timer

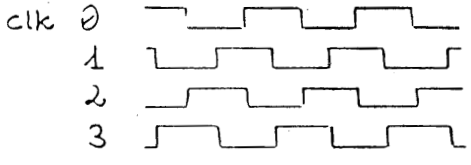


board VI B : divider chain
and update generation

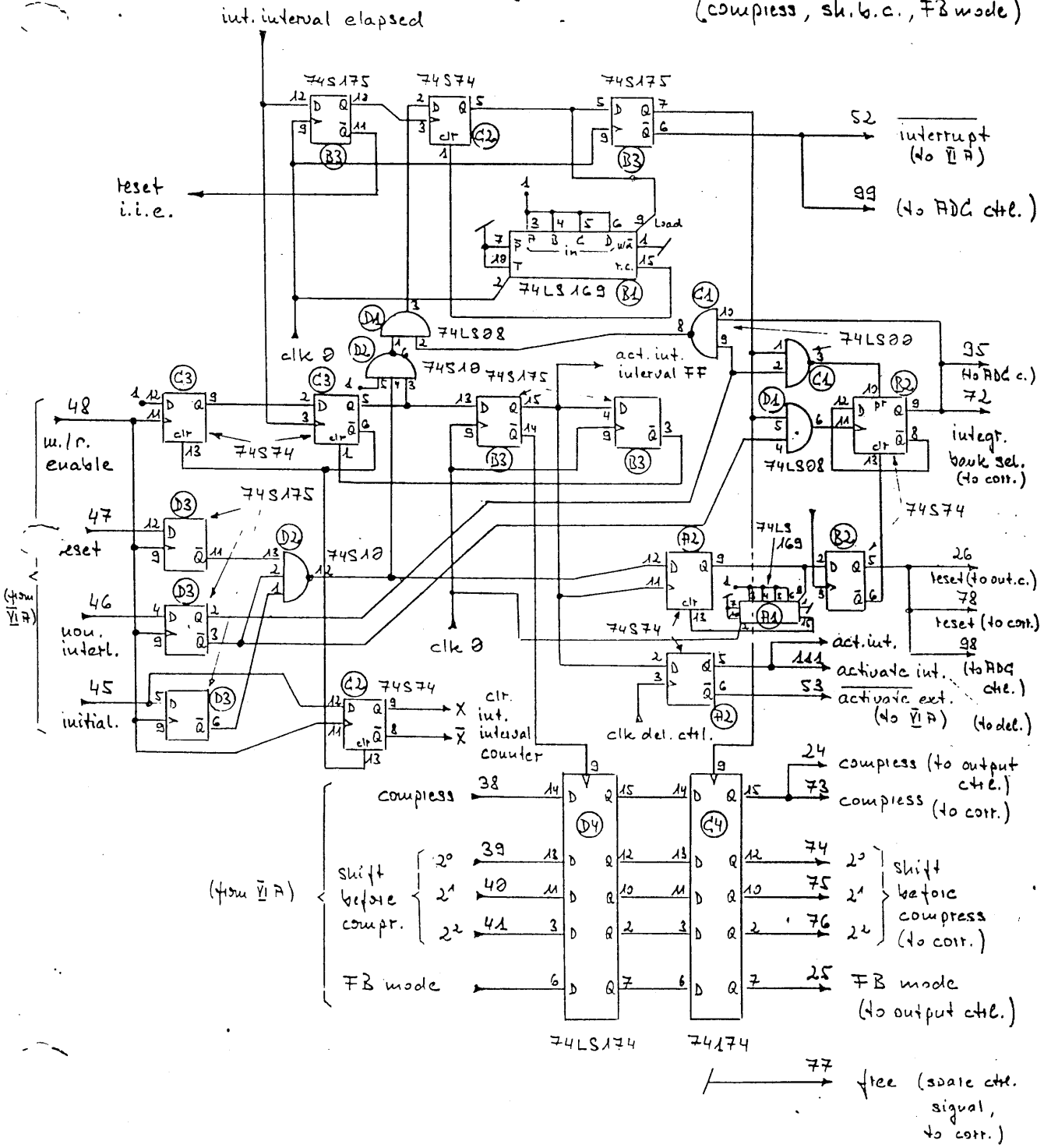


board VI B : 4 phase clock generator and clock phase selector

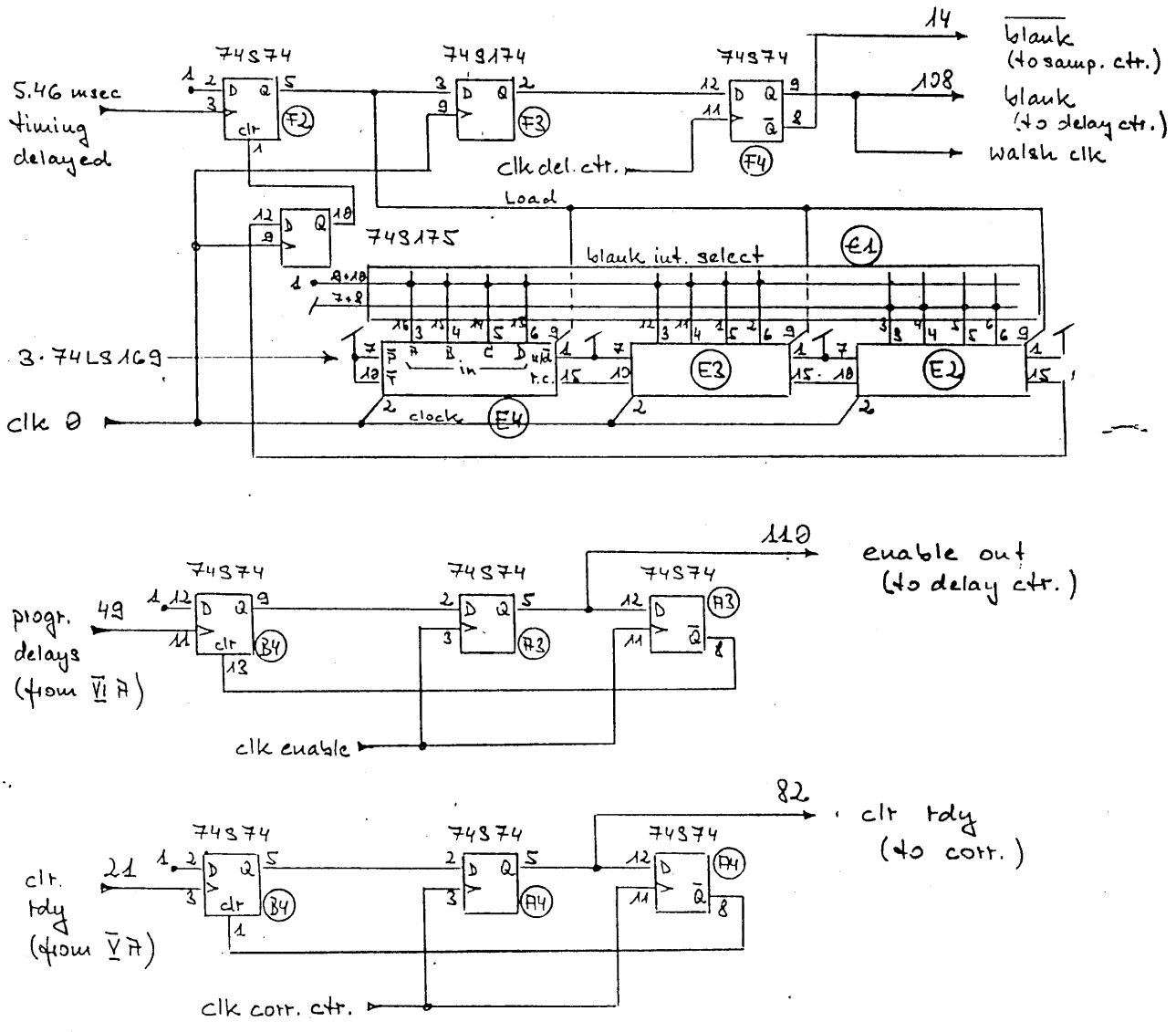




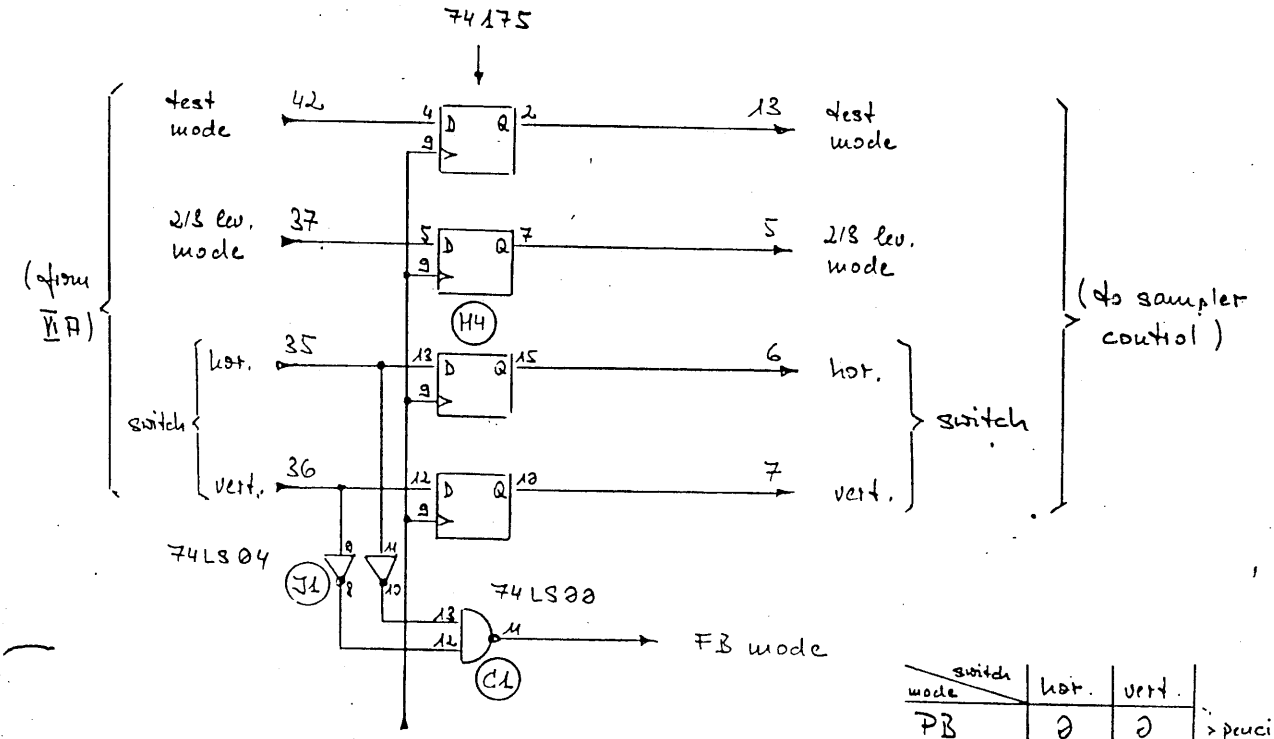
board VI B : generation of interrupt, int. bank sel., reset, activate and delaying of contr. inform. to correlator + outp.c. (compress, sh.b.c., FB mode)



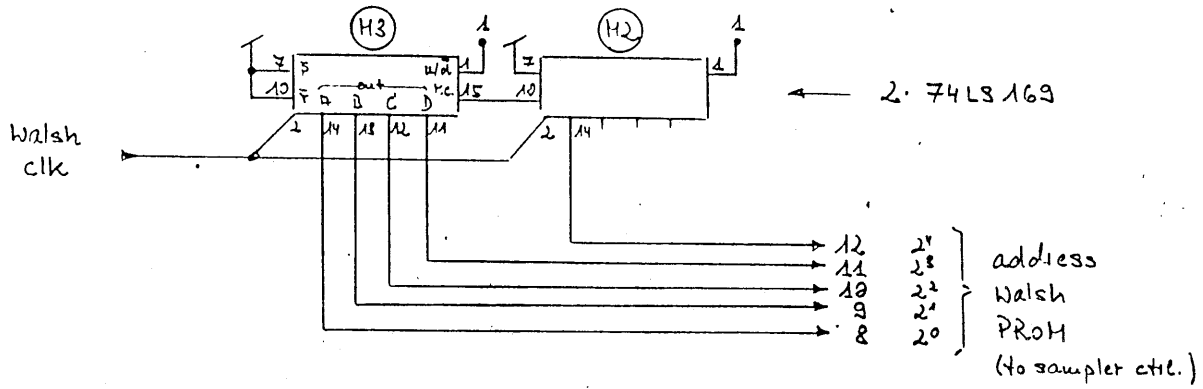
board VI B : generation of blank and pulse synchronizer for enable out and clr rdy



board VI B : second storage FF (act.) for sampler ctrl. information and generation of Walsh-PROM address

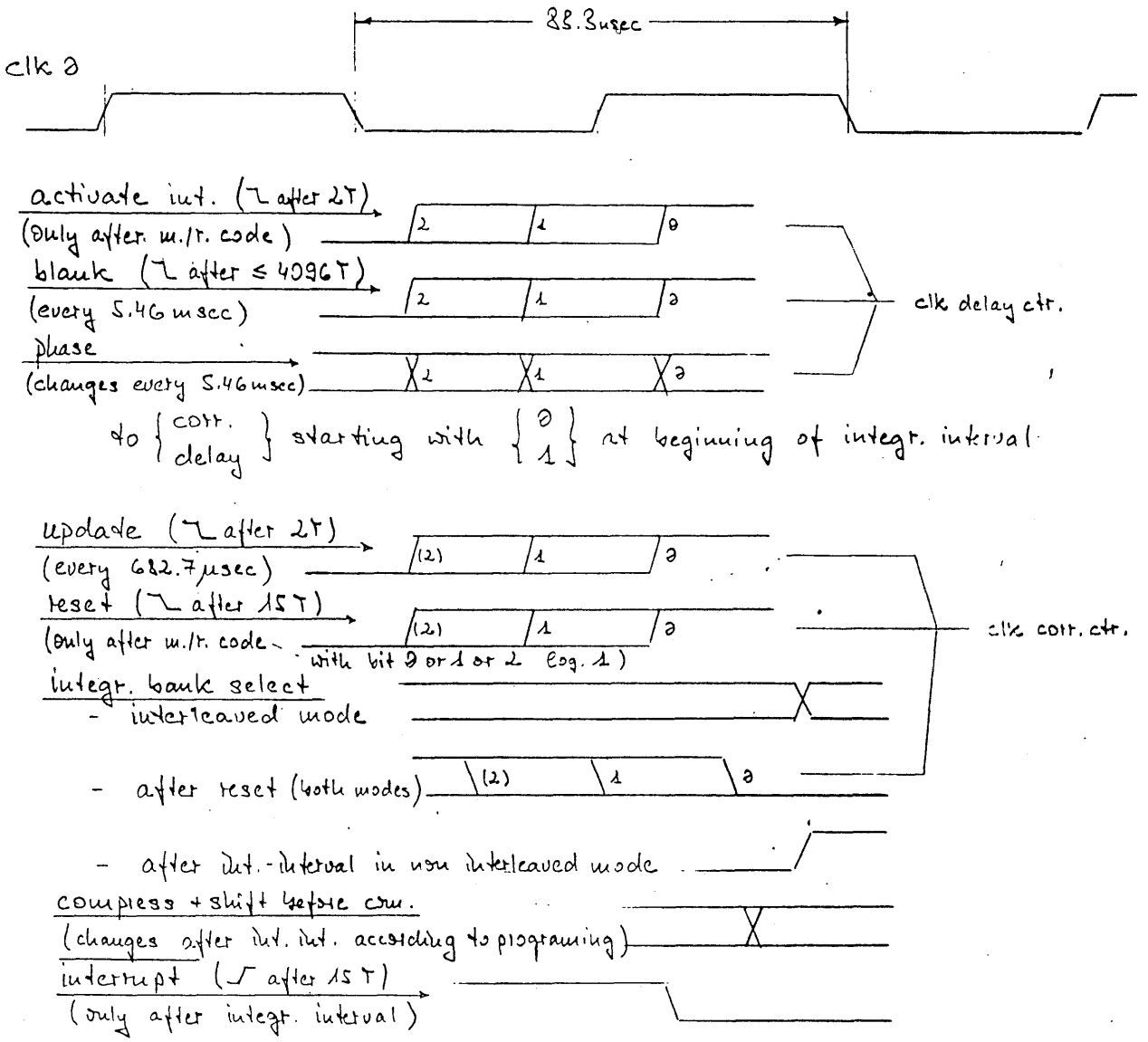


switch / mode	hor.	vert.	
PB	0	0	> pencil beam
FB NS	1	0	> fan beam
FB EW	0	1	> fan beam



board VI B : timing

shows transitions at gap between integration intervals, actual transition times depend on clock phase selection :



THE PROPOSED SYSTEM

The system clock operates at a set frequency of 12 MHz. The generation of this clock frequency is done by a 48 MHz local oscillator, located in the correlator unit.

This signal is first converted into a proper square wave by using an operational amplifier comparator chip - the NE521. The output is then fed to a divide by four arrangement called the four phase clock generator, which basically consists of a chain of three, hex D flip-flops (74F174).

As four phases of the resultant 12 MHz clock is required, the flip-flop chain is tapped at 4 output points and the driving capability of the four phase signals are enhanced by a 74F365 line driver.

As the sampler, delay and correlator boards contain ECL chips, the four clock phases are level shifted from TTL to ECL levels using the MC10124 - TTL to ECL interface chips.

As a set of clock phases is required for the proposed system, which operates at TTL levels, one set of clock phases are thus retained, at TTL levels.

The basic integration interval of the correlation process is 10.92 ms. The 5.46 ms waveform is generated from Clk 0 using a

divide by 2^{16} circuit as shown comprising of four 74LS169 chips. The 5.46 ms timing is obtained at the MSB of this cascade.

The Update signal occurs once every 2^{13} clock 0 cycles that is once every 682 micro seconds. Therefore the Update signal is tapped at the 13th output of the divider chain and is delayed by 166 ns seconds before it is synchronised with Clk Correlator Control and sent to the correlator system. This delay is introduced using a chain of 74S175 and 74S74 flip-flops.

The 80186 has three functions:-

a) Acquires data from the correlator matrix.

b) Programmes the correlator/delay system through the 8088 system.

c) For power system monitoring.

The outputing of the SCC (system configuration code) and the MRC (modify/reset code) from the 80186 to the 8088 is accomplished through two programmable peripheral interface chips (8255A). Ports A and B in both chips are programmed by the 80186 software to operate in mode 1 (strobed output). In this mode the OBF pins of the 8255A go low as soon as the data is written into its port. The OBFb of the MRC 8255A interrupts the 8088 through the 8088's INTR pin. This ensures that both SCC and MRC have been transfered entirely before the interrupt to the 8088 is actually made.

In the interrupt service routine the 8088 reads the four ports by seperately adressing four tri - state buffers (74241). After this it generates an $\overline{ACK}$ signal to clear the OBFb pin.

To ensure that the 8088 has received the codes, the 80186, after writing out all the codes, polls bit PC 1 of the MRC 8255A until it senses a logic 1 or a high bit. This indicates that the ACK signal has arrived and therefore the codes have been read. The 80186 software may be written so that it polls the PC 1 bit for only a predetermined period of time. Withen this time if the poll is unsuccessful the 80186 may write out the codes again.

An 8286 chip has been used as a parallel bi-directional bus driver for the 8088 data bus. The 8088 DEN is connected to the OE of the 8286 and eliminates bus contention and the DT/$\overline{R}$ (of the 8088) to the T (8286) determines the direction of data flow. T is sent low to receive data and is high if data is to be sent.

The 8282 I/O ports are used as address latches for the 8088. The OE pin is permanently at ground and the address is enabled into the 8282 using the $\overline{ALE}$ of the 8088 to the STB of the 8282. There are three in all, to latch the 20 bit address.

The 8254 select inputs are AD3 - AD0 and its chip select pin is enabled by an I/O device decoder circuit in accordance with the address mapping of the I/O devices, i.e. 0F00 being the decoder chip select combination and A3 - Ao enable the particular

I/O chip pin of the 74241 (tri state buffer) whose input is hard wired to 08h, the interrupt type. When the INTA signal is generated the interrupt type is read from which the interrupt pointer is calculated and using the CS and IP contents stored therein the interrupt service routine is acessed.

There are two interrupts in this sub system,

1) Interrupt 1 (INT1) to signify a change in system, modify/reset code.

2) Interrupt 2 (INT2) to indicate the occurance of an integration elapsed signal.

As the first is a level and the second is a pulse it was decided to use a 74LS74 (D flip-flop) with an associated circuitry which latches the interrupts (when either occurs) to the flip-flop output. The 74LS74 output therefore forms a 'Interrupt Word' which is read by the 8088 as soon as an interrupt occurs. The interrupt is identified (as INT1 or INT2) by the 8088 software. A 74LS241 - non inverting tri state buffer which is enabled by the 8088 using I/O addressing, to read the interrupt word.

The work of the circiut in VI B (a) is to handle the task of decoding and counting down the entire integration interval and then signalling an integration interval elapsed to the rest of the system. It was decided to replace this circuit with a combination of hardware and software. The hardware is the 8254 - timer chip, and it counts down the integration interval. The

signalling and decoding of the integration interval is done in the microprocessor itself in its software instructions. The software also handles the loading of the current integration interval value into counter 1 of the 8254.

The basic timing of the integration process is the 5.46 ms clock. This is therefore the clock input to the counter 1.

The D - type flip-flop at the gate of counter 1 has a power - on reset connection to it. This ensures that at the beginning of the operation counter 1 does not begin counting from any random number its count register might hold. Again, keeping the gate tied high would enable counting before the interrupt 1 occurs. This would disturb the entire system sequence of operation and its performance. The gate is at low level from the beginning of operation till the time the first Activate pulse is generated, i.e. - until the first set of System configuration and modify/reset codes are input. This pulse clocks the gate which enables the count. This counter is operated in mode 2, that is, it functions as a rate generator. The mode 2 is specified in the counters control register contents ,which is loaded into the 8254 at the beginning of operations.

The output pin is connected to the interrupt latch and to the interrupt enable.

Counter 2 of the 8254 generates the reset or interrupt pulses. The same count is loaded into the count register for

both signals as both have the same pulse width of 1.3 micro seconds. The closest pulse width obtainable to this using its 6 MHz clock is 1.44 micro seconds. The 6 MHz clock is obtained from the first output pin of the divider chain (in VI B (b)). The count loaded is 09h.

The counter operates in mode 1 and therefore functions as a programmable one-shot whose output pulse width is a product of the count and the clock's time period .

The gate input to this counter is an OR'ed output of the RESAND and INTRAND. This is because the same output pulse from the counter functions as two different signals. The reset is channelled to the output controller, the correlator and ADC controller. The negated reset serves to pull the IBS to 0 through a connection to the clear pin of the IBS flip-flop. The RESAND output goes high whenever there is an MRC change.

As the same output functions as two different signals at different times. A 74LS241 has been used to explicitly identify the pulse as a reset or an interrupt as the operation demands.

The output of counter 2 is input to two buffers (of the available eight) in the 74LS241 chip. Each is controlled by a separate enable pin. When the configuration requires a reset pulse to be output, the enable of the corresponding buffer is activated and simultaneously the buffer which channels the

interrupt pulse is disabled , and vice-versa . The reset has been used to enable one buffer and disable the other. Likewise the INTRAND output is always high for an interrupt signal to be generated and therefore used to enable the buffer for interrupt and disable the one for reset.

All signal generation in this subsystem is microprocessor controlled (by software). Whenever operation protocol demands, the reset, activate interrrupt and the IBS signal have to be directly generated by the software. One way to do this is to use two-input AND gates as separately addressable output devices. The I/O decoder enables the chosen AND gate . A high on a uniquely chosen data line produces a high output which either clocks the necessary flip-flops or enables the concerned gates to generate the necessary signals.

The activate signal signifies a change in the operating mode of the telescope to the various components of the digital system.

The pulse width of the activate signal is 166 ns. This has been retained in the proposed system along with the flip-flop circuit which generates it. Three D flip-flops are connected to constitute a shift register with the MSB flip-flop's $\overline{Q}$ is fed back to the clear input of the first. The activate is generated by the system whenever the initial bit in the modify/reset code is high or otherwise whenever there is a change in system configuration. The INITAND and the ACTAND which respectively signify the above conditions are both OR'ed before they clock the

activate generation. To ensure that the activate pulse is not shorter than 166 ns , the OR'ed output is AND'ed with CLK 0 before the AND output initiates the activate generation.

The ACTAND output goes high only after the occurence of the IIE signal (integration interval elapsed - which is sensed by the microprocessor) or when there is a modify signal. The INITAND output however, goes high immidiately after the modify/reset code has its 2^0 bit high. The activate generation in this case does not wait for the IIE to occur. The IBS (integration bank select) is cleared to 0 at the advent of every reset signal and toggles at the occurence of every interrupt signal. This is achieved by using a D-flip-flop (called the IBS flip-flop) connected in toggle mode, clocked by the by the interrupt signal and cleared by the reset signal.

The blank signal should occur a few nano seconds after the 5.46 ms clock's rising edge. To ensure this and keeping in mind the 21.3 micro second pulse width of the blanking pulse (< 5.43 ms) itself, it was decided to AND the 5.46 ms delayed clock with a 6 MHz clock (from the divider chain) at the clock input of the 8254's third counter.

As the gate pulse to the counter is specified to be of a minimum of 150 nano seconds, a 166 nano second gate pulse is generated using a CLK 0 and three flip-flops (7474 type). This flip-flop chain has an AND'ed clock input of CLK 0 and the 5.46 ms delayed signal. This ensures that the counter is enabled

through the gate, every 5.46 ms. The 5.46ms delayed clock is derived from two 7474 flip-flops connected in 2 bit shift register mode. A count of 128 (binary) is loaded into the third counter's count register during initilization and remains unchanged throughtout the system operation.

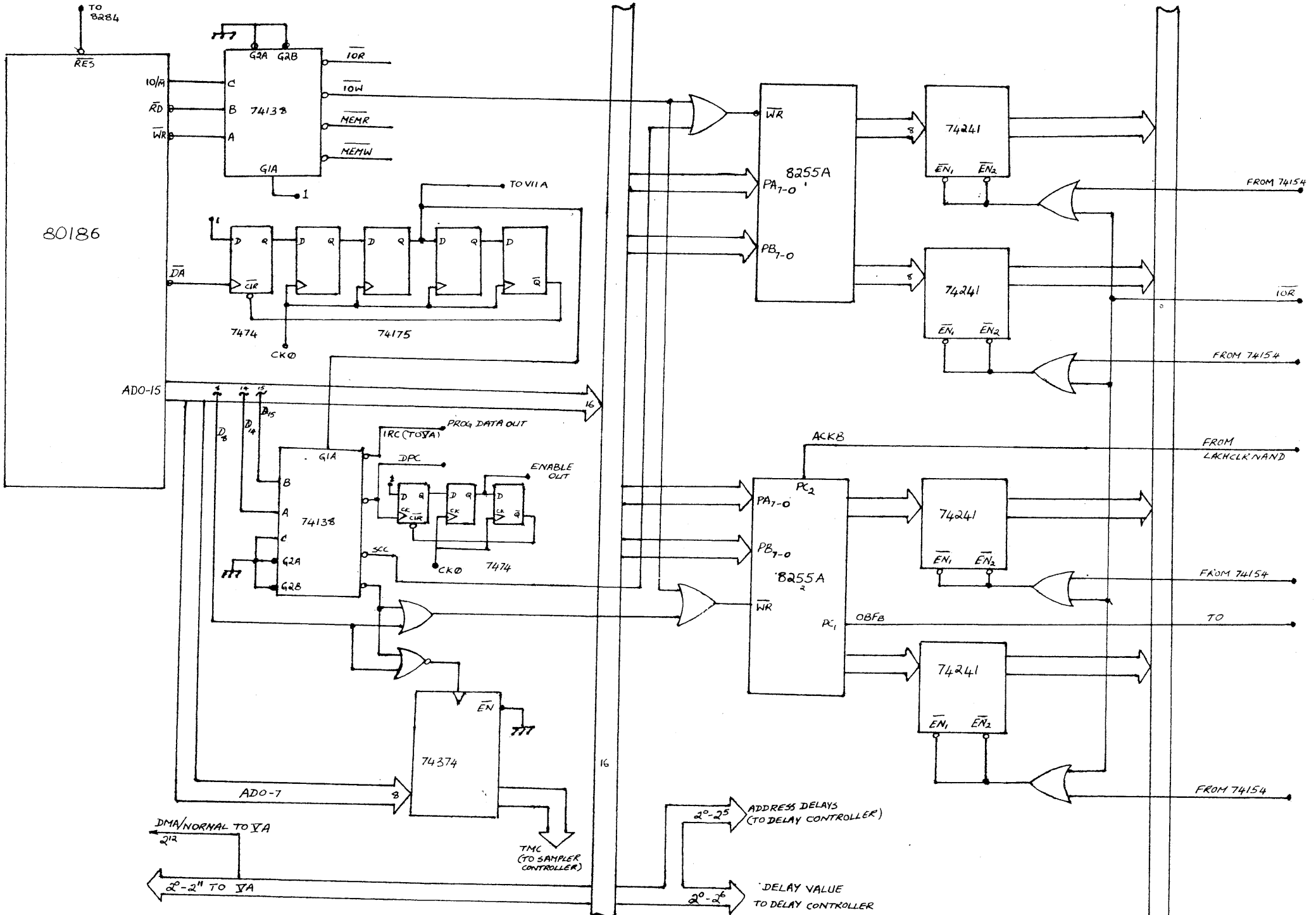
The output of the negative going pulse which is tapped for the sampler controller. An inverted pulse functions both as a Walsh clock and as the blank to delay controller.

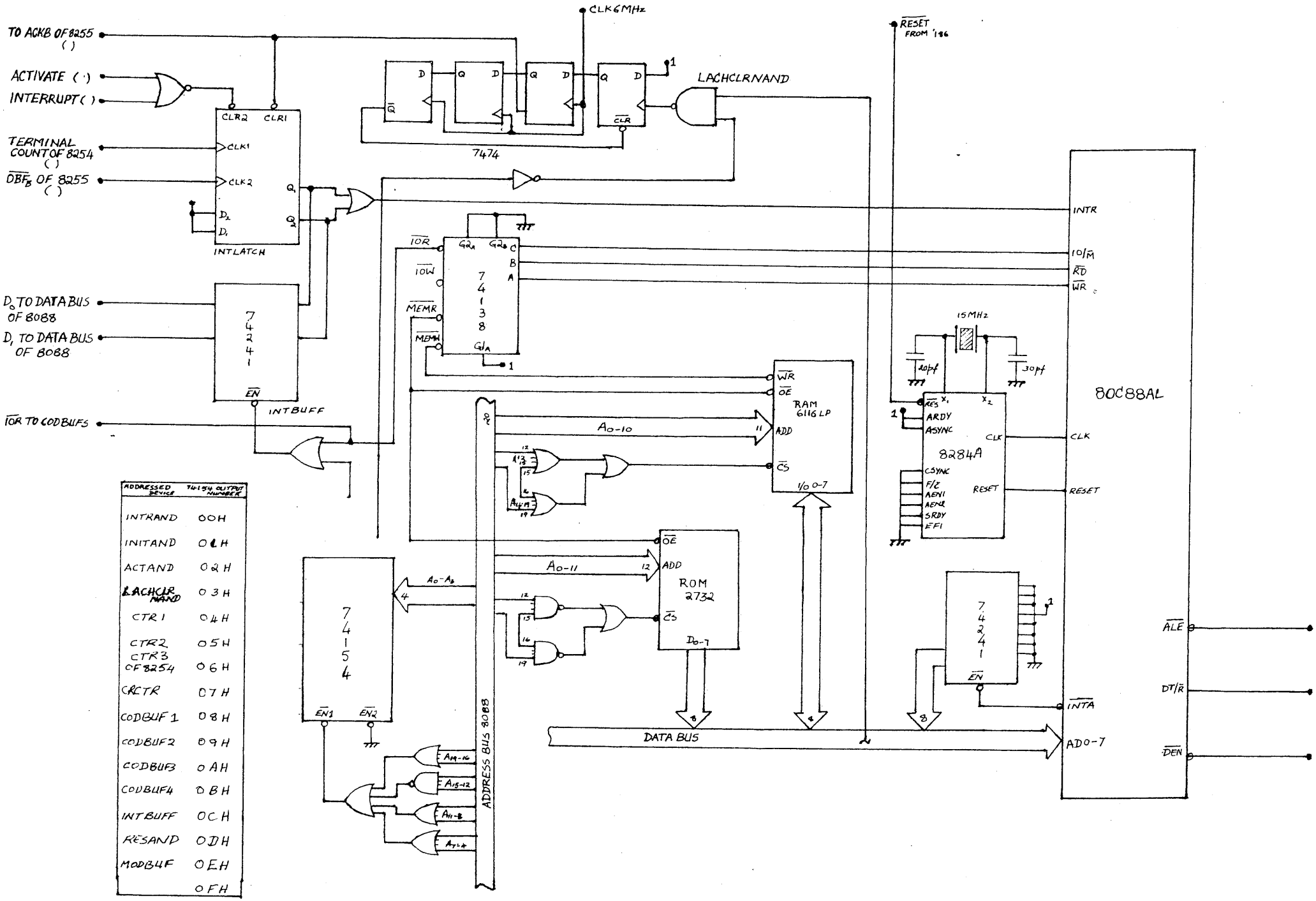
The phase signal which is equal to the smallest possible integration interval (10.96 ms) is generated in both inverted and noninverted versions by a D-flip-flop in toggle mode or divide by two mode. This output is suitably delayed using flip-flop register before the phase signal is sent to the correlator and inversion is sent to delay.

Pulse synchronisation is achieved (VI B (e)) for both the clr.rdy (clear ready from V A) and program delays (from VI A) with clock correlator control and the clock enable respectively. The programmed delays is the clock input to a D-flip-flop (74S74) with the D pin tied high. This flip-flop is followed by two other flip-flops connected in as a 2 bit shift register, clocked by CLK Enable. A $\overline{Q}$ fedback to the clear of the first flip-flop ensures that the enable out pulse to the delay controller is of 166 nano second maximum width.

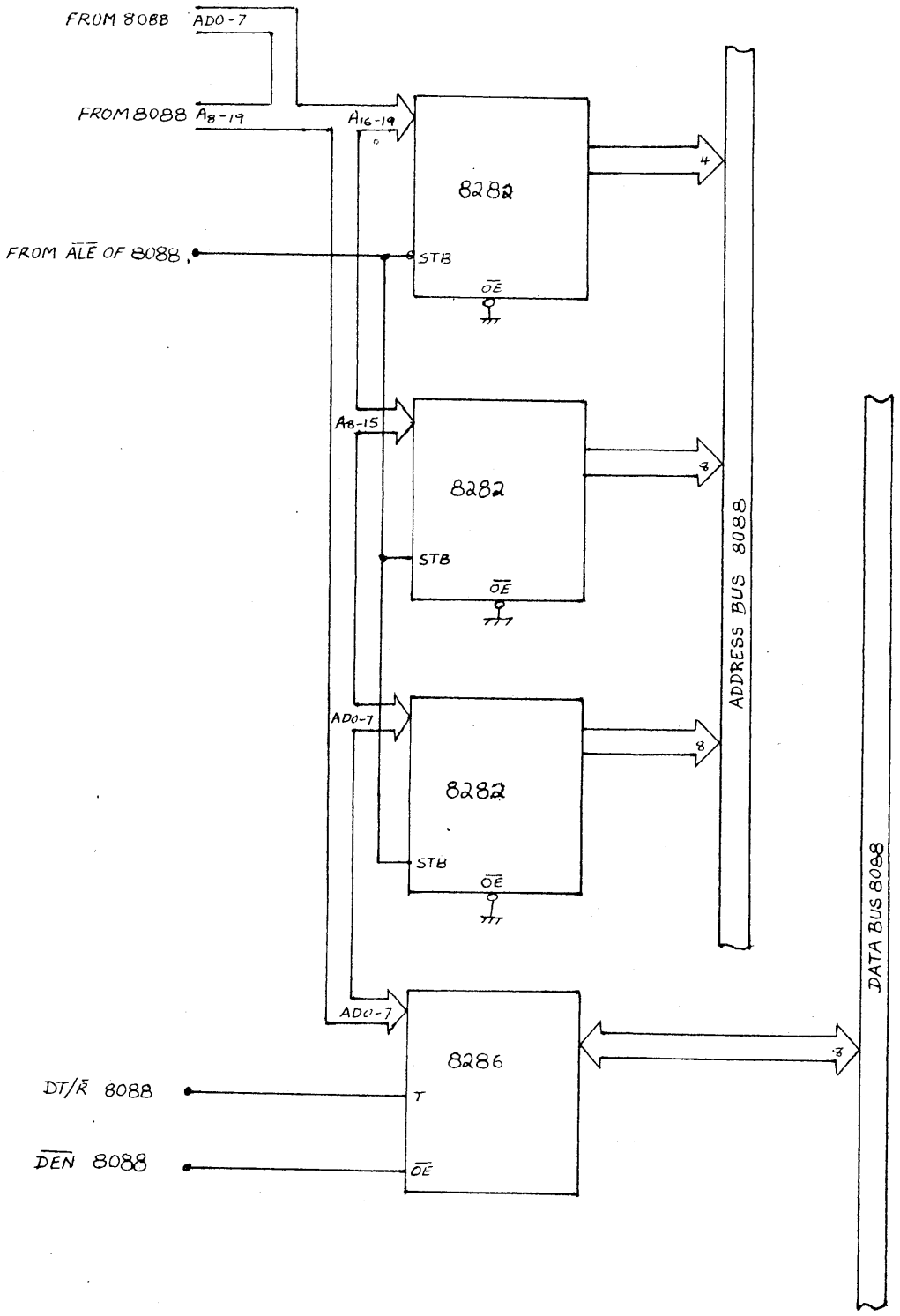
A similar connection for the Clr.rdy signal from board V A

ensures that the Clr.rdy pulse to the correlator is a maximum of 166 nano seconds. Four output bits - test mode, 2/3 level mode, horizontal switch and vertical switch are channelled to sampler control through a seperately addressable 74241 buffer. Further, the horizontal and vertical switch bits have to be sent to delay control also. These are tapped from the buffer inputs and are sent to delay through the buffer itself. A NAND'ed output of the vertical and horizontal switch bits specify whether or not the fan beam mode is operating. This output is also sent to the delay.

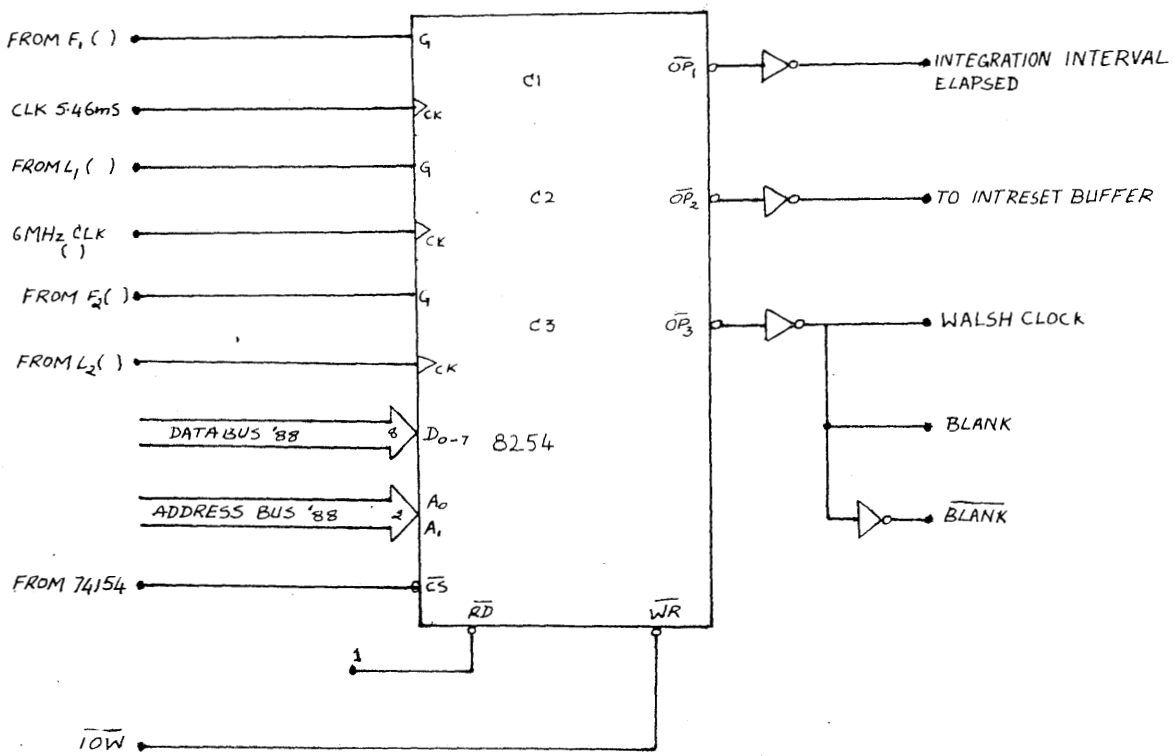

TO 8284
RES
80186
IO/M
RD
WR
ALE
DA
ADO-15
G2A G2B
G1A
74138
IOR
IOW
MEMR
MEMW
TO VII A
74474
74175
CKØ
D0
D14
D15
IRC (TO VA)
PROG DATA OUT
DPC
ENABLE OUT
SCC
8255A
PA7-0
PB7-0
PC2
PC1
OBFB
ACKB
74241
EN1
EN2
FROM 74154
FROM LACHCLK NAND
TO
74374
EN
ADO-7
DMA/NORNAL TO VA
2/2
2°-2¹¹ TO VA
TMC (TO SAMPLER CONTROLLER)
2°-25
ADDRESS DELAYS (TO DELAY CONTROLLER)
2°-26
DELAY VALUE TO DELAY CONTROLLER
16



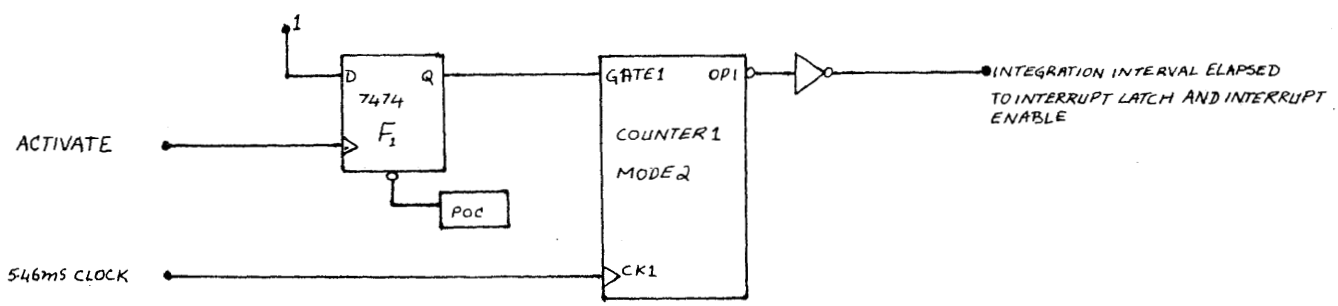
ADDRESSED DEVICE	74154 OUTPUT NUMBER
INTRAND	00H
INITAND	01H
ACTAND	02H
LACHCLR NAND	03H
CTR1	04H
CTR2	05H
CTR3 OF 8254	06H
CRCTR	07H
CODBUF1	08H
CODBUF2	09H
CODBUF3	0AH
CODBUF4	0BH
INTBUFF	0CH
RESAND	0DH
MODB4F	0EH
	0FH



DATA BUFFER FROM 8088



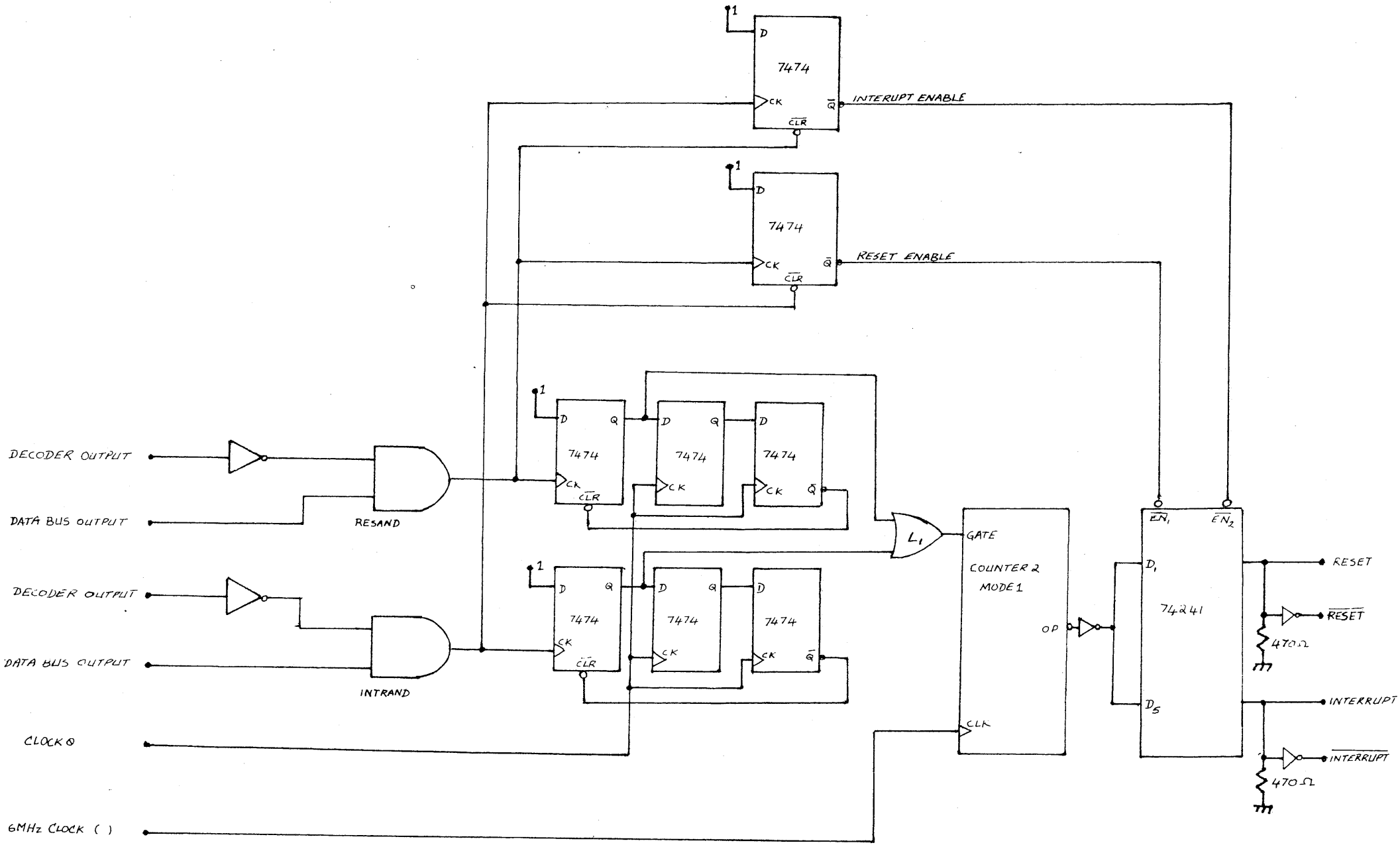
THE PROGRAMMABLE INTERVAL TIMER



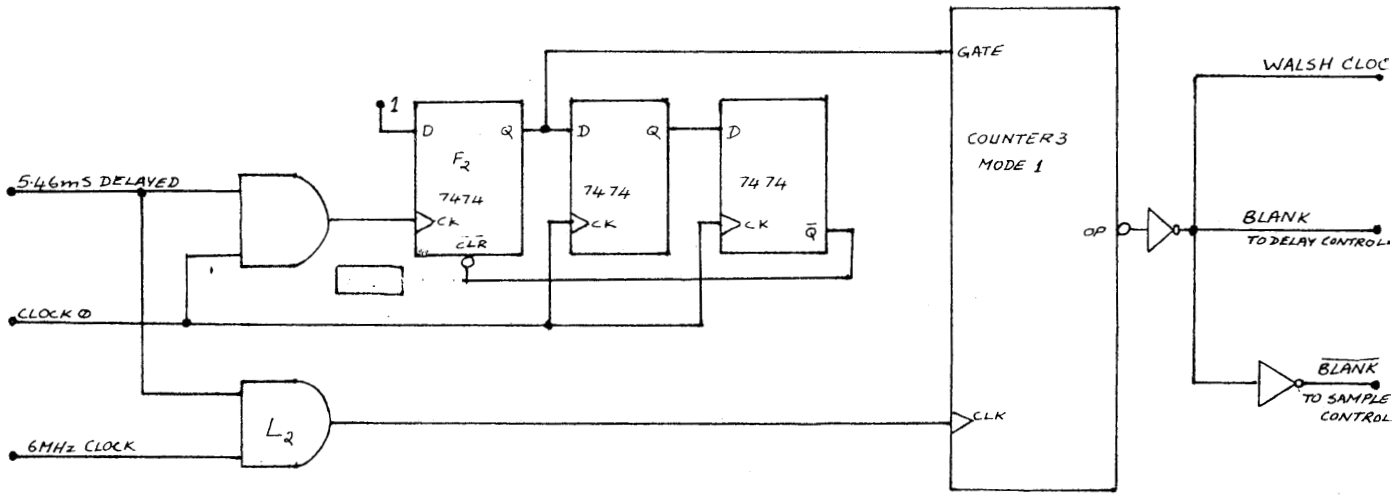
COUNTER 1 OF 8254

INTEGRATION INTERVAL COUNTER

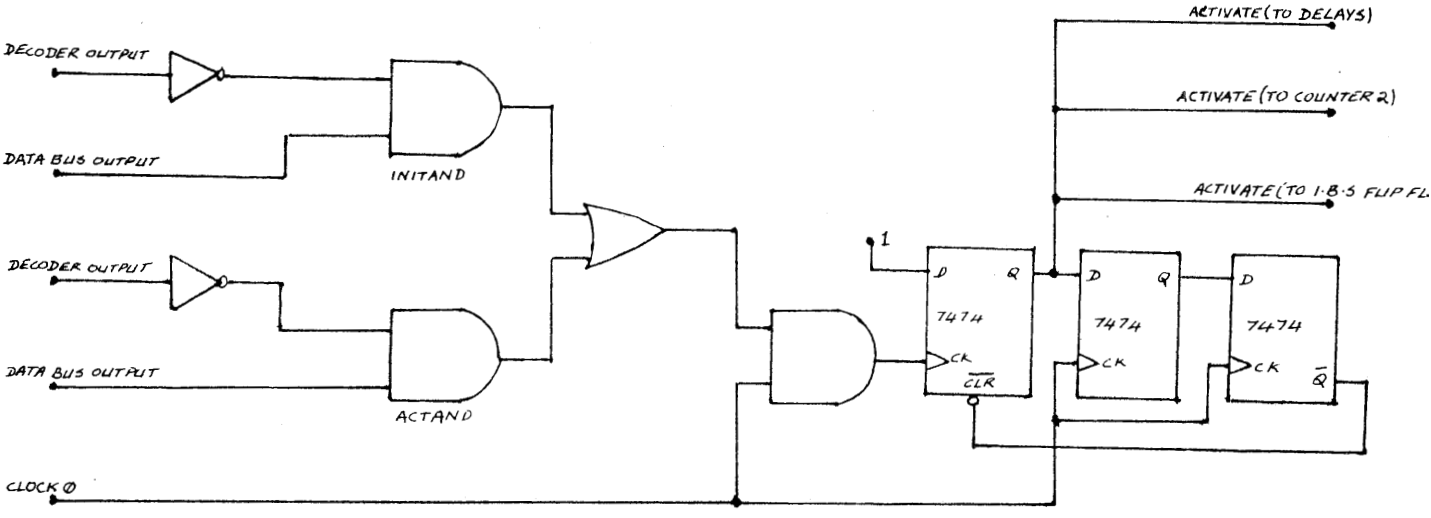
* POC IS POWER ON CLEAR CIRCUIT



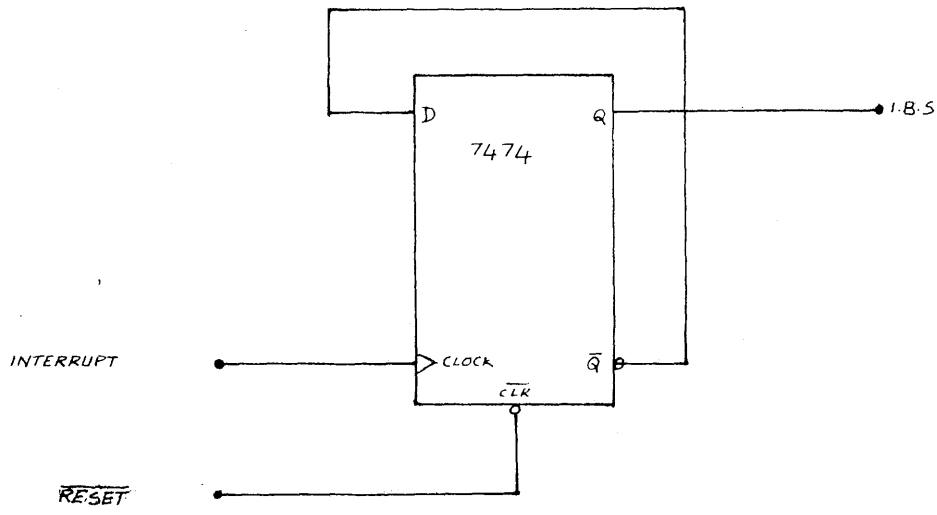
COUNTER 2 OF 8254 RESET & INTERRUPT GENERATION



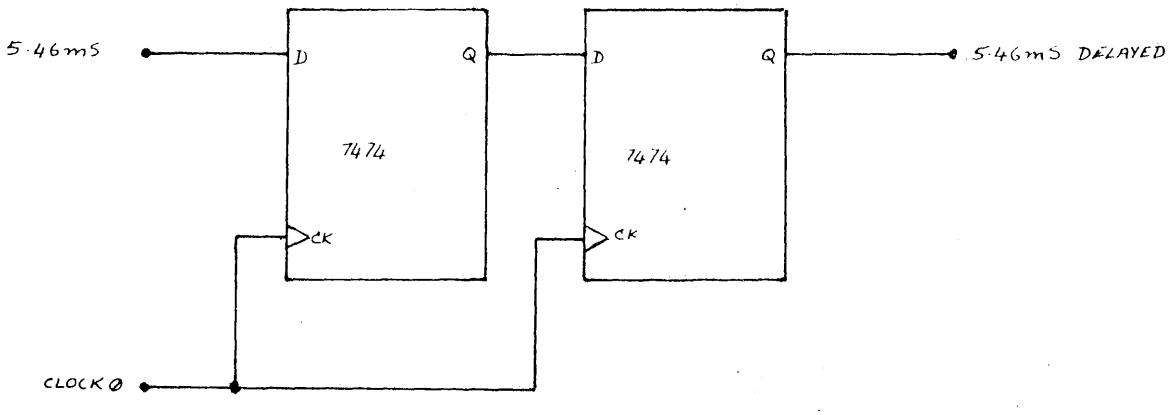
COUNTER 3 OF 8254
WALSH CLOCK AND BLANK GENERATION



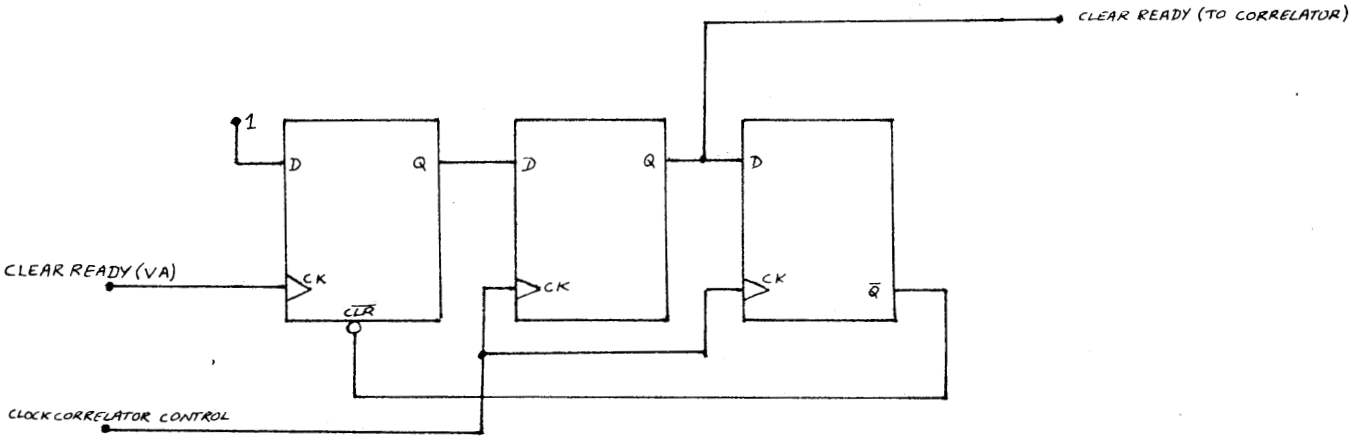
ACTIVATE GENERATION



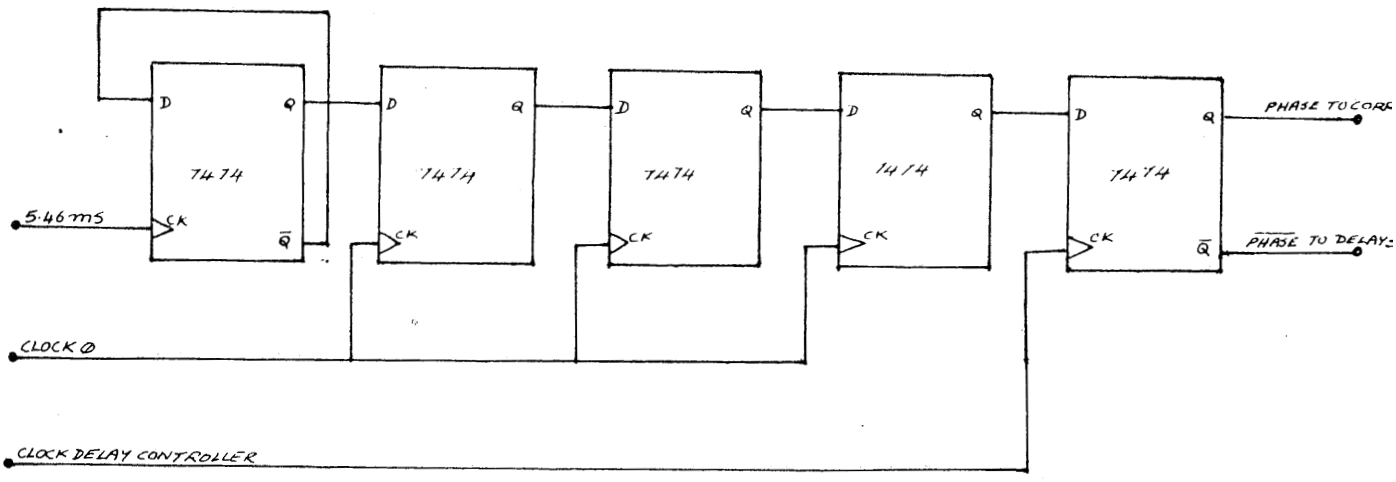
IBS FLIP-FLOP



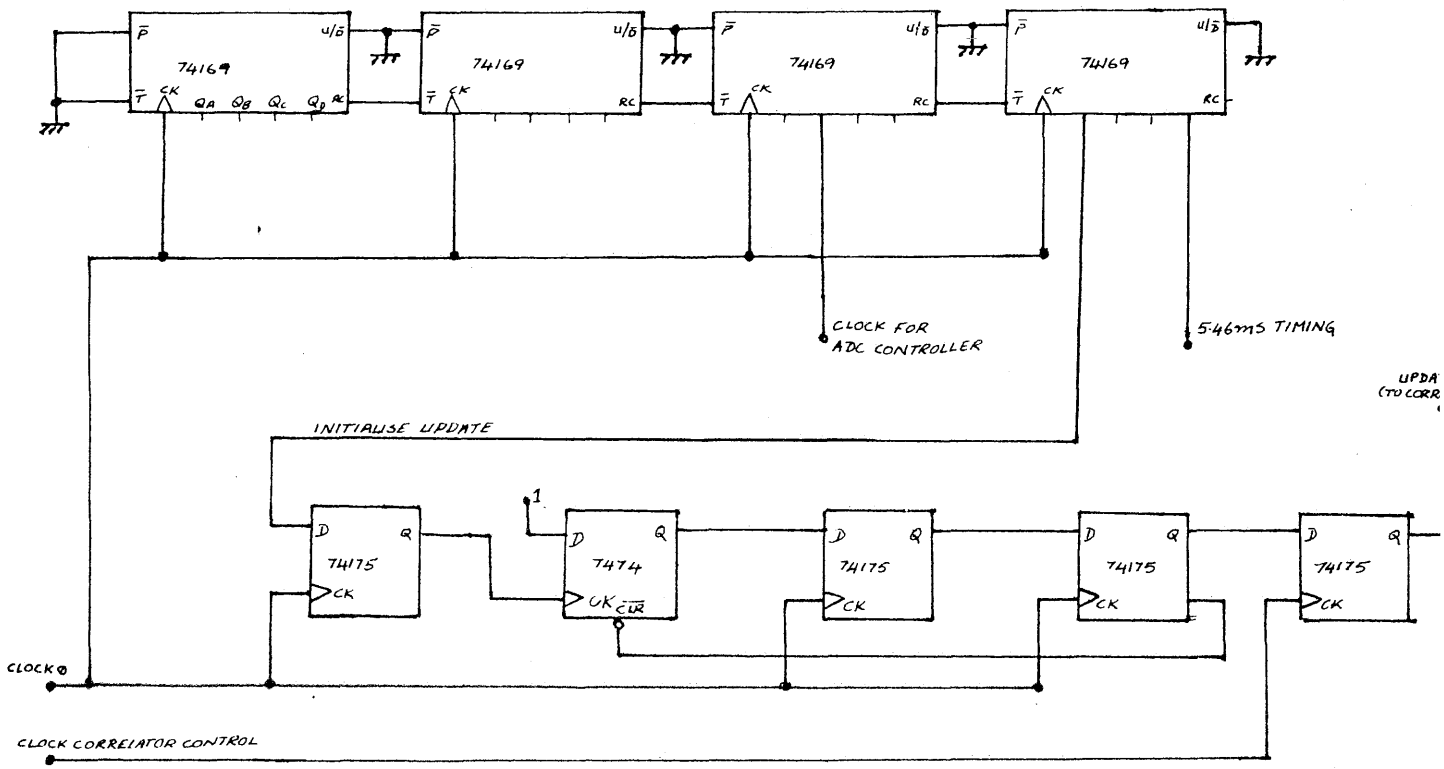
CLOCK DELAY CIRCUIT



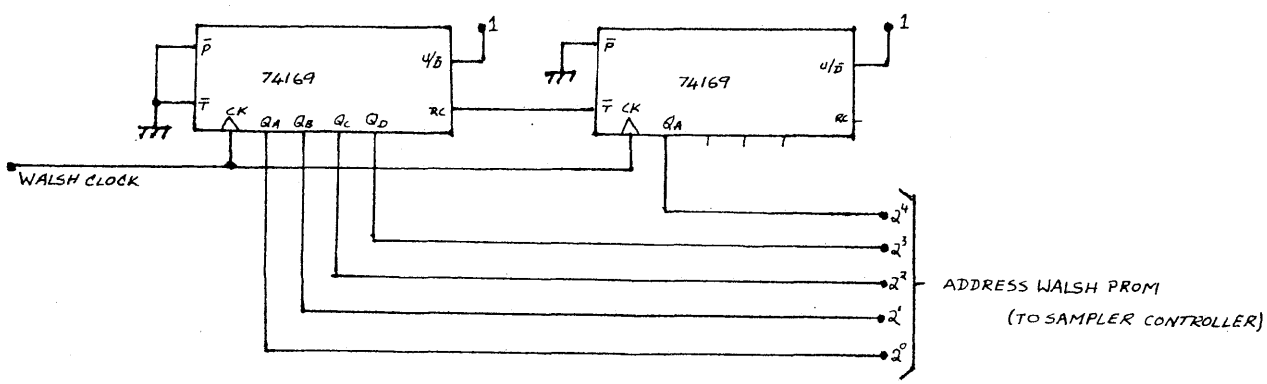
CLEAR READY SYNCHRONISATION



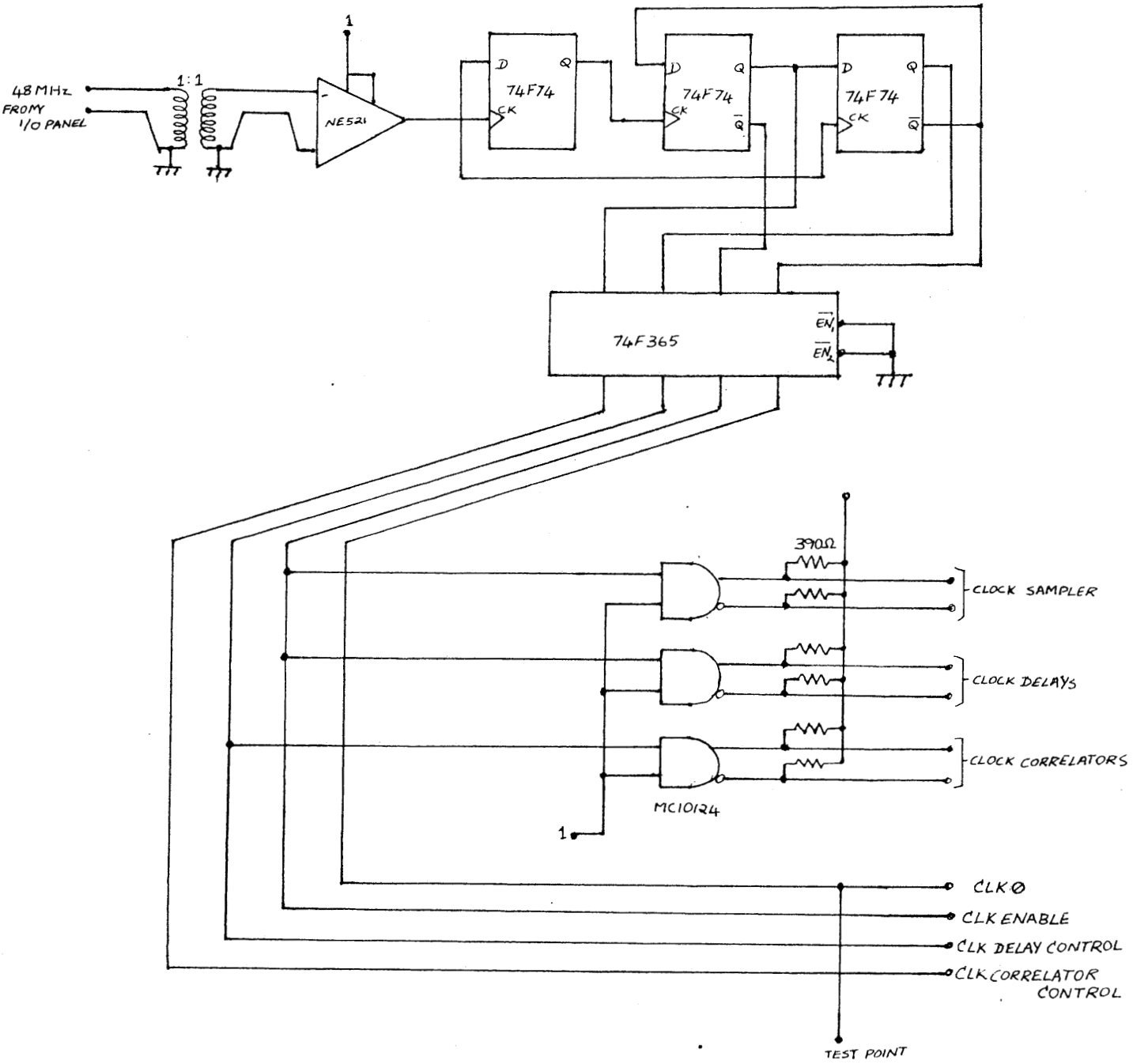
PHASE GENERATION



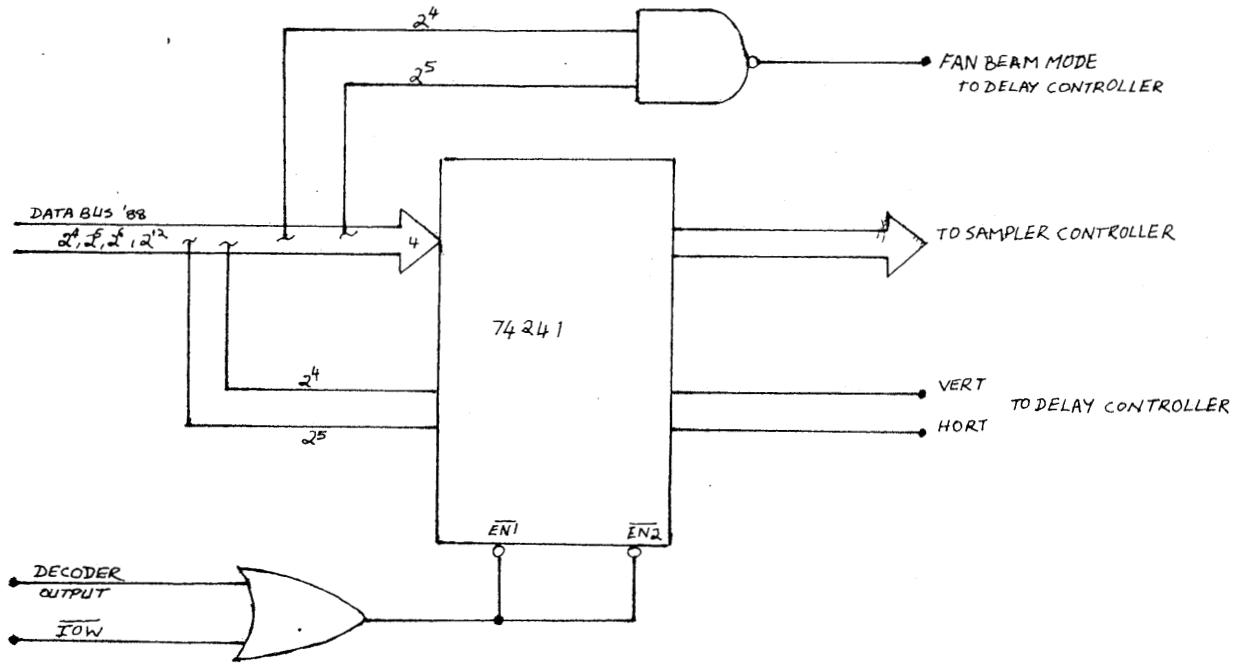
DIVIDER CHAIN AND UPDATE GENERATION



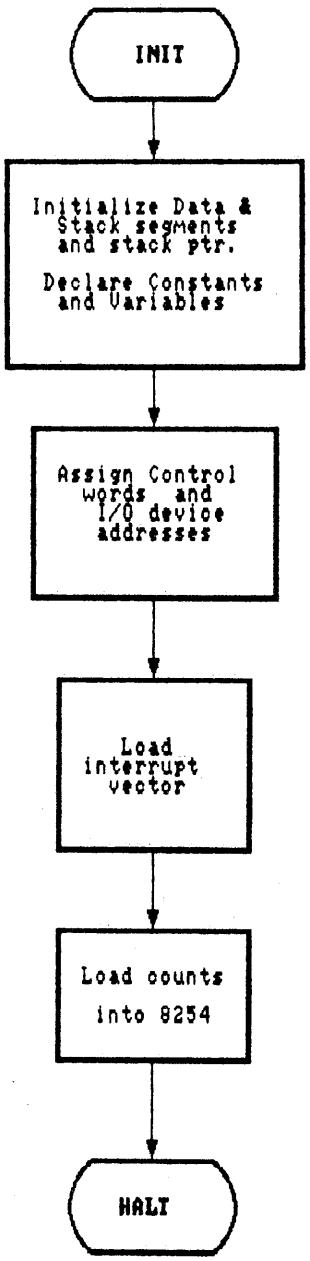
WALSH PROM ADDRESS GENERATION



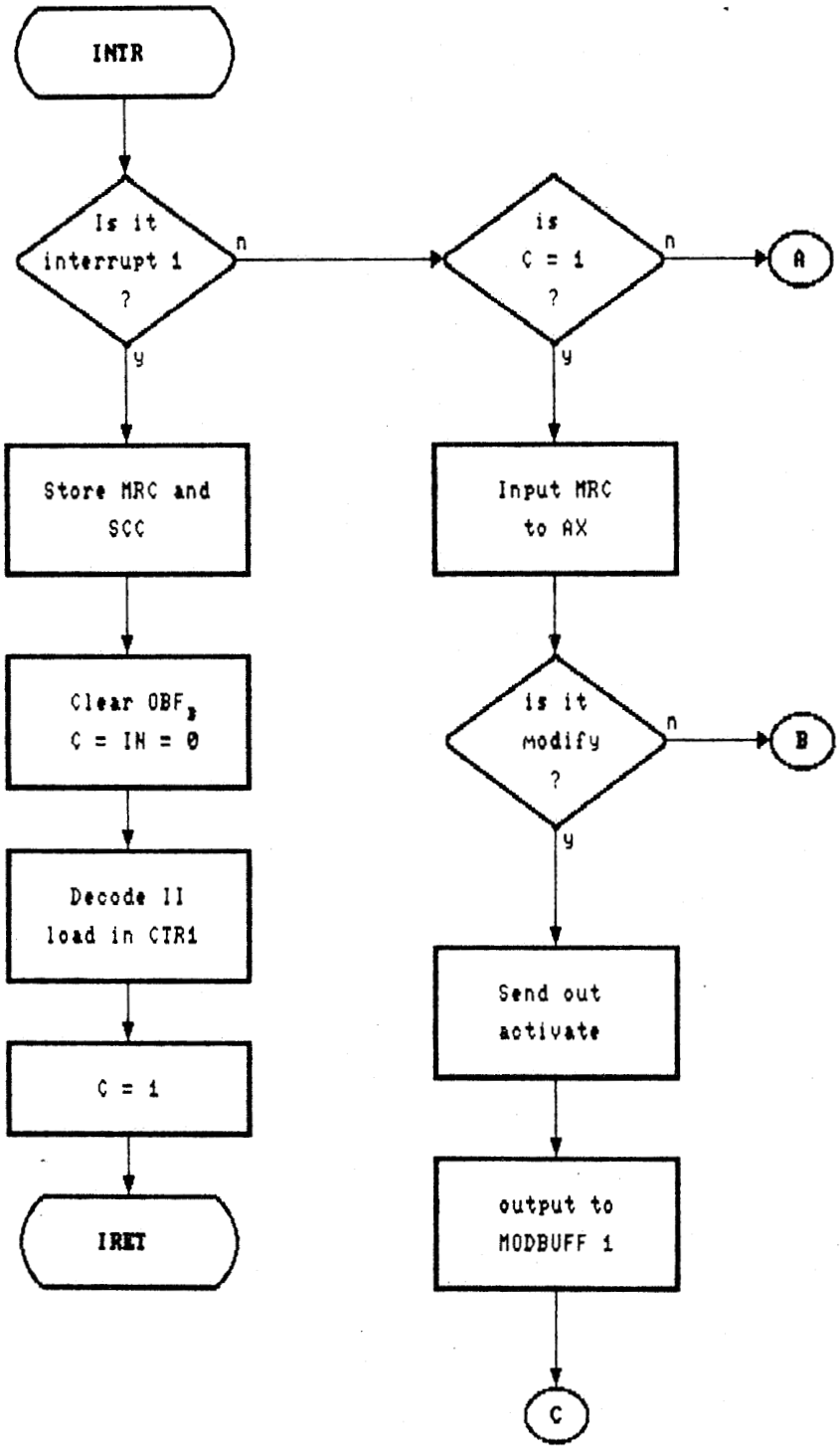
4 PHASE CLOCK GENERATOR AND CLOCK PHASE SELECTOR



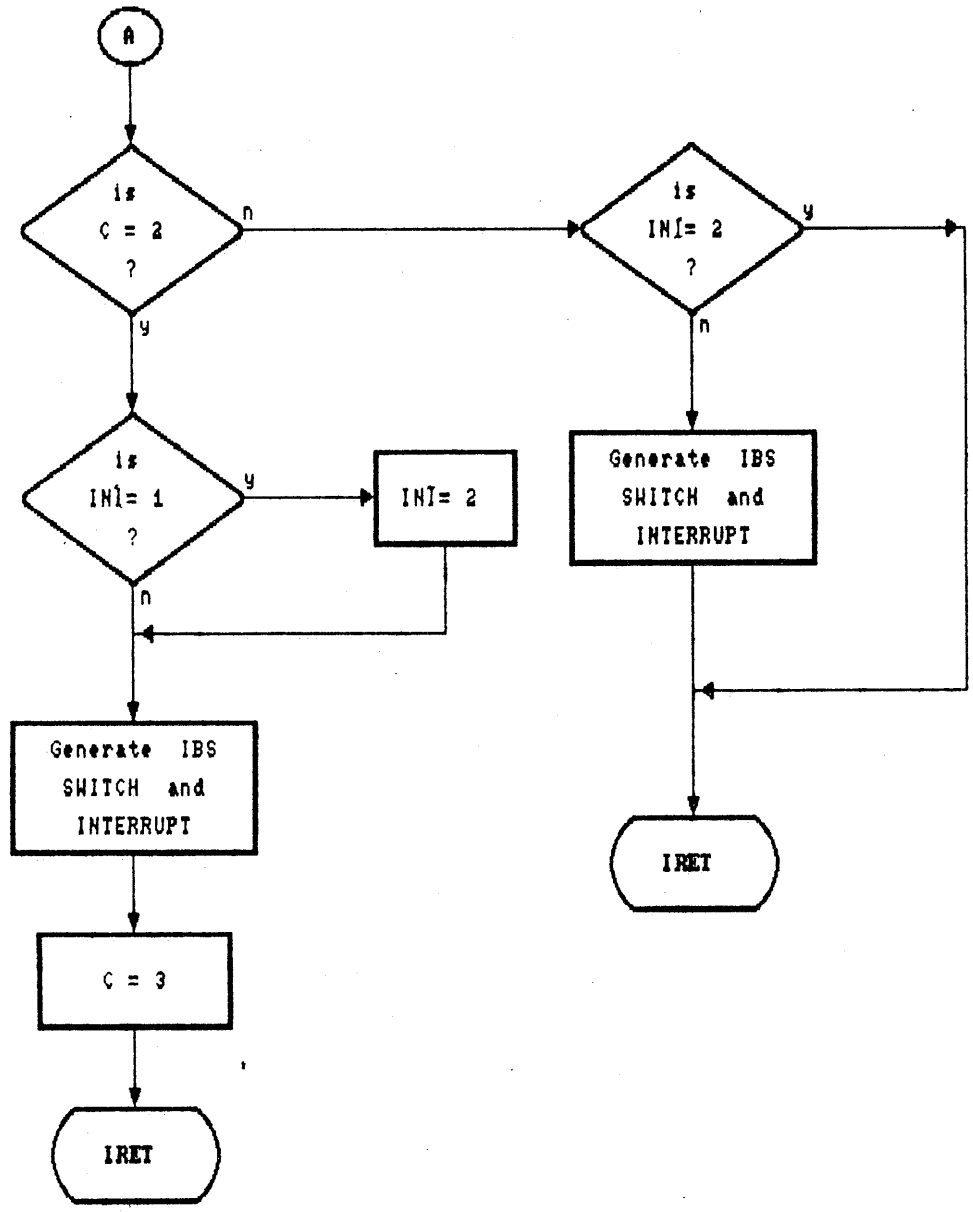
MODE SELECTION FOR SAMPLER CONTROL



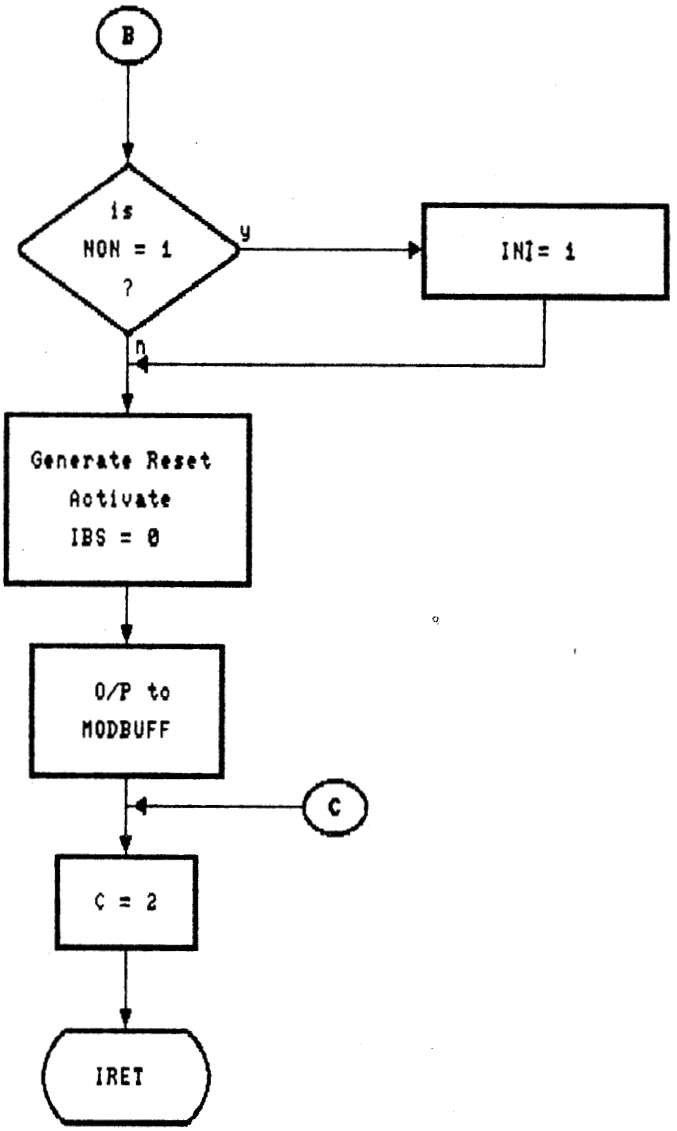
FLOWCHART SHEET 1 of 4



FLOWCHART SHEET 2 of 4



FLOWCHART SHEET 3 of 4



FLOWCHART SHEET 4 of 4

```
        if1
        include macro.lib
        endif

int_vec segment at      0h
        org     020h

        dd      int_rout
int_vec ends

;-----------------------------------;
;           DATA SEGMENT            ;
;-----------------------------------;

data_seg        segment at      070h

        memsc           dw      ?
        memmr           dw      ?
        i               dw      ?
        ini             dw      ?
        c               dw      ?

data_seg        ends

;-----------------------------------;
;          STACK SEGMENT            ;
;-----------------------------------;


stack_seg       segment at      075h

                dw      50 dup(?)
        tos             label   word
stack_seg       ends

;-----------------------------------;
;           CODE SEGMENT            ;
;-----------------------------------;


code_seg    segment     at      0ff00h
            assume cs:code_seg,ds:data_seg, ss:stack_seg


        intrand         equ     0f000h
```

```
initand          equ     0f001h
actand           equ     0f002h
resand           equ     0f00dh
lachclrnand      equ     0f003h
ctr1             equ     0f004h
ctr2             equ     0f005h
ctr3             equ     0f006h
crctr            equ     0f007h
codbuff1         equ     0f008h
codbuff2         equ     0f009h
codbuff3         equ     0f00ah
codbuff4         equ     0f00bh
intbuff          equ     0f00ch
modbuff          equ     0f00eh
cwctr1           equ     034h
cwctr2           equ     052h
cwctr3           equ     092h
cntctr2          equ     009h
cntctr3          equ     080h
datintrand       equ     01h
datinitand       equ     02h
datresactand     equ     04h
datlachclrnand   equ     08h
datresand        equ     010h

start :
        mov     ax, data_seg
        mov     ds, ax                  ; point ds to data
                                          seg
        mov     ax, stack_seg
        mov     ss, ax                  ; point  ss  to
                                          stack seg
        mov     sp, offset tos          ; init stack

intvectlod :
        push    ds                      ; save ds
        xor     ax, ax                  ; 0 ax
        mov     ds, ax                  ; 0 ds
        mov     bx, offset int_rout
        mov     ax, offset inint
        mov     [bx], ax                ; store offset of
                                          intr
        mov     ax, code_seg
        mov     [bx+2], ax              ; store reg.addr.
                                          of intr
        pop     ds                      ; restore ds

loadcw :
        mov     al, cwctr1
      @_sout    <crctr>                 ; load cw of ctr1
        mov     al, cwctr2
      @_sout    <crctr>                 ; load cw of ctr2
        mov     al, cwctr3
      @_sout    <crctr>                 ; load cw of ctr3
```

```
        loadcnt :
                  mov     al, cntctr2
                @_sout    <crctr>                 ; load count  of
ctr2
                  mov     al, cntctr3
                @_sout    <crctr>                 ; load count  of
ctr3
                  hlt                             ; halt

        inint :
                  xor     ax, ax                  ; zero
                                                    accumulator
                  xor     cx, cx                  ; zero reg. c

                @_gin     <intbuff>               ; input interrupt
                                                    word
                  cmp     al, 01                  ; check if 1
                  jnz     intr21                  ; if not 1  goto
                                                    intr21
                @_gin    <codbuff>
                @_gin    <codbuff2>
                  mov     memsc, ax
                @_gin    <codbuff3>
                @_gin    <codbuff4>
                  mov     memr, ax
                  mov     ax, datlachclrnand
                @_sout   <lachclrnand>

        integint :
                  push    ax
                  mov     ax, memsc
                  and     ax, 0fh                 ; extract it
                  add     al, 01
                  mov     cl, al
                  shl     ax, cl
                  sub     ax, 01                  ; decode  count
                                                    from it
                @_sout    <ctr1>
                @_sout    <ctr1>                  ; output count to
ctr1
                  pop     ax
                  mov     ax, 1
                  mov     c, ax

        intret :
                  iret


        intr21:
                  mov     ax, c
                  cmp     ax, 1
                  jnz     intr23
                  mov     ax, memrc
                  and     ax, 7h
                  cmp     ax, 0
```

```
        jnz     chkbits
        mov     ax, datactand
      @_sout    <actand>
        call near ptr modbuff
        mov     ax, 2
        mov     c, ax
        jmp     intret

intr1 :
      @_gin     <codbuf1>
      @_gin     <codbuf2>
        mov     memsc, ax
      @_gin     <codbuf3>
      @_gin     <codbuf4>
        mov     memmr, ax
        mov     ax, datlachclrnand
      @_sout    <lachclrnand>

integint:
        mov     ax, 1
        mov     c, ax
        mov     ax, 0
        mov     ini, ax
        jmp     intret

intr22 :
        mov     ax, c
        cmp     ax, 2
        jnz     intr23
        mov     ax, ini
        cmp     ax, 1
        jnz     theta
        mov     ax, 2
        mov     ini, ax

theta :
        mov     ax, datintrand
      @_sout    <intrand>
        mov     ax, 3
        mov     c, ax
        jmp     intret

intr23  :
        mov     ax, ini
        cmp     ax, 2
        jz      intretrn
        mov     ax, datintrand
      @_sout    <intrand>

intretrn:
        jmp     intret

chkbits :

        and     ax, 3
```

```
        cmp     ax, 3
        jnz     chk1
        mov     ax, 1
        mov     ini, ax
        jmp     genrai

chk1 :
        and     ax, 1
        cmp     ax, 1
        jz      genrai

genrai :

        mov     ax, datactand
      @_sout    <actand>
        call near ptr modbuffer
        mov     ax, datresand
      @_sout    <resand>
        mov     ax, 2
        mov     i, 2
        jmp     intret

        modbuffer proc near

modb:
        mov     ax, memsc
        and     ax, 1070h
        xor     bx, bx
        mov     bh, ah
        mov     cl, 05
        shr     bx, cl
        and     ax, 0070H
        add     ax, bx
      @_sout    <modbuff>

modbuffer       endp
code_seg        ends
                end start


CREATE "MACRO.LIB"

; @_sout
        macro   aport?
        local   around, where
        push    dx
        out     dx, al
        mov     where, dx
        jmp     around
where   dw      aport?

around:
        endm
```

```
@_gin   macro   aport?
        local   around, where
        push    dx
        mov     dx, where
        in      al, dx
        jmp     around
where   dw      aport?

around:
        endm
```

CONCLUSION

In this project, a means of arriving at a previously hardwired circuit for a computer controller interface for a radio telescope correlator system has been attempted at, using an intelligent system based on a Intel 8088 microprocessor.

The existing system was made up of two boards VI A and VI B which were implemented using digital hardware only.

The system has the following advantages over the existing system.

a) The entire hardware is laid out on one card.

b) The system is easily software upgradable.

c) This system is perfectly compatible with the 80186 master processor of the data acquisition system.

DATA SHEETS

8088
8-BIT HMOS MICROPROCESSOR
8088/8088-2

- 8-Bit Data Bus Interface
- 16-Bit Internal Architecture
- Direct Addressing Capability to 1 Mbyte of Memory
- Direct Software Compatibility with 8086 CPU
- 14-Word by 16-Bit Register Set with Symmetrical Operations
- 24 Operand Addressing Modes
- Byte, Word, and Block Operations
- 8-Bit and 16-Bit Signed and Unsigned Arithmetic in Binary or Decimal, Including Multiply and Divide
- Two Clock Rates:
  - 5 MHz for 8088
  - 8 MHz for 8088-2
- Available in EXPRESS
  - Standard Temperature Range
  - Extended Temperature Range

The Intel® 8088 is a high performance microprocessor implemented in N-channel, depletion load, silicon gate technology (HMOS), and packaged in a 40-pin CERDIP package. The processor has attributes of both 8- and 16-bit microprocessors. It is directly compatible with 8086 software and 8080/8085 hardware and peripherals.

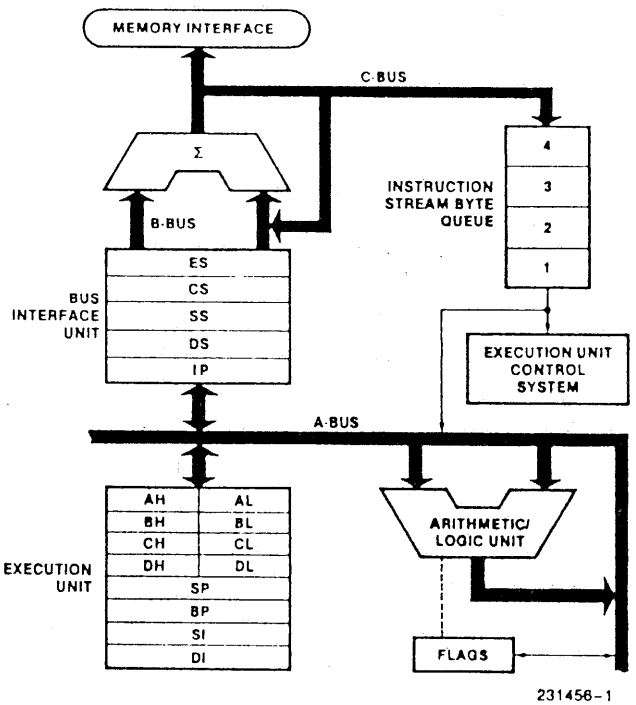


Figure 1. 8088 CPU Functional Block Diagram

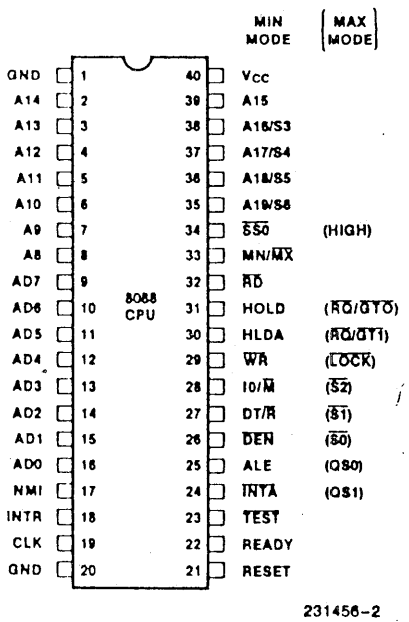


Figure 2. 8088 Pin Configuration

Table 1. Pin Description

The following pin function descriptions are for 8088 systems in either minimum or maximum mode. The "local bus" in these descriptions is the direct multiplexed bus interface connection to the 8088 (without regard to additional bus buffers).

Symbol	Pin No.	Type	Name and Function
AD7–AD0	9–16	I/O	**ADDRESS DATA BUS:** These lines constitute the time multiplexed memory/IO address (T1) and data (T2, T3, Tw, T4) bus. These lines are active HIGH and float to 3-state OFF during interrupt acknowledge and local bus "hold acknowledge".
A15–A8	2–8, 39	O	**ADDRESS BUS:** These lines provide address bits 8 through 15 for the entire bus cycle (T1–T4). These lines do not have to be latched by ALE to remain valid. A15–A8 are active HIGH and float to 3-state OFF during interrupt acknowledge and local bus "hold acknowledge".
A19/S6, A18/S5, A17/S4, A16/S3	35–38	O	**ADDRESS/STATUS:** During T1, these are the four most significant address lines for memory operations. During I/O operations, these lines are LOW. During memory and I/O operations, status information is available on these lines during T2, T3, Tw, and T4. S6 is always low. The status of the interrupt enable flag bit (S5) is updated at the beginning of each clock cycle. S4 and S3 are encoded as shown. This information indicates which segment register is presently being used for data accessing. These lines float to 3-state OFF during local bus "hold acknowledge".

S4	S3	Characteristics
0 (LOW)	0	Alternate Data
0	1	Stack
1 (HIGH)	0	Code or None
1	1	Data
S6 is 0 (LOW)		

$\overline{RD}$	32	O	**READ:** Read strobe indicates that the processor is performing a memory or I/O read cycle, depending on the state of the IO/$\overline{M}$ pin or S2. This signal is used to read devices which reside on the 8088 local bus. $\overline{RD}$ is active LOW during T2, T3 and Tw of any read cycle, and is guaranteed to remain HIGH in T2 until the 8088 local bus has floated. This signal floats to 3-state OFF in "hold acknowledge".
READY	22	I	**READY:** is the acknowledgement from the addressed memory or I/O device that it will complete the data transfer. The RDY signal from memory or I/O is synchronized by the 8284 clock generator to form READY. This signal is active HIGH. The 8088 READY input is not synchronized. Correct operation is not guaranteed if the set up and hold times are not met.
INTR	18	I	**INTERRUPT REQUEST:** is a level triggered input which is sampled during the last clock cycle of each instruction to determine if the processor should enter into an interrupt acknowledge operation. A subroutine is vectored to via an interrupt vector lookup table located in system memory. It can be internally masked by software resetting the interrupt enable bit. INTR is internally synchronized. This signal is active HIGH.
$\overline{TEST}$	23	I	**$\overline{TEST}$:** input is examined by the "wait for test" instruction. If the $\overline{TEST}$ input is LOW, execution continues, otherwise the processor waits in an "idle" state. This input is synchronized internally during each clock cycle on the leading edge of CLK.

Table 1. Pin Description (Continued)

Symbol	Pin No.	Type	Name and Function
NMI	17	I	**NON-MASKABLE INTERRUPT:** is an edge triggered input which causes a type 2 interrupt. A subroutine is vectored to via an interrupt vector lookup table located in system memory. NMI is not maskable internally by software. A transition from a LOW to HIGH initiates the interrupt at the end of the current instruction. This input is internally synchronized.
RESET	21	I	**RESET:** causes the processor to immediately terminate its present activity. The signal must be active HIGH for at least four clock cycles. It restarts execution, as described in the instruction set description, when RESET returns LOW. RESET is internally synchronized.
CLK	19	I	**CLOCK:** provides the basic timing for the processor and bus controller. It is asymmetric with a 33% duty cycle to provide optimized internal timing.
V_{CC}	40		**V_{CC}:** is the +5V ±10% power supply pin.
GND	1, 20		**GND:** are the ground pins.
MN/$\overline{MX}$	33	I	**MINIMUM/MAXIMUM:** indicates what mode the processor is to operate in. The two modes are discussed in the following sections.

The following pin function descriptions are for the 8088 minimum mode (i.e., MN/$\overline{MX}$ = V_{CC}). Only the pin functions which are unique to minimum mode are described; all other pin functions are as described above.

Symbol	Pin No.	Type	Name and Function
IO/$\overline{M}$	28	O	**STATUS LINE:** is an inverted maximum mode $\overline{S2}$. It is used to distinguish a memory access from an I/O access. IO/$\overline{M}$ becomes valid in the T4 preceding a bus cycle and remains valid until the final T4 of the cycle (I/O = HIGH, M = LOW). IO/$\overline{M}$ floats to 3-state OFF in local bus "hold acknowledge".
$\overline{WR}$	29	O	**WRITE:** strobe indicates that the processor is performing a write memory or write I/O cycle, depending on the state of the IO/$\overline{M}$ signal. WR is active for T2, T3, and Tw of any write cycle. It is active LOW, and floats to 3-state OFF in local bus "hold acknowledge".
$\overline{INTA}$	24	O	**INTA:** is used as a read strobe for interrupt acknowledge cycles. It is active LOW during T2, T3, and Tw of each interrupt acknowledge cycle.
ALE	25	O	**ADDRESS LATCH ENABLE:** is provided by the processor to latch the address into an address latch. It is a HIGH pulse active during clock low of T1 of any bus cycle. Note that ALE is never floated.
DT/$\overline{R}$	27	O	**DATA TRANSMIT/RECEIVE:** is needed in a minimum system that desires to use a data bus transceiver. It is used to control the direction of data flow through the transceiver. Logically, DT/$\overline{R}$ is equivalent to $\overline{S1}$ in the maximum mode, and its timing is the same as for IO/$\overline{M}$ (T = HIGH, R = LOW). This signal floats to 3-state OFF in local "hold acknowledge".
$\overline{DEN}$	26	O	**DATA ENABLE:** is provided as an output enable for the data bus transceiver in a minimum system which uses the transceiver. $\overline{DEN}$ is active LOW during each memory and I/O access, and for $\overline{INTA}$ cycles. For a read or $\overline{INTA}$ cycle, it is active from the middle of T2 until the middle of T4, while for a write cycle, it is active from the beginning of T2 until the middle of T4. $\overline{DEN}$ floats to 3-state OFF during local bus "hold acknowledge".

Table 1. Pin Description (Continued)

Symbol	Pin No.	Type	Name and Function
HOLD, HLDA	31, 30	I, O	**HOLD:** indicates that another master is requesting a local bus "hold". To be acknowledged, HOLD must be active HIGH. The processor receiving the "hold" request will issue HLDA (HIGH) as an acknowledgement, in the middle of a T4 or TI clock cycle. Simultaneous with the issuance of HLDA the processor will float the local bus and control lines. After HOLD is detected as being LOW, the processor lowers HLDA, and when the processor needs to run another cycle, it will again drive the local bus and control lines. Hold is not an asynchronous input. External synchronization should be provided if the system cannot otherwise guarantee the set up time.
$\overline{SSO}$	34	O	**STATUS LINE:** is logically equivalent to $\overline{SO}$ in the maximum mode. The combination of $\overline{SSO}$, IO/$\overline{M}$ and DT/$\overline{R}$ allows the system to completely decode the current bus cycle status.

IO/$\overline{M}$	DT/$\overline{R}$	$\overline{SSO}$	Characteristics
1(HIGH)	0	0	Interrupt Acknowledge
1	0	1	Read I/O Port
1	1	0	Write I/O Port
1	1	1	Halt
0(LOW)	0	0	Code Access
0	0	1	Read Memory
0	1	0	Write Memory
0	1	1	Passive

The following pin function descriptions are for the 8088/8288 system in maximum mode (i.e., MN/$\overline{MX}$ = GND). Only the pin functions which are unique to maximum mode are described; all other pin functions are as described above.

Symbol	Pin No.	Type	Name and Function
$\overline{S2}$, $\overline{S1}$, $\overline{S0}$	26–28	O	**STATUS:** is active during clock high of T4, T1, and T2, and is returned to the passive state (1,1,1) during T3 or during Tw when READY is HIGH. This status is used by the 8288 bus controller to generate all memory and I/O access control signals. Any change by $\overline{S2}$, $\overline{S1}$, or $\overline{S0}$ during T4 is used to indicate the beginning of a bus cycle, and the return to the passive state in T3 and Tw is used to indicate the end of a bus cycle. These signals float to 3-state OFF during "hold acknowledge". During the first clock cycle after RESET becomes active, these signals are active HIGH. After this first clock, they float to 3-state OFF.

$\overline{S2}$	$\overline{S1}$	$\overline{S0}$	Characteristics
0(LOW)	0	0	Interrupt Acknowledge
0	0	1	Read I/O Port
0	1	0	Write I/O Port
0	1	1	Halt
1(HIGH)	0	0	Code Access
1	0	1	Read Memory
1	1	0	Write Memory
1	1	1	Passive

A.C. CHARACTERISTICS

(T_A = 0°C to 70°C, T_{CASE} (Plastic) = 0°C to 95°C, T_{CASE} (CERDIP) = 0°C to 75°C,
T_A = 0°C to 55°C and T_{CASE} = 0°C to 80°C for P8088-2 only
T_A is guaranteed as long as T_{CASE} is not exceeded)

(V_{CC} = 5V ±10% for 8088, V_{CC} = 5V ±5% for 8088-2 and Extended Temperature EXPRESS)

MINIMUM COMPLEXITY SYSTEM TIMING REQUIREMENTS

Symbol	Parameter	8088		8088-2		Units	Test Conditions
		Min	Max	Min	Max		
TCLCL	CLK Cycle Period	200	500	125	500	ns	
TCLCH	CLK Low Time	118		68		ns	
TCHCL	CLK High Time	69		44		ns	
TCH1CH2	CLK Rise Time		10		10	ns	From 1.0V to 3.5V
TCL2CL2	CLK Fall Time		10		10	ns	From 3.5V to 1.0V
TDVCL	Data in Setup Time	30		20		ns	
TCLDX	Data in Hold Time	10		10		ns	
TR1VCL	RDY Setup Time into 8284 (Notes 1, 2)	35		35		ns	
TCLR1X	RDY Hold Time into 8284 (Notes 1, 2)	0		0		ns	
TRYHCH	READY Setup Time into 8088	118		68		ns	
TCHRYX	READY Hold Time into 8088	30		20		ns	
TRYLCL	READY Inactive to CLK (Note 3)	−8		−8		ns	
THVCH	HOLD Setup Time	35		20		ns	
TINVCH	INTR, NMI, $\overline{\text{TEST}}$ Setup Time (Note 2)	30		15		ns	
TILIH	Input Rise Time (Except CLK)		20		20	ns	From 0.8V to 2.0V
TIHIL	Input Fall Time (Except CLK)		12		12	ns	From 2.0V to 0.8V

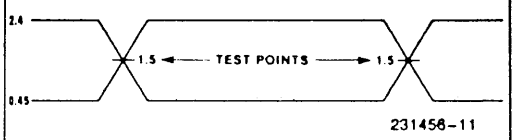
A.C. CHARACTERISTICS (Continued)

TIMING RESPONSES

Symbol	Parameter	8088		8088-2		Units	Test Conditions
		Min	Max	Min	Max		
TCLAV	Address Valid Delay	10	110	10	60	ns	
TCLAX	Address Hold Time	10		10		ns	
TCLAZ	Address Float Delay	TCLAX	80	TCLAX	50	ns	
TLHLL	ALE Width	TCLCH−20		TCLCH−10		ns	
TCLLH	ALE Active Delay		80		50	ns	
TCHLL	ALE Inactive Delay		85		55	ns	
TLLAX	Address Hold Time to ALE Inactive	TCHCL−10		TCHCL−10		ns	
TCLDV	Data Valid Delay	10	110	10	60	ns	
TCHDX	Data Hold Time	10		10		ns	
TWHDX	Data Hold Time after $\overline{WR}$	TCLCH−30		TCLCH−30		ns	
TCVCTV	Control Active Delay 1	10	110	10	70	ns	
TCHCTV	Control Active Delay 2	10	110	10	60	ns	
TCVCTX	Control Inactive Delay	10	110	10	70	ns	
TAZRL	Address Float to READ Active	0		0		ns	
TCLRL	$\overline{RD}$ Active Delay	10	165	10	100	ns	
TCLRH	$\overline{RD}$ Inactive Delay	10	150	10	80	ns	
TRHAV	$\overline{RD}$ Inactive to Next Address Active	TCLCL−45		TCLCL−40		ns	
TCLHAV	HLDA Valid Delay	10	160	10	100	ns	
TRLRH	$\overline{RD}$ Width	2TCLCL−75		2TCLCL−50		ns	
TWLWH	$\overline{WR}$ Width	2TCLCL−60		2TCLCL−40		ns	
TAVAL	Address Valid to ALE Low	TCLCH−60		TCLCH−40		ns	
TOLOH	Output Rise Time		20		20	ns	From 0.8V to 2.0V
TOHOL	Output Fall Time		12		12	ns	From 2.0V to 0.8V

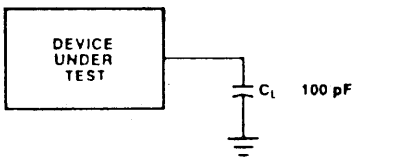
NOTES:
1. Signal at 8284A shown for reference only. See 8284A data sheet for the most recent specifications.
2. Set up requirement for asynchronous signal only to guarantee recognition at next CLK.
3. Applies only to T2 state (8 ns into T3 state).

A.C. TESTING INPUT, OUTPUT WAVEFORM



A.C. Testing; Inputs are driven at 2.4V for a logic "1" and 0.45V for a logic "0". Timing measurements are made at 2.0V for a logic "1" and 0.8V for a logic "0".

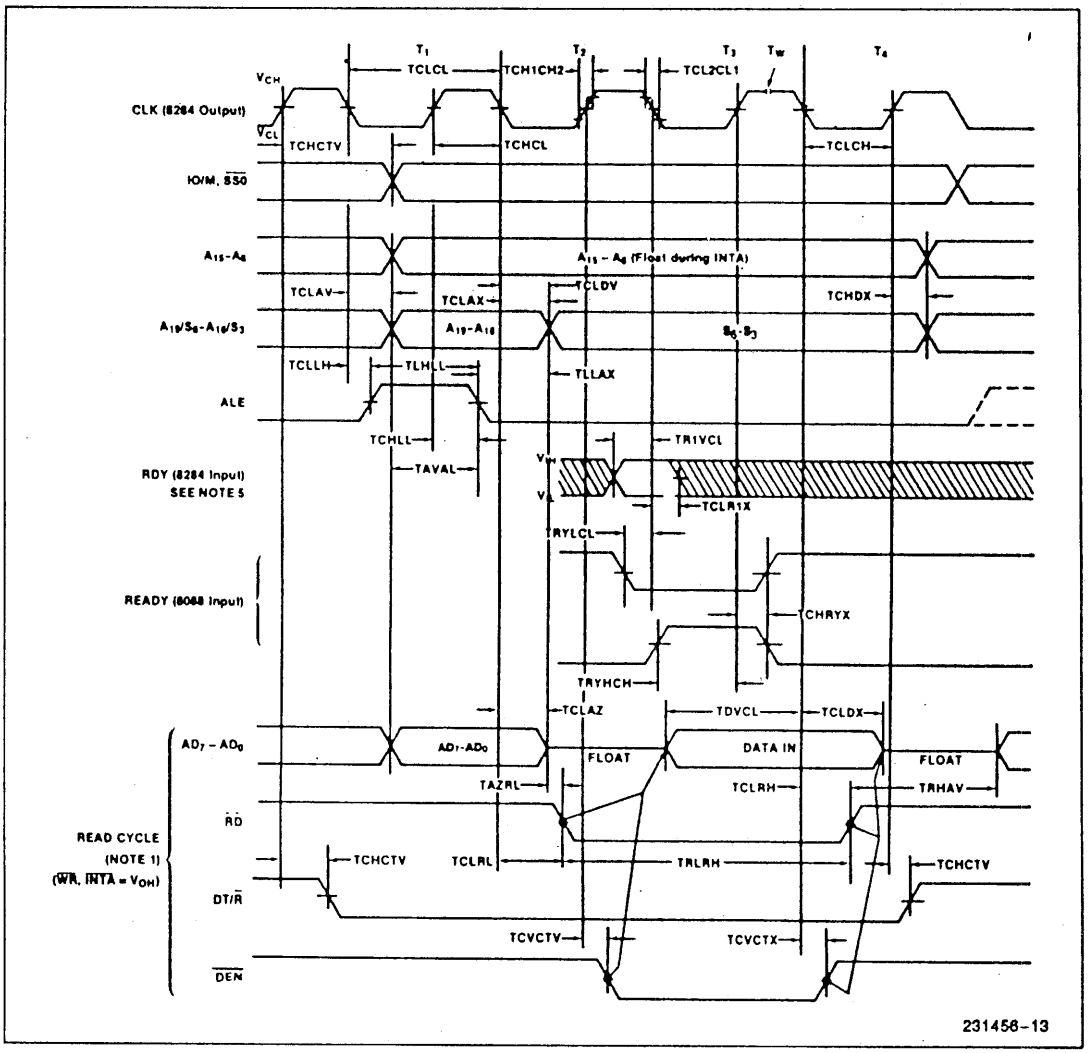
A.C. TESTING LOAD CIRCUIT



C_L Includes Jig Capacitance

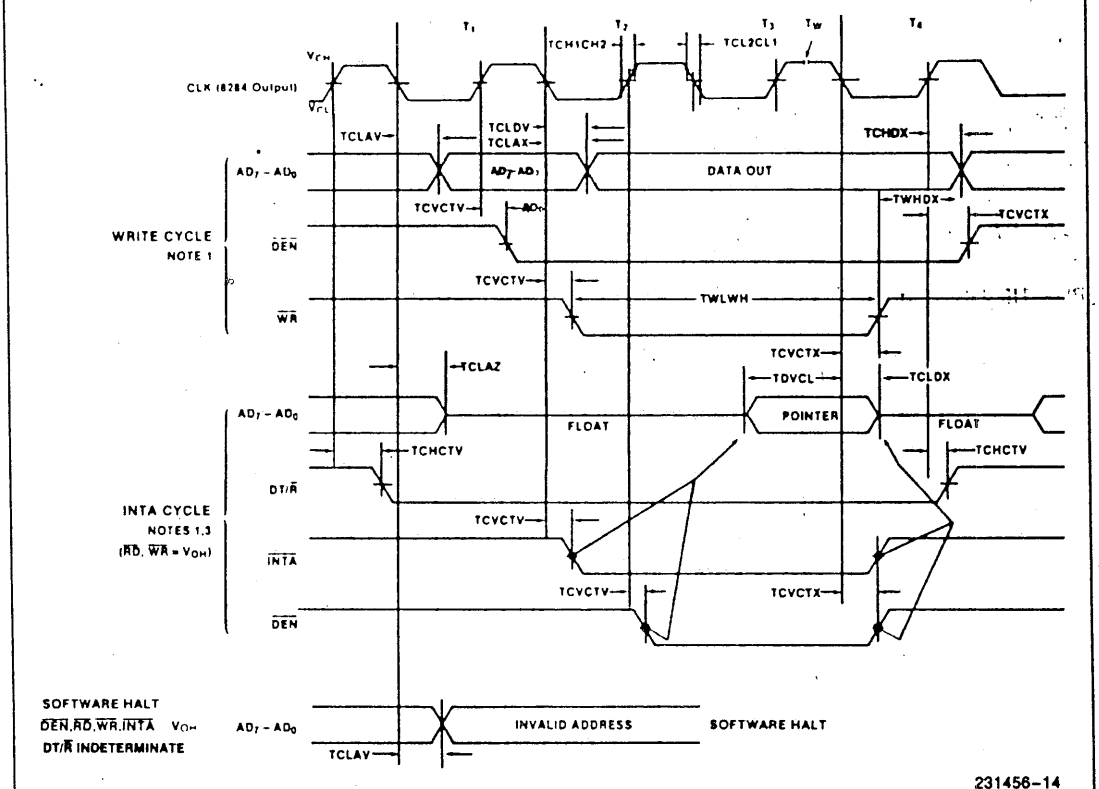
WAVEFORMS

BUS TIMING—MINIMUM MODE SYSTEM



WAVEFORMS (Continued)

BUS TIMING—MINIMUM MODE SYSTEM (Continued)



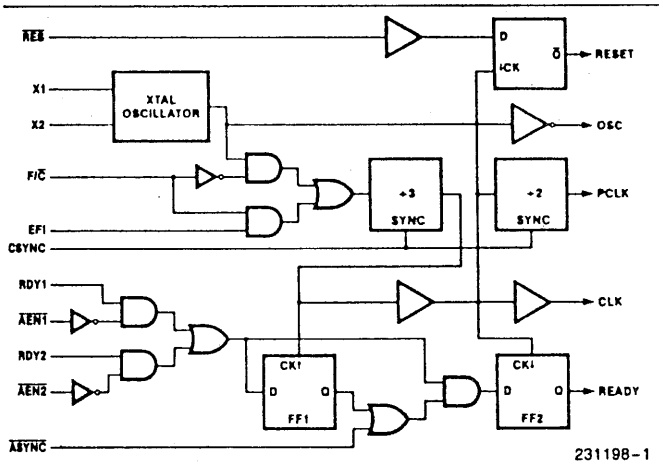
NOTES:
1. All signals switch between V_{OH} and V_{OL} unless otherwise specified.
2. RDY is sampled near the end of T_2, T_3, T_w to determine if T_w machines states are to be inserted.
3. Two INTA cycles run back-to-back. The 8088 local ADDR/DATA bus is floating during both INTA cycles. Control signals are shown for the second INTA cycle.
4. Signals at 8284 are shown for reference only.
5. All timing measurements are made at 1.5V unless otherwise noted.

82C84A
CHMOS CLOCK GENERATOR AND DRIVER FOR 80C86, 80C88 PROCESSORS

- Generates the System Clock for the 80C86, 80C88 Processors:
  - 82C84A-5 for 5 MHz
  - 82C84A for 8 MHz
- Pin Compatible with Bipolar 8284A*
- Uses a Crystal or an External Frequency Source
- Provides Local READY and MULTIBUS® READY Synchronization
- Generates System Reset Output from Schmitt Trigger Input
- Capable of Clock Synchronization with other 82C84As
- Low Power Consumption
- Single 5V Power Supply
- TTL Compatible Inputs/Outputs
- Available in 18-Lead Plastic DIP
  (See Packaging Spec., Order # 231369)

The Intel 82C84A is a high performance CHMOS clock generator-driver designed to service the requirements of the 80C86/88 and 8086/88. Power consumption is a fraction of that of equivalent bipolar circuits. The chip contains a crystal controlled oscillator, a divide-by-three counter and complete READY synchronization and reset logic. Crystal controlled operation up to 15, 25 MHz utilizes a parallel, fundamental mode crystal and two small load capacitors.

*The Bipolar 8284A requires two load resistors and a resonant crystal.

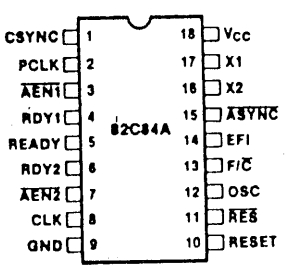


231198-1

82C84A Block Diagram

Control Pin	Logical 1	Logical 0
F/$\overline{C}$	External Clock	Crystal Drive
$\overline{RES}$	Normal	Reset
RDY 1 RDY 2	Bus Ready	Bus not ready
$\overline{AEN\ 1}$ $\overline{AEN\ 2}$	Address Disabled	Address Enabled
$\overline{ASYNC}$	1 Stage Ready Synchronization	2 Stage Ready Synchronization

82C84A Pin Description



231198-2

82C84A 18-Lead DIP Configuration

Table 1. Pin Description

Symbol	Type	Name and Function
$\overline{AEN1}$, $\overline{AEN2}$	I	**ADDRESS ENABLE:** $\overline{AEN}$ is an active LOW signal. AEN serves to qualify its repective Bus Ready Signal (RDY1 or RDY2). $\overline{AEN1}$ validates RDY1 while $\overline{AEN2}$ validates RDY2. Two AEN signal inputs are useful in system configurations which permit the processor to access two Multi-Master System Busses. In non Multi-Master configurations the $\overline{AEN}$ signal inputs are tied true (LOW).
RDY1, RDY2	I	**BUS READY:** (Transfer Complete). RDY is an active HIGH signal which is an indication from a device located on the system data bus that data has been received, or is available. RDY1 is qualified by $\overline{AEN1}$ while RDY2 is qualified by $\overline{AEN2}$.
$\overline{ASYNC}$	I	**READY SYNCHRONIZATION SELECT:** $\overline{ASYNC}$ is an input which defines the synchronization mode of the READY logic. When $\overline{ASYNC}$ is LOW, two stages of READY synchronization are provided. When $\overline{ASYNC}$ is left open (an internal pull-up is provided) or HIGH a single stage of READY synchronization is provided.
READY	O	**READY:** READY is an active HIGH signal which is the synchronized RDY signal input. READY is cleared after the guaranteed hold time to the processor has been met.
X1, X2	I	**CRYSTAL IN:** X1 and X2 are the pins to which a crystal is attached. The crystal frequency is 3 times the desired processor clock frequency. (If no crystal is attached, then X1 should be tied to V_{CC} or GND and X2 should be left open.)
F/$\overline{C}$	I	**FREQUENCY/CRYSTAL SELECT:** F/$\overline{C}$ is a strapping option. When strapped LOW, F/$\overline{C}$ permits the processor's clock to be generated by the crystal. When F/$\overline{C}$ is strapped HIGH, CLK is generated from the EFI input.
EFI	I	**EXTERNAL FREQUENCY:** When F/$\overline{C}$ is strapped HIGH, CLK is generated from the input frequency appearing on this pin. The input signal is a square wave 3 times the frequency of the desired CLK output. When F/$\overline{C}$ is strapped LOW, EFI should be tied HIGH or LOW.
CLK	O	**PROCESSOR CLOCK:** CLK is the clock output used by the processor and all devices which directly connect to the processor's local bus (i.e., the bipolar support chips and other MOS devices). CLK has an output frequency which is ⅓ of the crystal or EFI input frequency and a ⅓ duty cycle.
PCLK	O	**PERIPHERAL CLOCK:** PCLK is a TTL level peripheral clock signal whose output frequency is ½ that of CLK and has a 50% duty cycle.
OSC	O	**OSCILLATOR OUTPUT:** OSC is the TTL level output of the internal oscillator circuitry. Its frequency is equal to that of the crystal.
$\overline{RES}$	I	**RESET IN:** $\overline{RES}$ is an active LOW signal which is used to generate RESET. The 82C84A provides a Schmitt trigger input so that an RC connection can be used to establish the power-up reset of proper duration.

Table 1. Pin Description (Continued)

Symbol	Type	Name and Function
RESET	O	**RESET:** RESET is an active HIGH signal which is used to reset the 80C86/88 family processors. Its timing characteristics are determined by $\overline{RES}$.
CSYNC	I	**CLOCK SYNCHRONIZATION:** CSYNC is an active HIGH signal which allows multiple 82C84A's to be synchronized to provide clocks that are in phase. When CSYNC is HIGH the internal counters are reset. When CSYNC goes LOW the internal counters are allowed to resume counting. CSYNC needs to be externally synchronized to EFI. When using the internal oscillator CSYNC should be hardwired to ground.
GND		**GROUND.**
V_{CC}		**POWER:** +5V supply.

FUNCTIONAL DESCRIPTION

Oscillator

The oscillator circuit of the 82C84A is designed primarily for use with an external parallel resonant, fundamental mode crystal from which the basic operating frequency is derived.

The crystal frequency should be selected at three times the required CPU clock. X1 and X2 are the two crystal input crystal connections. For the most stable operation of the oscillator (OSC) output circuit, two capacitors (C1 = C2) as shown in the waveform figures are recommended. The output of the oscillator is buffered and brought out on OSC so that other system timing signals can be derived from this stable, crystal-controlled source.

Capacitors C1, C2 are chosen such that their combined capacitance:

$$CT = \frac{C1 \bullet C2}{C1 + C2}$$ (Including stray capacitance)

matches the load capacitance as specified by the crystal manufacturer. This insures operation within the frequency tolerance specified by the crystal manufacturer.

Clock Generator

The clock generator consists of a synchronous divide-by-three counter with a special clear input that inhibits the counting. This clear input (CSYNC) allows the output clock to be synchronized with an external event (such as another 82C84A clock). It is necessary to synchronize the CSYNC input to the EFI clock external to the 82C84A. This is accomplished with two Schottky flip-flops. The counter output is a 33% duty cycle clock at one-third the input frequency.

The F/$\overline{C}$ input is a strapping pin that selects either the crystal oscillator or the EFI input as the clock for the ÷3 counter. If the EFI input is selected as the clock source, the oscillator section can be used independently for another clock source. Output is taken from OSC.

Clock Outputs

The CLK ouput is a 33% duty cycle MOS clock driver designed to drive the 80C86/88 processors directly. PCLK is a TTL level peripheral clock signal whose output frequency is ½ that of CLK. PCLK has a 50% duty cycle.

Reset Logic

The reset logic provides a Schmitt trigger input ($\overline{RES}$) and a synchronizing flip-flop to generate the reset timing. The reset signal is synchronized to the falling edge of CLK. A simple RC network can be used to provide power-on reset by utilizing this function of the 82C84A.

READY Synchronization

Two READY inputs (RDY1, RDY2) are provided to accommodate two Multi-Master system busses. Each input has a qualifier ($\overline{AEN1}$ and $\overline{AEN2}$, respectively). The $\overline{AEN}$ signals validate their respective RDY signals. If a Multi-Master system is not being used the $\overline{AEN}$ pin should be tied LOW.

D.C. CHARACTERISTICS (Continued)

Symbol	Parameter	Min	Max	Units	Test Conditions
V_{IL}	Input LOW Voltage		0.8	V	
V_{IH}	Input HIGH Voltage	2.2	V_{CC} + 0.5	V	
V_{IHR}	Reset Input HIGH Voltage	0.6 V_{CC}		V	
V_{OL}	Output LOW Voltage		0.4	V	CLK: I_{OL} = 4 mA Others: I_{OL} = 2.5 mA
V_{OH}	Output HIGH Voltage	V_{CC} − 0.4		V V	CLK: I_{OH} = −4 mA Others: I_{OH} = −2.5 mA
V_{IHR}-V_{ILR}	$\overline{RES}$ Input Hysteresis: 82C84A 82C84A-5	0.15 0.25		V V	
C_{IN}	Input Capacitance		7	pF	freq = 1 MHz

NOTES:
1. V_{IH}, F/$\overline{C}$, X1 ≥ V_{CC} − 0.2V; EFI = V_{CC} or GND; ASYNC = V_{CC} or OPEN; X2 = OPEN; V_{IL} ≤ 0.2V.
2. An internal pull-up resistor is implemented on the $\overline{ASYNC}$ input.

A.C. CHARACTERISTICS (T_A = 0°C to +70°C, V_{CC} = 5V ±10%)

TIMING REQUIREMENTS

Symbol	Parameter	82C84A		82C84A-5		Units	Test Conditions
		Min	Max	Min	Max		
t_{EHEL}	External Frequency HIGH Time	13		20		ns	90%–90% V_{IN}
t_{ELEH}	External Frequency LOW Time	13		20		ns	10%–10% V_{IN}
t_{ELEL}	EFI Period	40		66		ns	(Note 1)
	XTAL Frequency	2.4	25	6.0	15	MHz	
t_{R1VCL}	RDY1, RDY2 Active Setup to CLK	35		35		ns	$\overline{ASYNC}$ = HIGH
t_{R1VCH}	RDY1, RDY2 Active Setup to CLK	35		35		ns	$\overline{ASYNC}$ = LOW
t_{R1VCL}	RDY1, RDY2 Inactive Setup to CLK	35		35		ns	
t_{CLR1X}	RDY1, RDY2 Hold to CLK	0		0		ns	
t_{AYVCL}	$\overline{ASYNC}$ Setup to CLK	50		50		ns	
t_{CLAYX}	$\overline{ASYNC}$ Hold to CLK	0		0		ns	
t_{A1VR1V}	$\overline{AEN1}$, $\overline{AEN2}$ Setup to RDY1, RDY2	15		15		ns	
t_{CLA1X}	$\overline{AEN1}$, $\overline{AEN2}$ Hold to CLK	0		0		ns	
t_{YHEH}	CSYNC Setup to EFI	20		20		ns	
t_{EHYL}	CSYNC Hold to EFI	10		20		ns	
t_{YHYL}	CSYNC Width	2 • t_{ELEL}		2 • t_{ELEL}		ns	
t_{I1HCL}	$\overline{RES}$ Setup to CLK	65		65		ns	(Note 2)
t_{CLI1H}	$\overline{RES}$ Hold to CLK	20		20		ns	(Note 2)
t_{ILIH}	Input Rise Time		15		15	ns	(Note 1)
t_{IHIL}	Input Fall Time		15		15	ns	(Note 1)

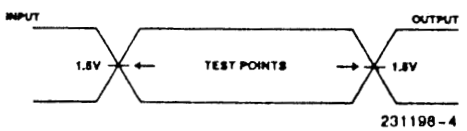
A.C. CHARACTERISTICS (Continued)

TIMING RESPONSES

Symbol	Parameter	Min 82C84A	Min 82C84A-5	Max	Units	Test Conditions
t_{CLCL}	CLK Cycle Period	125	200		ns	
t_{CHCL}	CLK HIGH Time	$(1/3\ t_{CLCL})+2$	$(1/3\ t_{CLCL})+2$		ns	
t_{CLCH}	CLK LOW Time	$(2/3\ t_{CLCL})-15$	$(2/3\ t_{CLCL})-15$		ns	
t_{CH1CH2} t_{CL2CL1}	CLK Rise or Fall Time			10	ns	1.0V to 3.5V
t_{PHPL}	PCLK HIGH Time	$t_{CLCL}-20$	$t_{CLCL}-20$		ns	
t_{PLPH}	PCLK LOW Time	$t_{CLCL}-20$	$t_{CLCL}-20$		ns	
t_{RYLCL}	Ready Inactive to CLK (Note 4)	−8	−8		ns	
t_{RYHCH}	Ready Active to CLK (Note 3)	$(2/3\ t_{CLCL})-15$	$(2/3\ t_{CLCL})-15$		ns	
t_{CLIL}	CLK to Reset Delay			40	ns	
t_{CLPH}	CLK to PCLK HIGH DELAY			22	ns	
t_{CLPL}	CLK to PCLK LOW Delay			22	ns	
t_{OLCH}	OSC to CLK HIGH Delay	−5	−5	22	ns	
t_{OLCL}	OSC to CLK LOW Delay	2	2	35	ns	
t_{OLOH}	Output Rise Time (except CLK)			15	ns	From 0.8V to 2.0V
t_{OHOL}	Output Fall Time (except CLK)			15	ns	From 2.0V to 0.8V

NOTES:
1. Transition between V_{IL}(max) − 0.4V and V_{IH}(min) + 0.4V.
2. Setup and hold necessary only to guarantee recognition at next clock.
3. Applies only to T3 and TW states.
4. Applies only to T2 states.

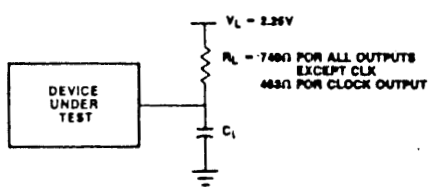
A.C. TESTING INPUT, OUTPUT WAVEFORM



231198-4

A.C. TESTING: ALL INPUT SIGNALS MUST SWITCH BETWEEN 0.45V AND 2.4V. T_{RISE} AND T_{FALL} MUST BE ≤ 15 ns.
ALL TIMING MEASUREMENTS ARE MADE AT 1.5V.

A.C. TESTING LOAD CIRCUIT



231198-5

C_L = 100 pF FOR CLK
C_L = 30 pF FOR READY
C_L INCLUDES PROBE AND JIG CAPACITANCE

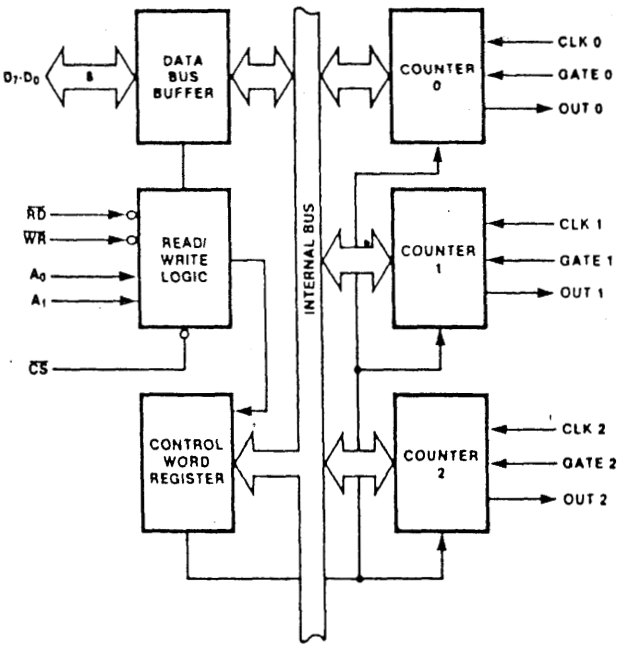
PRELIMINARY

8254
PROGRAMMABLE INTERVAL TIMER

- Compatible with All Intel and Most Other Microprocessors
- Handles Inputs from DC to 10 MHz
  - 5 MHz 8254-5
  - 8 MHz 8254
  - 10 MHz 8254-2
- Status Read-Back Command
- Six Programmable Counter Modes
- Three Independent 16-Bit Counters
- Binary or BCD Counting
- Single +5V Supply
- Available in EXPRESS
  - Standard Temperature Range

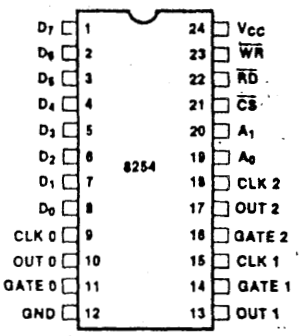
The Intel® 8254 is a counter/timer device designed to solve the common timing control problems in microcomputer system design. It provides three independent 16-bit counters, each capable of handling clock inputs up to 10 MHz. All modes are software programmable. The 8254 is a superset of the 8253.

The 8254 uses HMOS technology and comes in a 24-pin plastic or CERDIP package.



231164-1

Figure 1. 8254 Block Diagram



231164-2

Figure 2. Pin Configuration

Table 1. Pin Description

Symbol	Pin No.	Type	Name and Function
D_7-D_0	1-8	I/O	**DATA:** Bi-directional three state data bus lines, connected to system data bus.
CLK 0	9	I	**CLOCK 0:** Clock input of Counter 0.
OUT 0	10	O	**OUTPUT 0:** Output of Counter 0.
GATE 0	11	I	**GATE 0:** Gate input of Counter 0.
GND	12		**GROUND:** Power supply connection.
V_{CC}	24		**POWER:** +5V power supply connection.
$\overline{WR}$	23	I	**WRITE CONTROL:** This input is low during CPU write operations.
$\overline{RD}$	22	I	**READ CONTROL:** This input is low during CPU read operations.
$\overline{CS}$	21	I	**CHIP SELECT:** A low on this input enables the 8254 to respond to $\overline{RD}$ and $\overline{WR}$ signals. $\overline{RD}$ and $\overline{WR}$ are ignored otherwise.
A_1, A_0	20-19	I	**ADDRESS:** Used to select one of the three Counters or the Control Word Register for read or write operations. Normally connected to the system address bus.

A_1	A_0	Selects
0	0	Counter 0
0	1	Counter 1
1	0	Counter 2
1	1	Control Word Register

CLK 2	18	I	**CLOCK 2:** Clock input of Counter 2.
OUT 2	17	O	**OUT 2:** Output of Counter 2.
GATE 2	16	I	**GATE 2:** Gate input of Counter 2.
CLK 1	15	I	**CLOCK 1:** Clock input of Counter 1.
GATE 1	14	I	**GATE 1:** Gate input of Counter 1.
OUT 1	13	O	**OUT 1:** Output of Counter 1.

FUNCTIONAL DESCRIPTION

General

The 8254 is a programmable interval timer/counter designed for use with Intel microcomputer systems. It is a general purpose, multi-timing element that can be treated as an array of I/O ports in the system software.

The 8254 solves one of the most common problems in any microcomputer system, the generation of accurate time delays under software control. Instead of setting up timing loops in software, the programmer configures the 8254 to match his requirements and programs one of the counters for the desired delay. After the desired delay, the 8254 will interrupt the CPU. Software overhead is minimal and variable length delays can easily be accommodated.

Some of the other counter/timer functions common to microcomputers which can be implemented with the 8254 are:

- Real time clock
- Event-counter
- Digital one-shot
- Programmable rate generator
- Square wave generator
- Binary rate multiplier
- Complex waveform generator
- Complex motor controller

Block Diagram

DATA BUS BUFFER

This 3-state, bi-directional, 8-bit buffer is used to interface the 8254 to the system bus (see Figure 3).

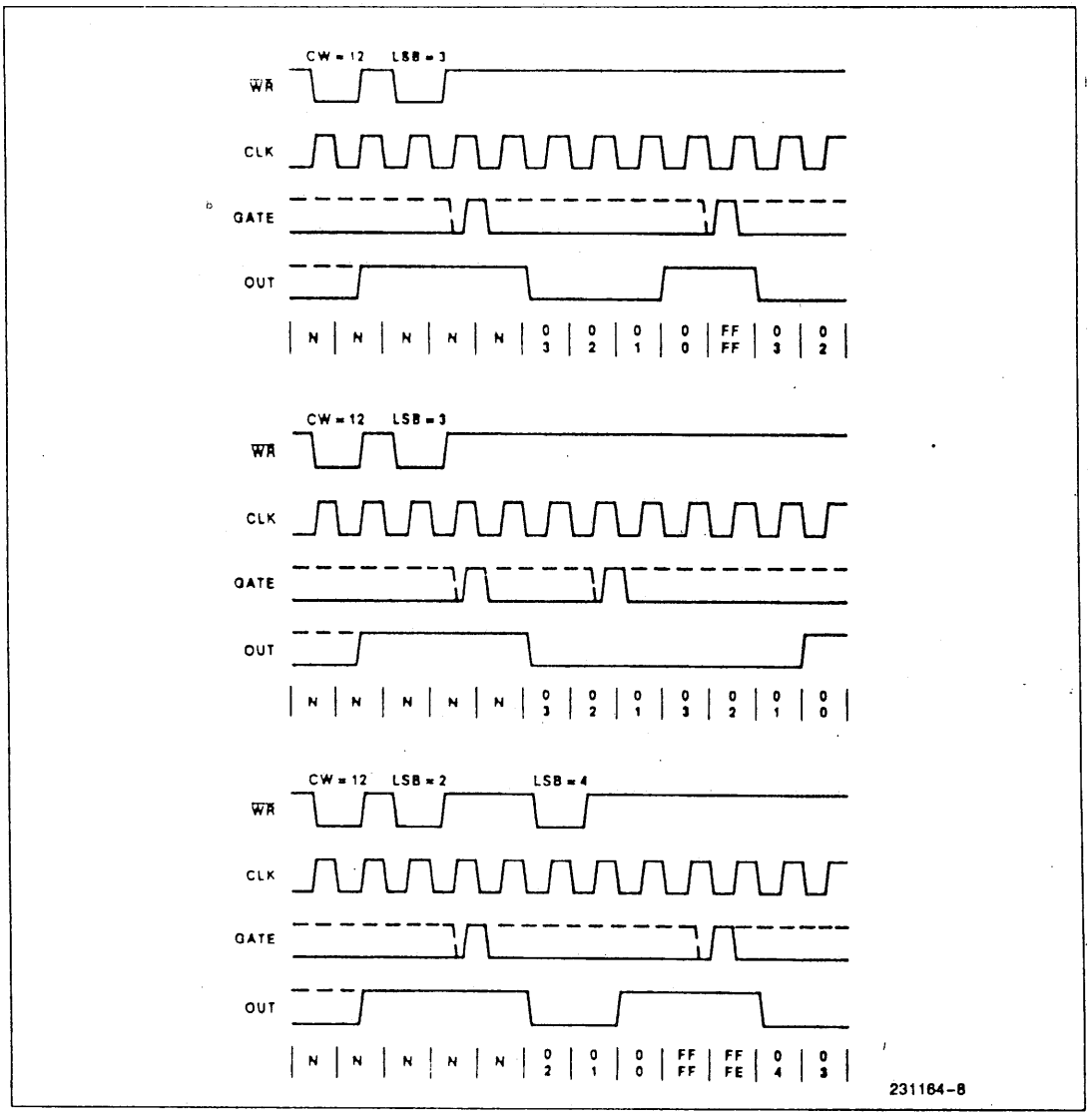


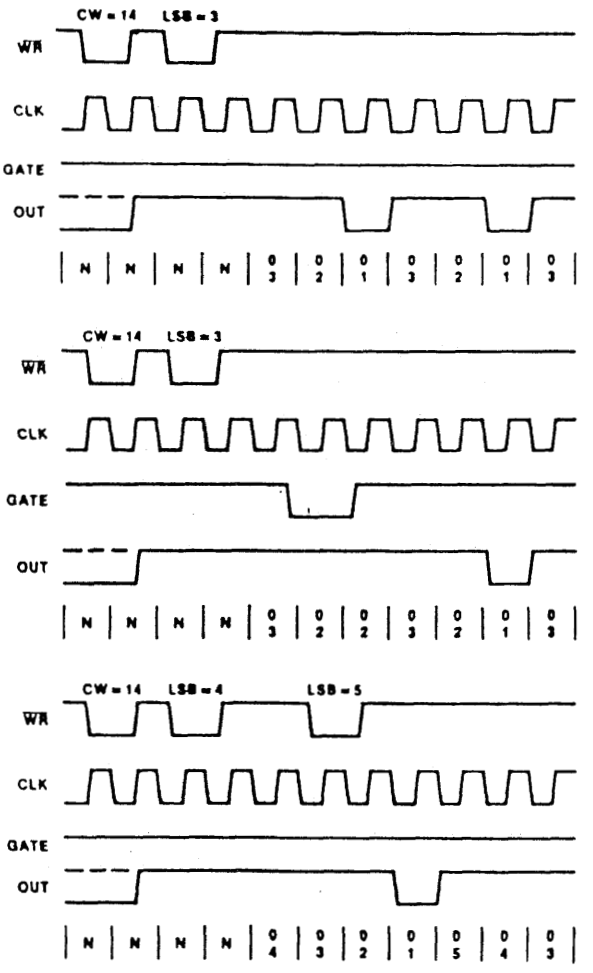
Figure 16. Mode 1

initial count has expired, OUT goes low for the remainder of the count. Mode 3 is periodic; the sequence above is repeated indefinitely. An initial count of N results in a square wave with a period of N CLK cycles.

GATE = 1 enables counting; GATE = 0 disables counting. If GATE goes low while OUT is low, OUT is set high immediately; no CLK pulse is required. A trigger reloads the Counter with the initial count on the next CLK pulse. Thus the GATE input can be used to synchronize the Counter.

After writing a Control Word and initial count, the Counter will be loaded on the next CLK pulse. This allows the Counter to be synchronized by software also.

Writing a new count while counting does not affect the current counting sequence. If a trigger is received after writing a new count but before the end of the current half-cycle of the square wave, the Counter will be loaded with the new count on the next CLK pulse and counting will continue from the



NOTE:
A GATE transition should not occur one clock prior to terminal count.

Figure 17. Mode 2

new count. Otherwise, the new count will be loaded at the end of the current half-cycle.

Mode 3 is implemented as follows:

Even counts: OUT is initially high. The initial count is loaded on one CLK pulse and then is decremented by two on succeeding CLK pulses. When the count expires OUT changes value and the Counter is reloaded with the initial count. The above process is repeated indefinitely.

Odd counts: OUT is initially high. The initial count minus one (an even number) is loaded on one CLK pulse and then is decremented by two on succeeding CLK pulses. One CLK pulse *after* the count expires, OUT goes low and the Counter is reloaded with the initial count minus one. Succeeding CLK pulses decrement the count by two. When the count expires, OUT goes high again and the Counter is reloaded with the initial count minus one. The above process is repeated indefinitely. So for odd counts, OUT will be high for $(N + 1)/2$ counts and low for $(N - 1)/2$ counts.

ABSOLUTE MAXIMUM RATINGS*

Ambient Temperature Under Bias .....0°C to 70°C
Storage Temperature .....−65°C to +150°C
Voltage on Any Pin with Respect to Ground.....−0.5V to +7V
Power Dissipation 1W

Notice: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

NOTICE: Specifications contained within the following tables are subject to change.

D.C. CHARACTERISTICS T_A = 0°C to 70°C, V_{CC} = 5V ±10%

Symbol	Parameter	Min	Max	Units	Test Conditions
V_{IL}	Input Low Voltage	−0.5	0.8	V	
V_{IH}	Input High Voltage	2.0	V_{CC} +0.5V	V	
V_{OL}	Output Low Voltage		0.45	V	I_{OL} = 2.0 mA
V_{OH}	Output High Voltage	2.4		V	I_{OH} = −400 μA
I_{IL}	Input Load Current		±10	μA	V_{IN} = V_{CC} to 0V
I_{OFL}	Output Float Leakage		±10	μA	V_{OUT} = V_{CC} to 0.45V
I_{CC}	V_{CC} Supply Current		170	mA	

CAPACITANCE T_A = 25°C, V_{CC} = GND = 0V

Symbol	Parameter	Min	Max	Units	Test Conditions
C_{IN}	Input Capacitance		10	pF	f_c = 1 MHz
$C_{I/O}$	I/O Capacitance		20	pF	Unmeasured pins returned to V_{SS}

A.C. CHARACTERISTICS T_A = 0°C to 70°C, V_{CC} = 5V ±10%, GND = 0V

Bus Parameters(1)

READ CYCLE

Symbol	Parameter	8254-5		8254		8254-2		Unit
		Min	Max	Min	Max	Min	Max	
t_{AR}	Address Stable Before $\overline{RD}$ ↓	45		45		30		ns
t_{SR}	$\overline{CS}$ Stable Before $\overline{RD}$ ↓	0		0		0		ns
t_{RA}	Address Hold Time After $\overline{RD}$ ↑	0		0		0		ns
t_{RR}	$\overline{RD}$ Pulse Width	150		150		95		ns
t_{RD}	Data Delay from $\overline{RD}$ ↓		120		120		85	ns
t_{AD}	Data Delay from Address		220		220		185	ns
t_{DF}	$\overline{RD}$ ↑ to Data Floating	5	90	5	90	5	65	ns
t_{RV}	Command Recovery Time	200		200		165		ns

NOTE:
1. AC timings measured at V_{OH} = 2.0V, V_{OL} = 0.8V.

A.C. CHARACTERISTICS T_A = 0°C to 70°C, V_{CC} = 5V ± 10%, GND = 0V (Continued)

WRITE CYCLE

Symbol	Parameter	8254-5		8254		8254-2		Unit
		Min	Max	Min	Max	Min	Max	
t_{AW}	Address Stable Before $\overline{WR}$ ↓	0		0		0		ns
t_{SW}	$\overline{CS}$ Stable Before $\overline{WR}$ ↓	0		0		0		ns
$t_{\overline{WA}}$	Address Hold Time After $\overline{WR}$ ↓	0		0		0		ns
t_{WW}	$\overline{WR}$ Pulse Width	150		150		95		ns
t_{DW}	Data Setup Time Before $\overline{WR}$ ↑	120		120		95		ns
t_{WD}	Data Hold Time After $\overline{WR}$ ↑	0		0		0		ns
t_{RV}	Command Recovery Time	200		200		165		ns

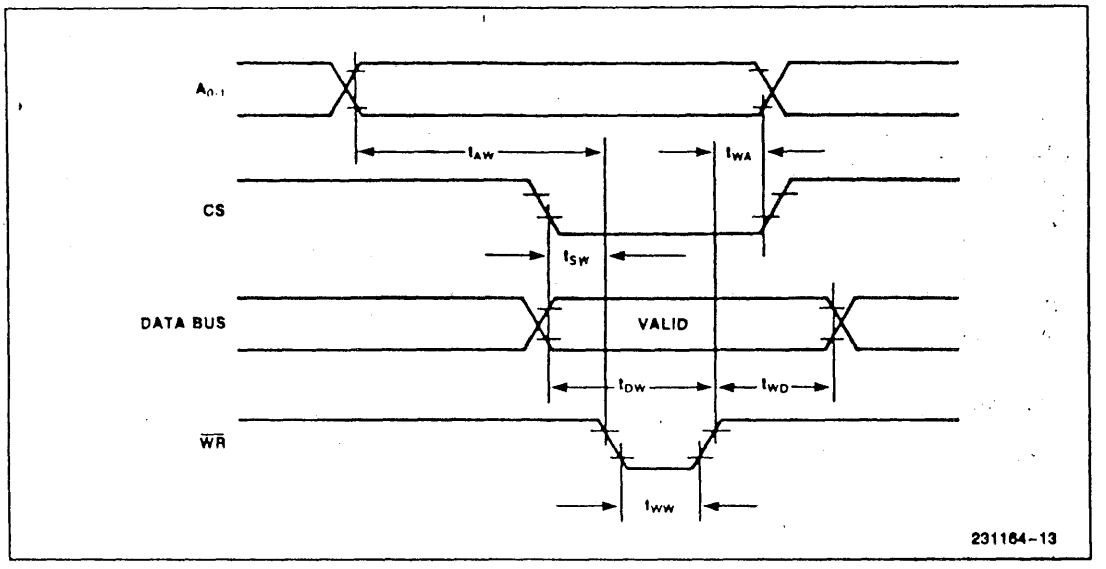
CLOCK AND GATE

Symbol	Parameter	8254-5		8254		8254-2		Unit
		Min	Max	Min	Max	Min	Max	
t_{CLK}	Clock Period	200	DC	125	DC	100	DC	ns
t_{PWH}	High Pulse Width	60(3)		60(3)		30(3)		ns
t_{PWL}	Low Pulse Width	60(3)		60(3)		50(3)		ns
t_R	Clock Rise Time		25		25		25	ns
t_F	Clock Fall Time		25		25		25	ns
t_{GW}	Gate Width High	50		50		50		ns
t_{GL}	Gate Width Low	50		50		50		ns
t_{GS}	Gate Setup Time to CLK ↑	50		50		40		ns
t_{GH}	Gate Setup Time After CLK ↑	50(2)		50(2)		50(2)		ns
t_{OD}	Output Delay from CLK ↓		150		150		100	ns
t_{ODG}	Output Delay from Gate ↓		120		120		100	ns
t_{WC}	CLK Delay for Loading ↓	0	55	0	55	0	55	ns
t_{WG}	Gate Delay for Sampling	−5	50	−5	50	−5	40	ns
t_{WO}	OUT Delay from Mode Write		260		260		240	ns
t_{CL}	CLK Set Up for Count Latch	−40	45	−40	45	−40	40	ns

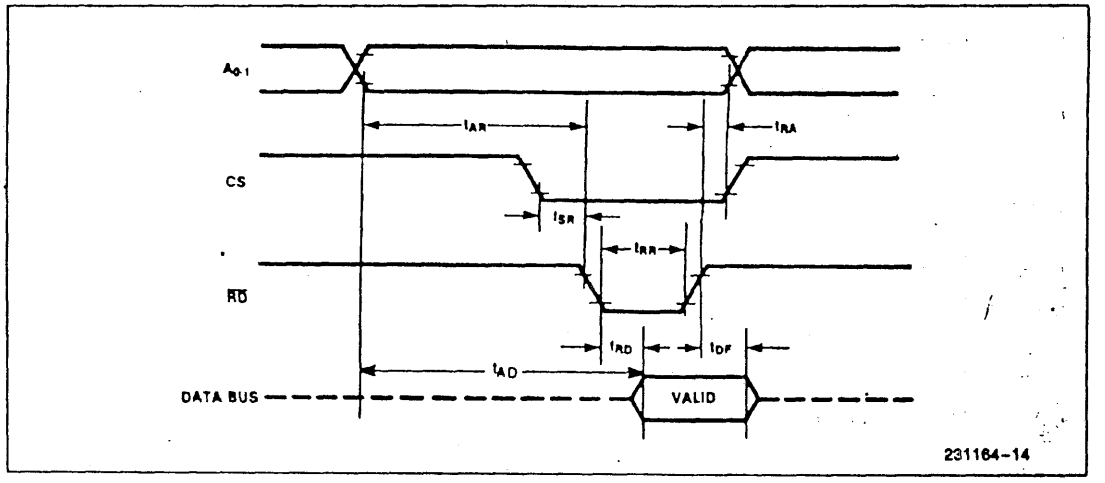
NOTES:
2. In Modes 1 and 5 triggers are sampled on each rising clock edge. A second trigger within 120 ns (70 ns for the 8254-2) of the rising clock edge may not be detected.
3. Low-going glitches that violate t_{PWH}, t_{PWL} may cause errors requiring counter reprogramming.

WAVEFORMS

WRITE

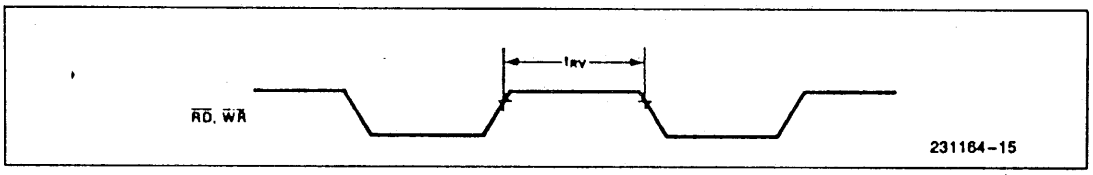


READ

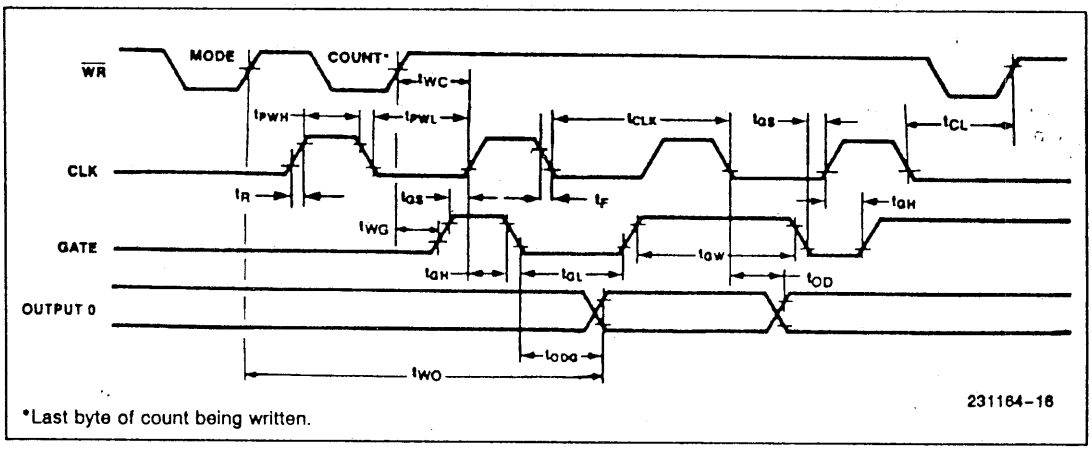


WAVEFORMS (Continued)

RECOVERY

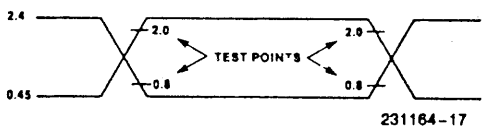


CLOCK AND GATE



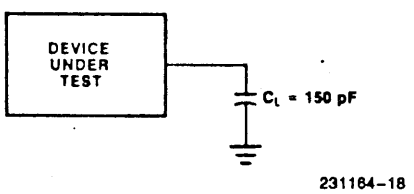
*Last byte of count being written.

A.C. TESTING INPUT, OUTPUT WAVEFORM



A.C. Testing: Inputs are driven at 2.4V for a Logic "1" and 0.45V for a Logic "0." Timing measurements are made at 2.0V for a Logic "1" and 0.8V for a Logic "0".

A.C. TESTING LOAD CIRCUIT



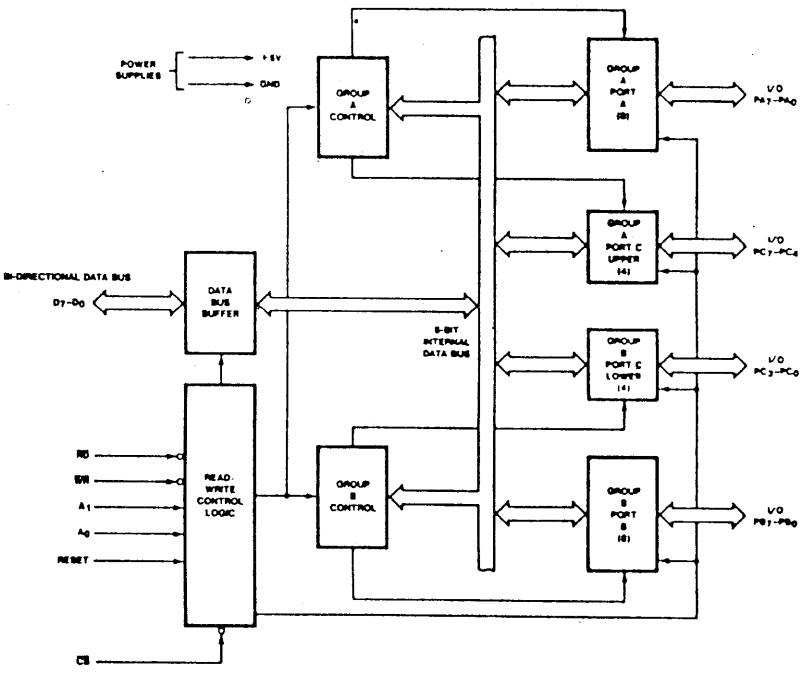
C_L = 150 pF
C_L Includes Jig Capacitance

8255A/8255A-5
PROGRAMMABLE PERIPHERAL INTERFACE

- MCS-85™ Compatible 8255A-5
- 24 Programmable I/O Pins
- Completely TTL Compatible
- Fully Compatible with Intel Microprocessor Families
- Improved Timing Characteristics
- Direct Bit Set/Reset Capability Easing Control Application Interface
- Reduces System Package Count
- Improved DC Driving Capability
- Available in EXPRESS
  - Standard Temperature Range
  - Extended Temperature Range
- 40 Pin DIP Package or 44 Lead PLCC

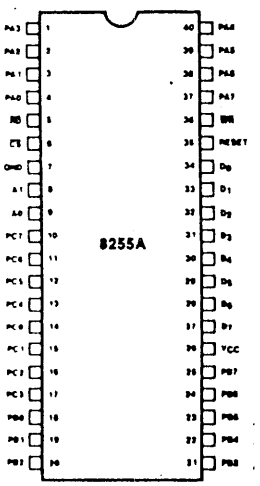
(See Intel Packaging: Order Number: 231369)

The Intel 8255A is a general purpose programmable I/O device designed for use with Intel microprocessors. It has 24 I/O pins which may be individually programmed in 2 groups of 12 and used in 3 major modes of operation. In the first mode (MODE 0), each group of 12 I/O pins may be programmed in sets of 4 to be input or output. In MODE 1, the second mode, each group may be programmed to have 8 lines of input or output. Of the remaining 4 pins, 3 are used for handshaking and interrupt control signals. The third mode of operation (MODE 2) is a bidirectional bus mode which uses 8 lines for a bidirectional bus, and 5 lines, borrowing one from the other group, for handshaking.



231308-1

Figure 1. 8255A Block Diagram



231308-2

Figure 2. Pin Configuration

8255A FUNCTIONAL DESCRIPTION

General

The 8255A is a programmable peripheral interface (PPI) device designed for use in Intel microcomputer systems. Its function is that of a general purpose I/O component to interface peripheral equipment to the microcomputer system bus. The functional configuration of the 8255A is programmed by the system software so that normally no external logic is necessary to interface peripheral devices or structures.

Data Bus Buffer

This 3-state bidirectional 8-bit buffer is used to interface the 8255A to the system data bus. Data is transmitted or received by the buffer upon execution of input or output instructions by the CPU. Control words and status information are also transferred through the data bus buffer.

Read/Write and Control Logic

The function of this block is to manage all of the internal and external transfers of both Data and Control or Status words. It accepts inputs from the CPU Address and Control busses and in turn, issues commands to both of the Control Groups.

($\overline{CS}$)

Chip Select. A "low" on this input pin enables the communication between the 8255A and the CPU.

($\overline{RD}$)

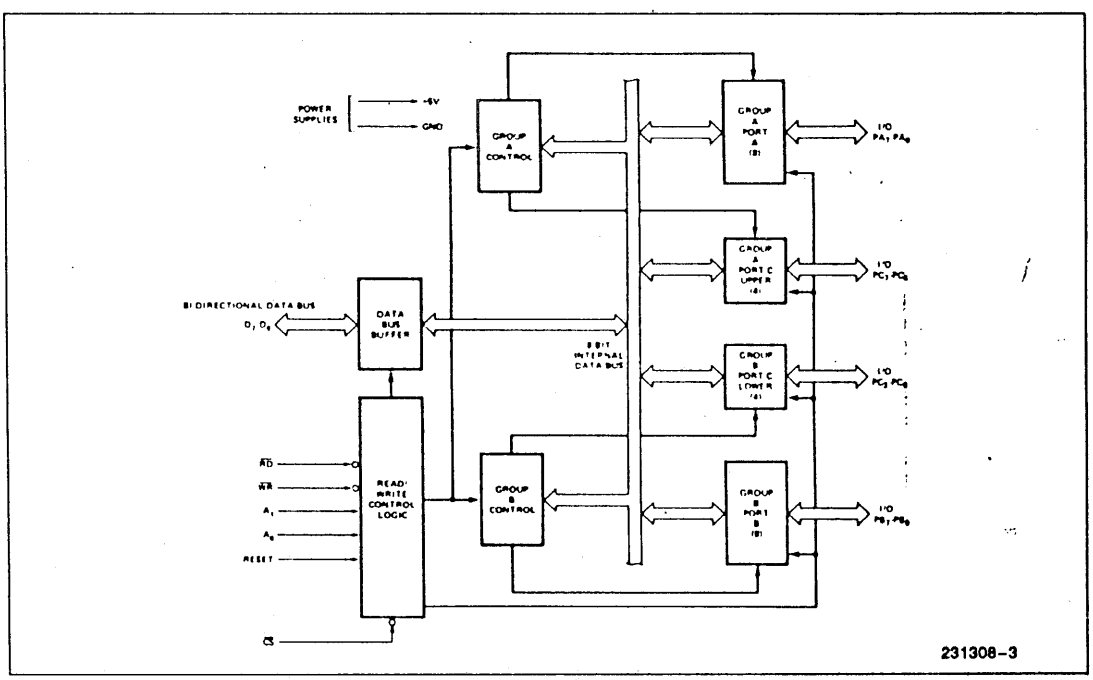
Read. A "low" on this input pin enables the 8255A to send the data or status information to the CPU on the data bus. In essence, it allows the CPU to "read from" the 8255A.

($\overline{WR}$)

Write. A "low" on this input pin enables the CPU to write data or control words into the 8255A.

(A_0 and A_1)

Port Select 0 and Port Select 1. These input signals, in conjunction with the RD and WR inputs, control the selection of one of the three ports or the control word registers. They are normally connected to the least significant bits of the address bus (A_0 and A_1).



8255A Block Diagram Showing Data Bus Buffer and Read/Write Control Logic Functions

8255A BASIC OPERATION

A_1	A_0	$\overline{RD}$	$\overline{WR}$	$\overline{CS}$	Input Operation (READ)
0	0	0	1	0	Port A → Data Bus
0	1	0	1	0	Port B → Data Bus
1	0	0	1	0	Port C → Data Bus
					Output Operation (WRITE)
0	0	1	0	0	Data Bus → Port A
0	1	1	0	0	Data Bus → Port B
1	0	1	0	0	Data Bus → Port C
1	1	1	0	0	Data Bus → Control
					Disable Function
X	X	X	X	1	Data Bus → 3-State
1	1	0	1	0	Illegal Condition
X	X	1	1	0	Data Bus → 3-State

(RESET)

Reset. A "high" on this input clears the control register and all ports (A, B, C) are set to the input mode.

Group A and Group B Controls

The functional configuration of each port is programmed by the systems software. In essence, the CPU "outputs" a control word to the 8255A. The control word contains information such as "mode", "bit set", "bit reset", etc., that initializes the functional configuration of the 8255A.

Each of the Control blocks (Group A and Group B) accepts "commands" from the Read/Write Control Logic, receives "control words" from the internal data bus and issues the proper commands to its associated ports.

Control Group A—Port A and Port C upper (C7–C4)

Control Group B—Port B and Port C lower (C3–C0)

The Control Word Register can **Only** be written into. No Read operation of the Control Word Register is allowed.

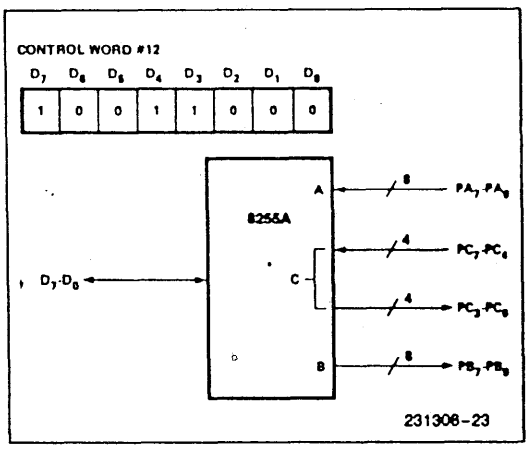
Ports A, B, and C

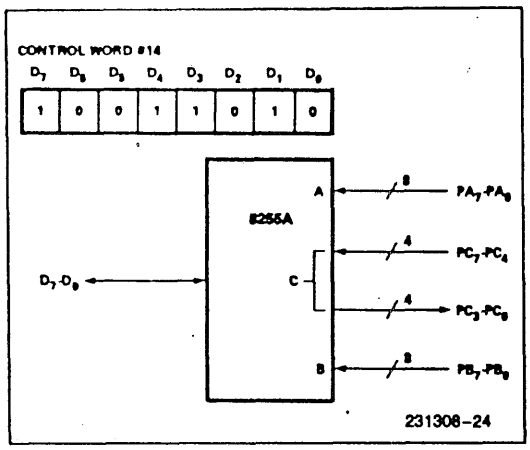
The 8255A contains three 8-bit ports (A, B, and C). All can be configured in a wide variety of functional characteristics by the system software but each has its own special features or "personality" to further enhance the power and flexibility of the 8255A.

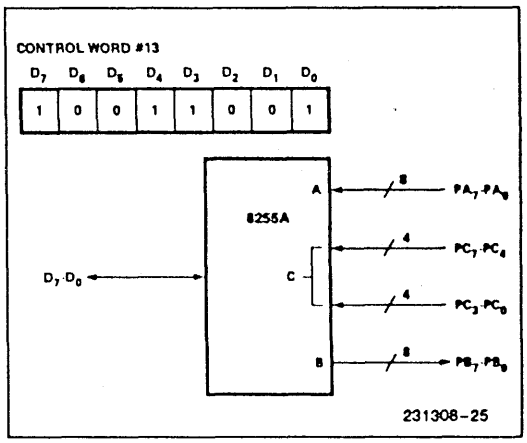
Port A. One 8-bit data output latch/buffer and one 8-bit data input latch.

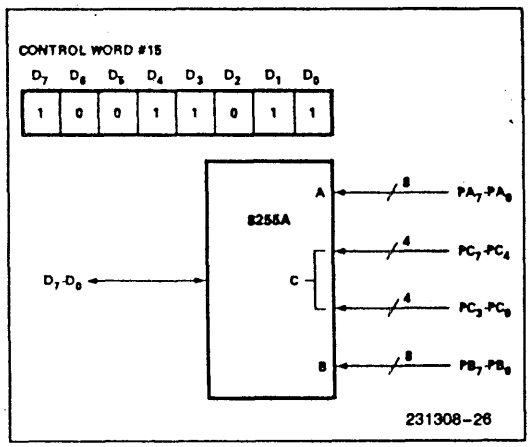
Port B. One 8-bit data input/output latch/buffer and one 8-bit data input buffer.

Port C. One 8-bit data output latch/buffer and one 8-bit data input buffer (no latch for input). This port can be divided into two 4-bit ports under the mode control. Each 4-bit port contains a 4-bit latch and it can be used for the control signal outputs and status signal inputs in conjunction with ports A and B.









Operating Modes

MODE 1 (Strobed Input/Output). This functional configuration provides a means for transferring I/O data to or from a specified port in conjunction with strobes or "handshaking" signals. In mode 1, port A and port B use the lines on port C to generate or accept these "handshaking" signals.

Mode 1 Basic Functional Definitions:

- Two Groups (Group A and Group B)
- Each group contains one 8-bit data port and one 4-bit control/data port.
- The 8-bit data port can be either input or output. Both inputs and outputs are latched.
- The 4-bit port is used for control and status of the 8-bit data port.

Input Control Signal Definition

$\overline{\text{STB}}$ (Strobe Input). A "low" on this input loads data into the input latch.

IBF (Input Buffer Full F/F)

A "high" on this output indicates that the data has been loaded into the input latch; in essence, an acknowledgement. IBF is set by STB input being low and is reset by the rising edge of the RD input.

INTR (Interrupt Request)

A "high" on this output can be used to interrupt the CPU when an input device is requesting service. INTR is set by the $\overline{\text{STB}}$ is a "one", IBF is a "one" and INTE is a "one". It is reset by the falling edge of $\overline{\text{RD}}$. This procedure allows an input device to request service from the CPU by simply strobing its data into the port.

INTE A

Controlled by bit set/reset of PC_4.

INTE B

Controlled by bit set/reset of PC_2.

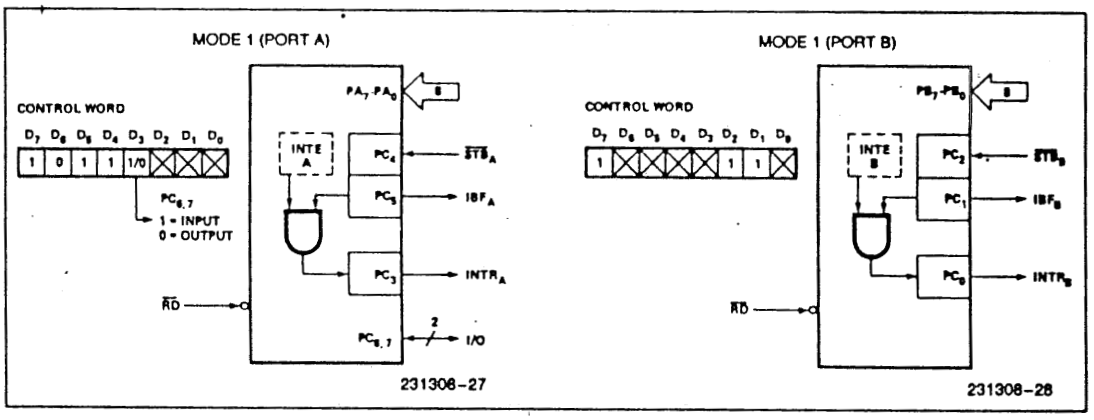


Figure 8. MODE 1 Input

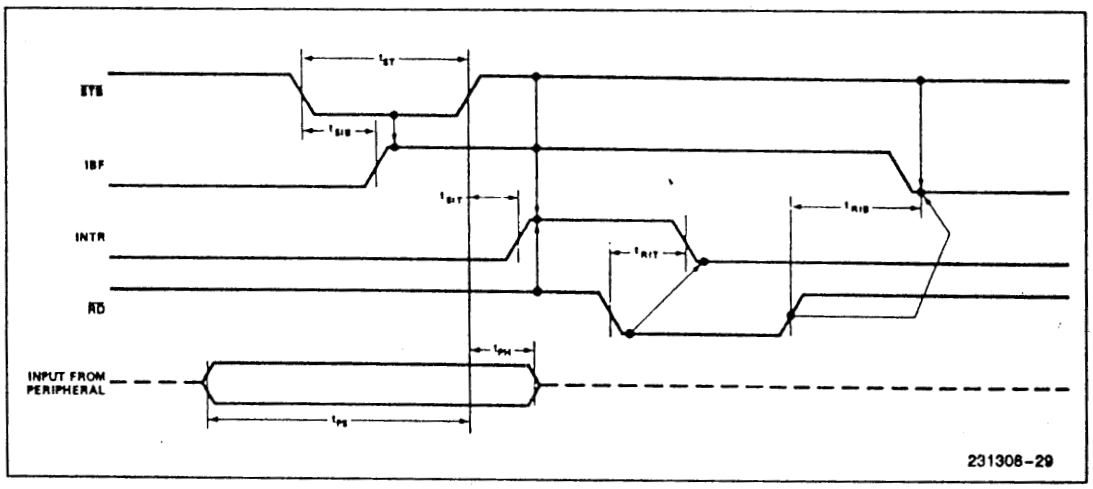


Figure 9. MODE 1 (Strobed Input)

Output Control Signal Definition

$\overline{OBF}$ (Output Buffer Full F/F). The $\overline{OBF}$ output will go "low" to indicate that the CPU has written data out to the specified port. The $\overline{OBF}$ F/F will be set by the rising edge of the $\overline{WR}$ input and reset by $\overline{ACK}$ input being low.

$\overline{ACK}$ (Acknowledge Input). A "low" on this input informs the 8255A that the data from port A or port B has been accepted. In essence, a response from the peripheral device indicating that it has received the data output by the CPU.

INTR (Interrupt Request). A "high" on this output can be used to interrupt the CPU when an output device has accepted data transmitted by the CPU. INTR is set when $\overline{ACK}$ is a "one", $\overline{OBF}$ is a "one", and INTE is a "one". It is reset by the falling edge of $\overline{WR}$.

INTE A

Controlled by bit set/reset of PC_6.

INTE B

Controlled by bit set/reset of PC_2.

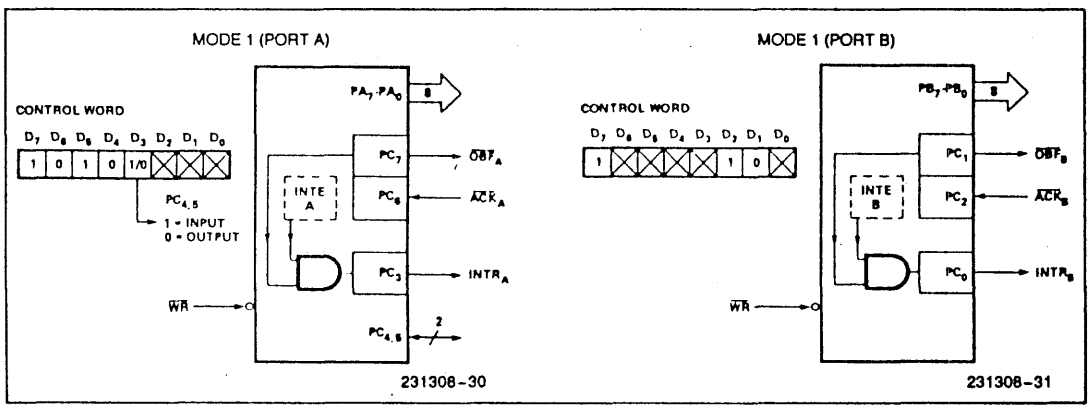


Figure 10. MODE 1 Output

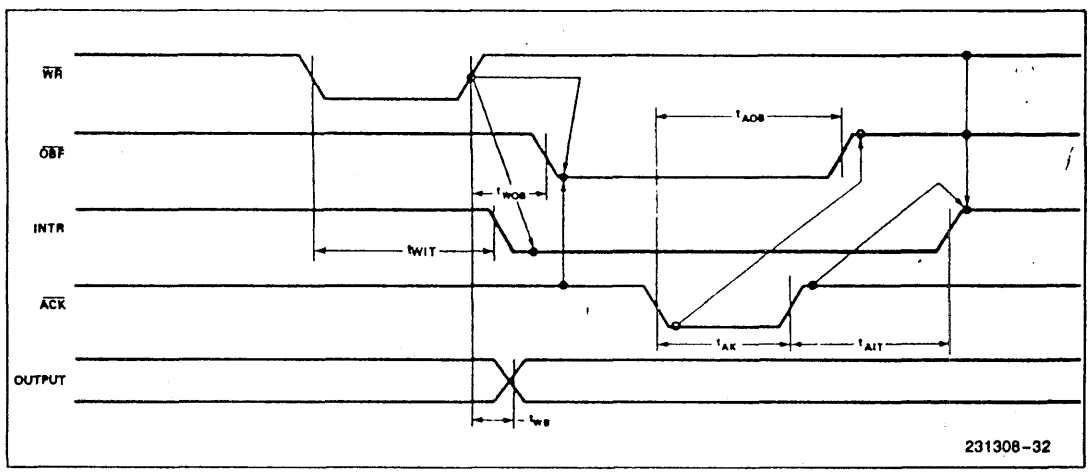


Figure 11. MODE 1 (Strobed Output)

TYPES SN5400, SN54H00, SN54L00, SN54LS00, SN54S00, SN7400, SN74H00, SN74LS00, SN74S00
QUADRUPLE 2-INPUT POSITIVE-NAND GATES

REVISED DECEMBER 1983

- **Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

description

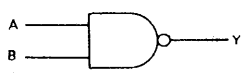
These devices contain four independent 2-input NAND gates.

The SN5400, SN54H00, SN54L00, and SN54LS00, and SN54S00 are characterized for operation over the full military temperature range of −55°C to 125°C. The SN7400, SN74H00, SN74LS00, and SN74S00 are characterized for operation from 0°C to 70°C.

FUNCTION TABLE (each gate)

INPUTS		OUTPUT
A	B	Y
H	H	L
L	X	H
X	L	H

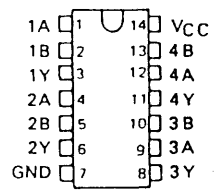
logic diagram (each gate)



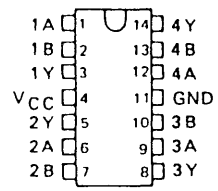
positive logic

$$Y = \overline{A \cdot B} \text{ or } Y = \overline{A} + \overline{B}$$

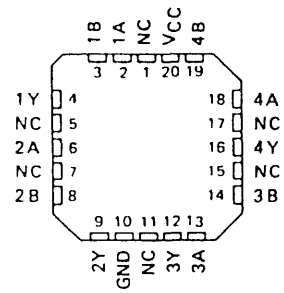
SN5400, SN54H00, SN54L00 . . . J PACKAGE
SN54LS00, SN54S00 . . . J OR W PACKAGE
SN7400, SN74H00 . . . J OR N PACKAGE
SN74LS00, SN74S00 . . . D, J OR N PACKAGE
(TOP VIEW)



SN5400, SN54H00 . . . W PACKAGE
(TOP VIEW)



SN54LS00, SN54S00 . . . FK PACKAGE
SN74LS00, SN74S00 . . . FN PACKAGE
(TOP VIEW)



NC – No internal connection

TYPES SN5402, SN54L02, SN54LS02, SN54S02, SN7402, SN74LS02, SN74S02
QUADRUPLE 2-INPUT POSITIVE-NOR GATES

REVISED DECEMBER 1983

- **Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

description

These devices contain four independent 2-input-NOR gates.

The SN5402, SN54L02, SN54LS02 and SN54S02 are characterized for operation over the full military temperature range of −55°C to 125°C. The SN7402, SN74LS02 and SN74S02 are characterized for operation from 0°C to 70°C.

FUNCTION TABLE (each gate)

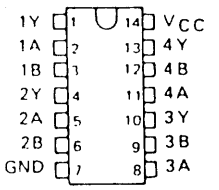
INPUTS		OUTPUT
A	B	Y
H	X	L
X	H	L
L	L	H

logic diagram (each gate)

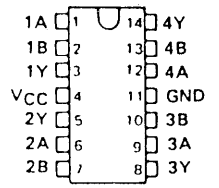
positive logic

$$Y = \overline{A} \cdot \overline{B} \text{ or } Y = \overline{A + B}$$

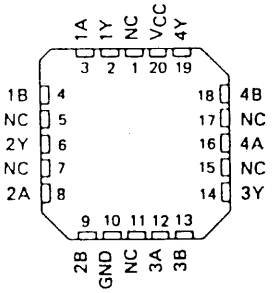
SN5402, SN54L02 . . . J PACKAGE
SN54LS02, SN54S02 . . . J OR W PACKAGE
SN7402 . . . J OR N PACKAGE
SN74LS02, SN74S02 . . . D, J OR N PACKAGE
(TOP VIEW)



SN5402 . . . W PACKAGE
(TOP VIEW)



SN54LS02, SN54S02 . . . FK PACKAGE
SN74LS02, SN74S02 . . . FN PACKAGE
(TOP VIEW)



NC - No internal connection

TYPES SN5404, SN54H04, SN54L04, SN54LS04, SN54S04, SN7404, SN74H04, SN74LS04, SN74S04
HEX INVERTERS

REVISED DECEMBER 1983

- **Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

description

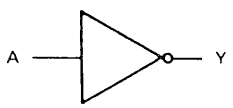
These devices contain six independent inverters.

The SN5404, SN54H04, SN54L04, SN54LS04 and SN54S04 are characterized for operation over the full military temperature range of −55°C to 125°C. The SN7404, SN74H04, SN74LS04 and SN74S04 are characterized for operation from 0°C to 70°C.

FUNCTION TABLE (each inverter)

INPUTS	OUTPUT
A	Y
H	L
L	H

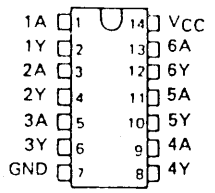
logic diagram (each inverter)



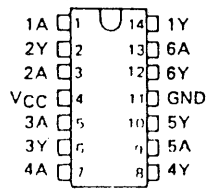
positive logic

$Y = \overline{A}$

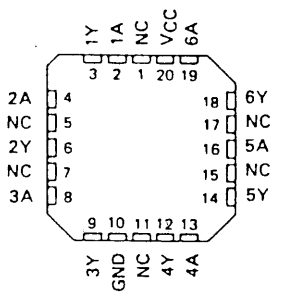
SN5404, SN54H04, SN54L04 . . . J PACKAGE
SN54LS04, SN54S04 . . . J OR W PACKAGE
SN7404, SN74H04 . . . J OR N PACKAGE
SN74LS04, SN74S04 . . . D, J OR N PACKAGE
(TOP VIEW)



SN5404, SN54H04 . . . W PACKAGE
(TOP VIEW)



SN54LS04, SN54S04 . . . FK PACKAGE
SN74LS04, SN74S04 . . . FN PACKAGE
(TOP VIEW)



NC — No internal connection

TYPES SN5420, SN54H20, SN54L20, SN54LS20, SN54S20, SN7420, SN74H20, SN74LS20, SN74S20
DUAL 4-INPUT POSITIVE-NAND GATES

REVISED DECEMBER 1983

- Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs
- Dependable Texas Instruments Quality and Reliability

description

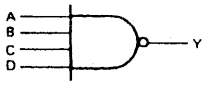
These devices contain two independent 4-input NAND gates.

The SN5420, SN54H20, SN54L20, SN54LS20 and SN54S20 are characterized for operation over the full military range of −55°C to 125°C. The SN7420, SN74H20, SN74LS20 and SN74S20 are characterized for operation from 0°C to 70°C.

FUNCTION TABLE (each gate)

INPUTS				OUTPUT
A	B	C	D	Y
H	H	H	H	L
L	X	X	X	H
X	L	X	X	H
X	X	L	X	H
X	X	X	L	H

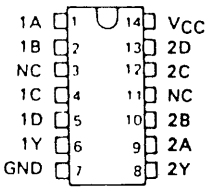
logic diagram (each gate)



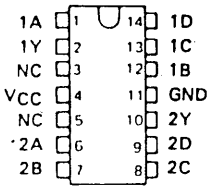
positive logic

$$Y = \overline{A \cdot B \cdot C \cdot D} \text{ or } Y = \overline{A} + \overline{B} + \overline{C} + \overline{D}$$

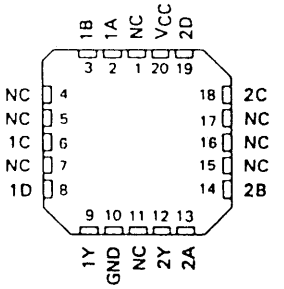
SN5420, SN54H20, SN54L20 . . . J PACKAGE
SN54LS20, SN54S20 . . . J OR W PACKAGE
SN7420, SN74H20 . . . J OR N PACKAGE
SN74LS20, SN74S20 . . . D, J OR N PACKAGE
(TOP VIEW)



SN5420, SN54H20 . . . W PACKAGE
(TOP VIEW)



SN54LS20, SN64S20 . . . FK PACKAGE
SN74LS20, SN74S20 . . . FN PACKAGE
(TOP VIEW)



NC – No internal connection

TYPES SN54H21, SN54LS21, SN74H21, SN74LS21
DUAL 4-INPUT POSITIVE-AND GATES

REVISED APRIL 1985

- **Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

description

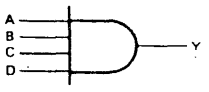
These devices contain two independent 4-input AND gates.

The SN54H21 and SN54LS21 are characterized for operation over the full military temperature range of −55°C to 125°C. The SN74H21 and SN74LS21 are characterized for operation from 0°C to 70°C.

FUNCTION TABLE (each gate)

INPUTS				OUTPUT
A	B	C	D	Y
H	H	H	H	H
L	X	X	X	L
X	L	X	X	L
X	X	L	X	L
X	X	X	L	L

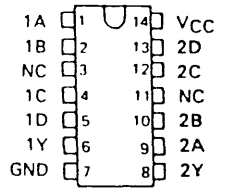
logic diagram (each gate)



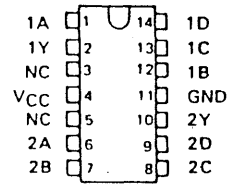
positive logic

$$Y = A \cdot B \cdot C \cdot D \text{ or } Y = \overline{\overline{A} + \overline{B} + \overline{C} + \overline{D}}$$

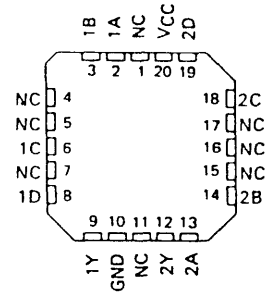
SN54H21 . . . J PACKAGE
SN54LS21 . . . J OR W PACKAGE
SN74H21 . . . J OR N PACKAGE
SN74LS21 . . . D, J OR N PACKAGE
(TOP VIEW)



SN54H21 . . . W PACKAGE
(TOP VIEW)



SN54LS21 . . . FK PACKAGE
SN74LS21 . . . FN PACKAGE
(TOP VIEW)



NC – No internal connection

TYPES SN5432, SN54LS32, SN54S32, SN7432, SN74LS32, SN74S32
QUADRUPLE 2-INPUT POSITIVE-OR GATES

REVISED DECEMBER 1983

- Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs
- Dependable Texas Instruments Quality and Reliability

description

These devices contain four independent 2-input OR gates.

The SN5432, SN54LS32 and SN54S32 are characterized for operation over the full military range of −55°C to 125°C. The SN7432, SN74LS32 and SN74S32 are characterized for operation from 0°C to 70°C.

FUNCTION TABLE (each gate)

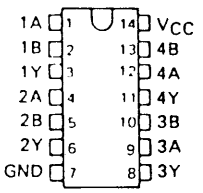
INPUTS		OUTPUT
A	B	Y
H	X	H
X	H	H
L	L	L

logic diagram (each gate)

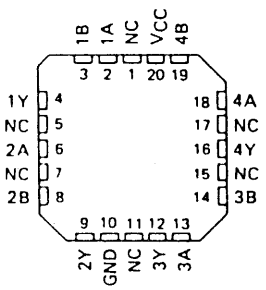
positive logic

$$Y = A + B \text{ or } Y = \overline{\overline{A} \cdot \overline{B}}$$

SN5432, SN54LS32, SN54S32 . . . J OR W PACKAGE
SN7432 . . . J OR N PACKAGE
SN74LS32, SN74S32 . . . D, J or N PACKAGE
(TOP VIEW)



SN54LS32, SN54S32 . . . FK PACKAGE
SN74LS32, SN74S32 . . . FN PACKAGE
(TOP VIEW)



NC No internal connection

TYPES SN5474, SN54H74, SN54L74, SN54LS74A, SN54S74, SN7474, SN74H74, SN74LS74A, SN74S74
DUAL D-TYPE POSITIVE-EDGE-TRIGGERED FLIP-FLOPS WITH PRESET AND CLEAR

REVISED DECEMBER 1983

- Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs
- Dependable Texas Instruments Quality and Reliability

description

These devices contain two independent D type positive-edge triggered flip flops. A low level at the preset or clear inputs sets or resets the outputs regardless of the levels of the other inputs. When preset and clear are inactive (high), data at the D input meeting the setup time requirements are transferred to the outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a voltage level and is not directly related to the rise time of the clock pulse. Following the hold time interval, data at the D input may be changed without affecting the levels at the outputs.

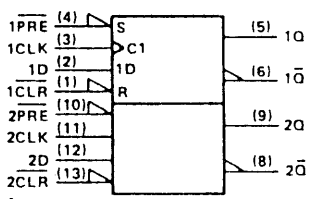
The SN54' family is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74' family is characterized for operation from 0°C to 70°C.

FUNCTION TABLE

INPUTS				OUTPUTS	
$\overline{PRE}$	$\overline{CLR}$	CLK	D	Q	$\overline{Q}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H†	H†
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	Q_0	$\overline{Q}_0$

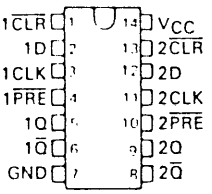
† The output levels in this configuration are not guaranteed to meet the minimum levels for V_{OH} if the lows at preset and clear are near V_{IL} maximum. Furthermore, this configuration is nonstable; that is, it will not persist when either preset or clear returns to its inactive (high) level.

logic symbol

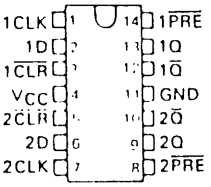


Pin numbers shown on logic notation are for D, J or N packages.

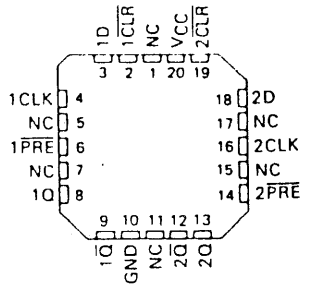
SN5474, SN54H74, SN54L74 . . . J PACKAGE
SN54LS74A, SN54S74 J OR W PACKAGE
SN7474, SN74H74 J OR N PACKAGE
SN74LS74A, SN74S74 D, J OR N PACKAGE
(TOP VIEW)*



SN5474, SN54H74 . . . W PACKAGE
(TOP VIEW)

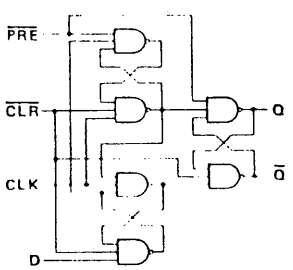


SN54LS74A, SN54S74 . . . FK PACKAGE
SN74LS74A, SN74S74 FN PACKAGE
(TOP VIEW)



NC – No internal connection

logic diagram



TYPES SN54LS138, SN54S138, SN74LS138, SN74S138
3-LINE TO 8-LINE DECODERS/DEMULTIPLEXERS

DECEMBER 1972 REVISED APRIL 1985

- **Designed Specifically for High-Speed:**
  Memory Decoders
  Data Transmission Systems
- **3 Enable Inputs to Simplify Cascading and/or Data Reception**
- **Schottky-Clamped for High Performance**

description

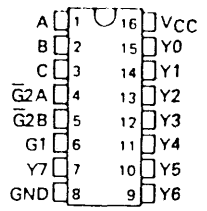
These Schottky-clamped TTL MSI circuits are designed to be used in high-performance memory decoding or data-routing applications requiring very short propagation delay times. In high-performance memory systems these decoders can be used to minimize the effects of system decoding. When employed with high-speed memories utilizing a fast enable circuit the delay times of these decoders and the enable time of the memory are usually less than the typical access time of the memory. This means that the effective system delay introduced by the Schottky-clamped system decoder is negligible.

The 'LS138 and 'S138 decode one of eight lines dependent on the conditions at the three binary select inputs and the three enable inputs. Two active-low and one active-high enable inputs reduce the need for external gates or inverters when expanding. A 24-line decoder can be implemented without external inverters and a 32-line decoder requires only one inverter. An enable input can be used as a data input for demultiplexing applications.

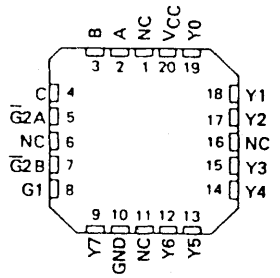
All of these decoder/demultiplexers feature fully buffered inputs, each of which represents only one normalized load to its driving circuit. All inputs are clamped with high-performance Schottky diodes to suppress line-ringing and to simplify system design.

The SN54LS138 and SN54S138 are characterized for operation over the full military temperature range of −55°C to 125°C. The SN74LS138 and SN74S138 are characterized for operation from 0°C to 70°C.

SN54LS138, SN54S138 . . . J OR W PACKAGE
SN74LS138, SN74S138 . . . D, J OR N PACKAGE
(TOP VIEW)

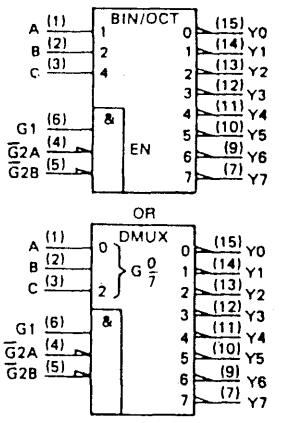


SN54LS138, SN54S138 . . . FK PACKAGE
SN74LS138, SN74S138 . . . FN PACKAGE
(TOP VIEW)



NC – No internal connection

logic symbols



Pin numbers shown on logic notation are for D, J or N packages.

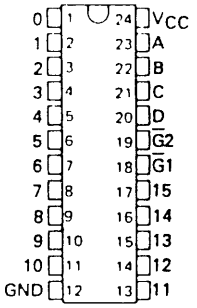
TYPES SN54154, SN54L154, SN74154
4-LINE TO 16-LINE DECODERS/DEMULTIPLEXERS

DECEMBER 1972 REVISED DECEMBER 1983

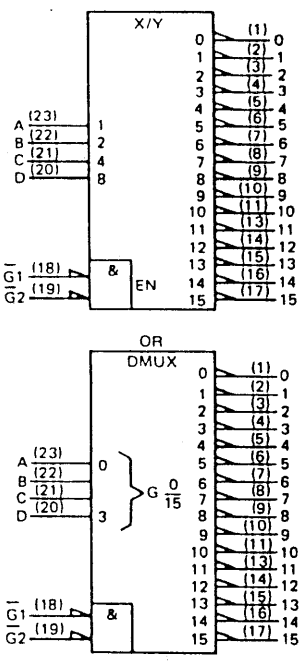
- '154 is Ideal for High Performance Memory Decoding
- 'L154 is Designed for Power-Critical Applications
- Decodes 4 Binary-Coded Inputs into One of 16 Mutually Exclusive Outputs
- Performs the Demultiplexing Function by Distributing Data From One Input Line to Any One of 16 Outputs
- Input Clamping Diodes Simplify System Design
- High Fan-Out, Low-Impedance, Totem-Pole Outputs
- Fully Compatible with Most TTL and MSI Circuits

TYPE	TYPICAL AVERAGE PROPAGATION DELAY		TYPICAL POWER DISSIPATION
	3 LEVELS OF LOGIC	STROBE	
'154	23 ns	19 ns	170 mW
'L154	46 ns	38 ns	85 mW

SN54154 . . . J OR W PACKAGE
SN54L154 . . . J PACKAGE
SN74154 . . . J OR N PACKAGE
(TOP VIEW)



logic symbol



Pin numbers shown on logic notation are for J or N packages.

description

Each of these monolithic, 4-line-to-16-line decoders utilizes TTL circuitry to decode four binary-coded inputs into one of sixteen mutually exclusive outputs when both the strobe inputs, $\overline{G1}$ and $\overline{G2}$, are low. The demultiplexing function is performed by using the 4 input lines to address the output line, passing data from one of the strobe inputs with the other strobe input low. When either strobe input is high, all outputs are high. These demultiplexers are ideally suited for implementing high-performance memory decoders. For ultra-high speed systems, SN54S138/SN74S138 and SN54S139/SN74S139 are recommended.

These circuits are fully compatible for use with most other TTL circuits. All inputs are buffered and input clamping diodes are provided to minimize transmission-line effects and thereby simplify system design.

The SN54154 and SN54L154 are characterized for operation over the full military temperature range of −55°C to 125°C. The SN74154 is characterized for operation from 0°C to 70°C.

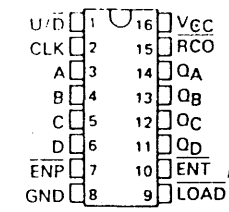
TYPES SN54LS169B, SN54S168, SN54S169, SN74LS169B, SN74S168, SN74S169
SYNCHRONOUS 4-BIT UP/DOWN COUNTERS

OCTOBER 1976 - REVISED MAY 1983

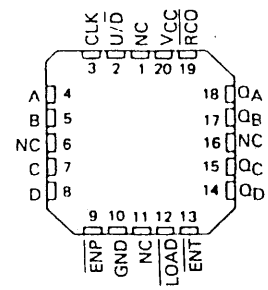
'S168 . . . SYNCHRONOUS UP/DOWN DECADE COUNTERS
'LS169B, 'S169 . . . SYNCHRONOUS UP/DOWN BINARY COUNTERS

- Programmable Look-Ahead Up/Down Binary/Decade Counters
- Fully Synchronous Operation for Counting and Programming
- Internal Look-Ahead for Fast Counting
- Carry Output for n-Bit Cascading
- Fully Independent Clock Circuit

SN54S168, SN54LS169B, SN54S169 . . . J OR W PACKAGE
SN74S168, SN74LS169B, SN74S169 . . . D, J OR N PACKAGE
(TOP VIEW)



SN54S168, SN54LS169B, SN54S169 . . . FK PACKAGE
SN74S168, SN74LS169B, SN74S169 . . . FN PACKAGE
(TOP VIEW)



NC No internal connection

description

These synchronous presettable counters feature an internal carry look ahead for cascading in high speed counting applications. The 'S168 is a decade counter and the 'LS169B and 'S169 are 4-bit binary counters. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincident with each other when so instructed by the count-enable inputs and internal gating. This mode of operation helps eliminate the output counting spikes that are normally associated with asynchronous (ripple-clock) counters. A buffered clock input triggers the four master-slave flip-flops on the rising (positive-going) edge of the clock waveform.

These counters are fully programmable; that is, the outputs may each be preset to either level. The load input circuitry allows loading with the carry-enable output of cascaded counters. As loading is synchronous, setting up a low level at the load input disables the counter and causes the outputs to agree with the data inputs after the next clock pulse.

TYPE	TYPICAL MAXIMUM CLOCK FREQUENCY		TYPICAL POWER DISSIPATION
	COUNTING UP	COUNTING DOWN	
'LS169B	35MHz	35MHz	100mW
'S168, 'S169	70MHz	55MHz	500mW

The carry look-ahead circuitry provides for cascading counters for n-bit synchronous applications without additional gating. Instrumental in accomplishing this function are two count-enable inputs and a carry output. Both count enable inputs ($\overline{ENP}$, $\overline{ENT}$) must be low to count. The direction of the count is determined by the level of the up/down input. When the input is high, the counter counts up; when low, it counts down. Input $\overline{ENT}$ is fed forward to enable the carry output. The carry output thus enabled will produce a low-level output pulse with a duration approximately equal to the high portion of the Q_A output when counting up and approximately equal to the low portion of the Q_A output when counting down. This low-level overflow carry pulse can be used to enable successive cascaded stages. Transitions at the $\overline{ENP}$ or $\overline{ENT}$ inputs are allowed regardless of the level of the clock input. All inputs are diode-clamped to minimize transmission-line effects, thereby simplifying system design.

These counters feature a fully independent clock circuit. Changes at control inputs ($\overline{ENP}$, $\overline{ENT}$, $\overline{LOAD}$, U/$\overline{D}$) that will modify the operating mode have no effect until clocking occurs. The function of the counter (whether enabled, disabled, loading, or counting) will be dictated solely by the conditions meeting the stable setup and hold times.

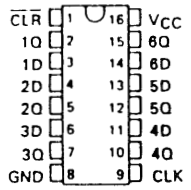
TYPES SN54174, SN54175, SN54LS174, SN54LS175, SN54S174, SN54S175, SN74174, SN74175, SN74LS174, SN74LS175, SN74S174, SN74S175
HEX/QUADRUPLE D-TYPE FLIP-FLOPS WITH CLEAR

DECEMBER 1972 · REVISED DECEMBER 1983

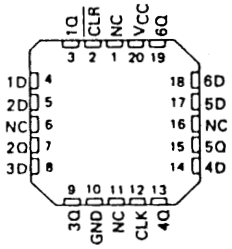
'174, 'LS174, 'S174 . . . HEX D-TYPE FLIP-FLOPS
'175, 'LS175, 'S175 . . . QUADRUPLE D-TYPE FLIP-FLOPS

- '174, 'LS174, 'S174 Contain Six Flip-Flops with Single-Rail Outputs
- '175, 'LS175, 'S175 Contain Four Flip-Flops with Double-Rail Outputs
- Three Performance Ranges Offered: See Table Lower Right
- Buffered Clock and Direct Clear Inputs
- Individual Data Input to Each Flip-Flop
- Applications include:
  - Buffer/Storage Registers
  - Shift Registers
  - Pattern Generators

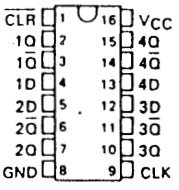
SN54174, SN54LS174, SN54S174 . . . J OR W PACKAGE
SN74174 . . . J OR N PACKAGE
SN74LS174, SN74S174 . . . D, J OR N PACKAGE
(TOP VIEW)



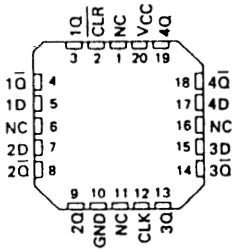
SN54LS174, SN54S174 . . . FK PACKAGE
SN74LS174, SN74S174 . . . FN PACKAGE
(TOP VIEW)



SN54175, SN54LS175, SN54S175 . . . J OR W PACKAGE
SN74175 . . . J OR N PACKAGE
SN74LS175, SN74S175 . . . D, J OR N PACKAGE
(TOP VIEW)



SN54LS175, SN54S175 . . . FK PACKAGE
SN74LS175, SN74S175 . . . FN PACKAGE
(TOP VIEW)



NC · No internal connection

description

These monolithic, positive-edge-triggered flip-flops utilize TTL circuitry to implement D-type flip-flop logic. All have a direct clear input, and the '175, 'LS175, and 'S175 feature complementary outputs from each flip-flop.

Information at the D inputs meeting the setup time requirements is transferred to the Q outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a particular voltage level and is not directly related to the transition time of the positive-going pulse. When the clock input is at either the high or low level, the D input signal has no effect at the output.

These circuits are fully compatible for use with most TTL circuits.

FUNCTION TABLE
(EACH FLIP-FLOP)

INPUTS			OUTPUTS	
CLEAR	CLOCK	D	Q	$\bar{Q}$†
L	X	X	L	H
H	↑	H	H	L
H	↑	L	L	H
H	L	X	Q_0	$\bar{Q}_0$

H = high level (steady state)
L = low level (steady state)
X = irrelevant
↑ = transition from low to high level
Q_0 = the level of Q before the indicated steady state input conditions were established.
† = '175, 'LS175, and 'S175 only

TYPES	TYPICAL MAXIMUM CLOCK FREQUENCY	TYPICAL POWER DISSIPATION PER FLIP FLOP
'174, '175	35 MHz	38 mW
'LS174, 'LS175	40 MHz	14 mW
'S174, 'S175	110 MHz	75 mW

TYPES SN54365A THRU SN54368A, SN54LS365A THRU SN54LS368A
SN74365A THRU SN74368A, SN74LS365A THRU SN74LS368A
HEX BUS DRIVERS WITH 3-STATE OUTPUTS

REVISED DECEMBER 1983

- **3-State Outputs Drive Bus Lines or Buffer Memory Address Registers**
- **Choice of True or Inverting Outputs**
- **Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIP's**
- **Dependable Texas Instruments Quality and Reliability**

'365A, '367A, 'LS365A, 'LS367A True Outputs
'366A, '368A, 'LS366A, 'LS368A Inverting Outputs

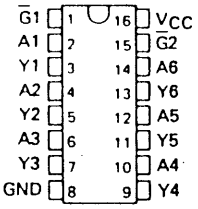
description

These Hex buffers and line drivers are designed specifically to improve both the performance and density of three-state memory address drivers, clock drivers, and bus oriented receivers and transmitters. The designer has a choice of selected combinations of inverting and noninverting outputs, symmetrical $\overline{G}$ (active low control) inputs.

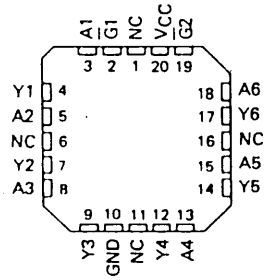
These devices feature high fan out, improved fan in, and can be used to drive terminated lines down to 133 ohms.

The SN54365A thru SN54368A and SN54LS365A thru SN54LS368A are characterized for operation over the full military temperature range of −55 C to 125 C. The SN74365A thru SN74368A and SN74LS365A thru SN74LS368A are characterized for operation from 0 C to 70 C.

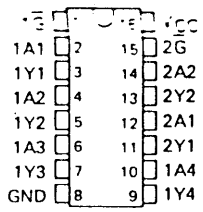
SN54365A, 366A, SN54LS365A, 366A . . . J PACKAGE
SN74365A, 366A . . . J OR N PACKAGE
SN74LS365A, SN74LS366A . . . D, J OR N PACKAGE
(TOP VIEW)



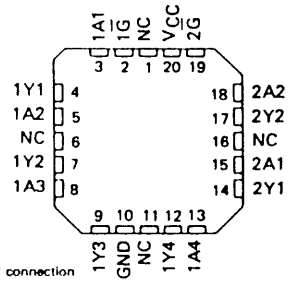
SN54LS365A, SN54LS366A . . . FK PACKAGE
SN74LS365A, SN74LS366A . . . FN PACKAGE
(TOP VIEW)



SN54367A, 368A, SN54LS367A, 368A . . . J PACKAGE
SN74367A, 368A . . . J OR N PACKAGE
SN74LS367A, SN74LS368A . . . D, J OR N PACKAGE
(TOP VIEW)



SN54LS367A, SN54LS368A . . . FK PACKAGE
SN74LS367A, SN74LS368A . . . FN PACKAGE
(TOP VIEW)



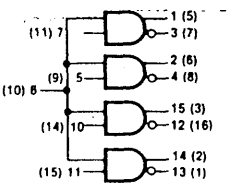
NC - No internal connection

F10124 • F10524
QUAD TTL TO ECL TRANSLATOR

DESCRIPTION — The F10124 and F10524 are Quad Translators, designed to convert TTL logic levels to 10K ECL logic levels. The inputs are compatible with standard or with Schottky TTL. A Common Enable input (E_C), when LOW, holds all inverting outputs HIGH and holds all True outputs LOW. The differential outputs allow each circuit to be used as an inverting/non-inverting translator or as a differential line driver. The output levels are voltage compensated.

When the circuit is used in the differential mode, the F10124, due to its high common mode rejection, overcomes voltage gradients between the TTL and ECL ground systems.

LOGIC DIAGRAM



V_{CC} = 9 (13)
V_{EE} = 8 (12)
GND = 16 (4)

Logic Equations
2 = 5•6
4 = 5•6

DC CHARACTERISTICS: V_{EE} = −5.2 V, V_{CC} = GND

SYMBOL	CHARACTERISTIC	LIMITS B	LIMITS TYP	LIMITS A	UNITS	T_A	CONDITIONS
V_{IH}	Input Current HIGH	+1.9 +1.8 +1.8		5.0 5.0 5.0	V	0°C 25°C 75°C	Guaranteed Input Voltage HIGH for All Inputs
V_{IL}	Input Voltage LOW	0 0 0		+1.1 +1.1 +0.95	V	0°C 25°C 75°C	Guaranteed Input Voltage LOW for All Inputs
V_{CD}	Clamp Input Voltage	−1.5			V	25°C	I_{IN} = −10 mA
V_{BD}	Input Breakdown Voltage	+5.5			V	25°C	I_{IN} = +1.0 mA, Other Inputs V_{IN} = GND
I_{IH}	Input Current HIGH			50	µA	25°C	V_{IN} = +2.4 V, E_C V_{IN} = +0.4 V
I_{IHX}	Input Current HIGH E_C			200	µA	25°C	E_C V_{IN} = +2.4 V All Other Inputs V_{IN} = +0.4 V
I_{ILX}	Input Current LOW E_C	−12.8		mA	~~-25°C~~	25°C	E_C V_{IN} = +0.4 V, All Other Inputs V_{IN} = +4.0 V
I_{IL}	Input Current LOW	−3.2			mA	25°C	V_{IN} = +0.4 V, E_C V_{IN} = +4.0 V
I_{EE}	Power Supply Current	−34	−26		mA	25°C	Inputs and Outputs Open
I_{CCH}	Power Supply Current		+13	+16	mA	25°C	All Inputs V_{IN} = +4.0 V
I_{CCL}	Power Supply Current		+18	+25	mA	25°C	All Inputs V_{IN} = GND

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