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SARAS CD/EoR Radiometer: Design and Performance of the Digital Correlation Spectrometer

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In the currently accepted model for cosmic baryon evolution, Cosmic Dawn (CD) and the Epoch of Reionization (EoR) are significant times when first light from the first luminous objects emerged, transformed and subsequently ionized the primordial gas. The 21 cm (1420 MHz) hyperfine transition of neutral hydrogen, redshifted from these cosmic times to a frequency range of 40 MHz to 200 MHz, has been recognized as an important probe of the physics of CD/EoR. The global 21 cm signal is predicted to be a spectral distortion of a few 10's to a few 100's of mK, which is expected to be present in the cosmic radio background as a trace additive component. Shaped Antenna measurement of the background RAdio Spectrum (SARAS) is a spectral radiometer purpose designed to detect the weak 21 cm signal from CD/EoR. An important subsystem of the radiometer, the digital correlation spectrometer, is developed around a high-speed digital signal processing platform called pSPEC. pSPEC is built around two quad 10-bit analog-to-digital converters (EV10AQ190) and a Virtex 6 (XC6VLX240T) field programmable gate array, with provision for multiple Gigabit Ethernet and 4.5 Gbps fiber-optic interfaces. Here, we describe the system design of the digital spectrometer, the pSPEC board, and the adaptation of pSPEC to implement a high spectral resolution (61 kHz), high dynamic range (10^5:1) correlation spectrometer covering the entire CD/EoR band. As the SARAS radiometer is required to be deployed in remote locations where terrestrial radio frequency interference (RFI) is a minimum, the spectrometer is designed to be compact, portable and operating off internal batteries. The paper includes an evaluation of the spectrometer's susceptibility to RFI and capability to detect signals from CD/EoR.

Keywords: 21 cm signal; channelization; FPGA; correlation spectrometer; RFI; nonlinearity.

1. Introduction

Cosmic Dawn (CD) and the Epoch of Reionization (EoR) represent significant moments in the history of the evolving universe when growing matter inhomogeneities transformed the primordial gas to one with galaxies surrounded by a diffuse intergalactic medium. There is considerable uncertainty in our understanding of the precise timing of events across this period and of the nature of the first stars and first ultra-faint galaxies that lit up the universe and transformed the state of the gas; the uncertainty is owing to lack of observational constraints. It has long been recognized that the 21 cm (1420 MHz) hyperfine transition of neutral hydrogen, redshifted from this interval in cosmic time to a frequency range of about 40 MHz to 200 MHz, could potentially serve as an important probe of CD/EoR. Two complimentary approaches have been pursued to probe the evolving hydrogen in CD/EoR via redshifted 21 cm: one, using a radiometer (an antenna connected to a spectrometer) to measure the global spectrum of the radio sky and hence the mean evolution of the hyperfine level populations and ionization state; second, using large interferometer arrays to measure

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the fluctuations in 21 cm brightness temperature at those epochs. Both approaches require careful design of radio telescopes so that confusing spectral structure from unwanted additives and bandpass calibration errors are minimized.

SARAS is an on-going experiment that aims to detect the global 21 cm from CD and EoR in the frequency range 40 MHz to 200 MHz. The first SARAS radiometer, SARAS 1, deployed a fat-dipole antenna over ferrite tiles, operating usefully in the 110 MHz to 175 MHz band (Patra *et al.*, 2013, 2015) and provided improved accuracy in the absolute calibration of the sky emission at 150 MHz. SARAS 2 deployed a sphere monopole antenna that operated in the 110 MHz to 200 MHz band and placed the first constraints on models for CD/EoR by ruling out a subset of plausible models for thermal baryon evolution (Singh *et al.*, 2017, 2018a,b). SARAS 3, currently under development, aims at the 50 MHz to 100 MHz band and targets the redshifted 21 cm absorption at CD. The SARAS spectrometer is a common digital receiver for all SARAS antennas and analog receiver configurations, that may individually target up to octave bandwidth spectral segments in the (40 to 200) MHz band. The paper presented here is on the design and performance of a digital correlation spectrometer purpose built for SARAS.

Apart from SARAS, there are a few other global 21 cm experiments; for example, EDGES (Monsalve *et al.*, 2017a,b; Bowman *et al.*, 2018), LEDA (Bernardi *et al.*, 2016; Price *et al.*, 2018), PRI^{z}M (Philip *et al.*, 2019), SCI-HI (Voytek *et al.*, 2014) and BIGHORNS (Sokolowski *et al.*, 2015). Interferometer arrays that are operational and have been built with a key science goal of detecting the 21 cm power spectrum are MWA (Lonsdale *et al.*, 2009), LoFAR (van Haarlem *et al.*, 2013) and HERA (DeBoer *et al.*, 2017). We present in Table 1 a comparison of digital receiver specifications for global EoR experiments underway, including the SARAS digital receiver that is described in this paper. Following the recent EDGES claim of a detection of a deep absorption at 78 MHz, and in the context of the need for independent verification and concerns (Hills *et al.*, 2018; Bradley *et al.*, 2019; Singh *et al.*, 2019), SARAS 3 is targeting the (50 to 100) MHz octave band.

Recent advances in processing capabilities of Field Programmable Gate Arrays (FPGAs), combined with high-speed analog-to-digital converters (ADC), make the implementation of high-resolution, high dynamic range spectrometers for detecting 21 cm from CD/EoR possible. ADCs capable of directly sampling signals in the frequency band of interest for CD/EoR — the 40 MHz to 200 MHz radio-frequency (RF) band — without the need for nonlinear analog down conversion, and modern FPGAs with their high-density programmable features, have enabled development of robust, high-performance RFI-tolerant CD/EoR spectrometers with better control over systematics.

The SARAS system configuration has evolved over the years. However, in all versions, the sky signal is split at some stage, band limited in parallel analog receiver chains to below 250 MHz, before being presented to a digital correlation spectrometer. The correlation spectrometer concept has been a feature of all versions of SARAS, along with phase switching between the two arms so as to cancel any additive systematics that couple into the receiver chains. At the core of the SARAS digital

Table 1. Spectrometer specification for SARAS compared with other ongoing experiments attempting to detect global redshifted 21 cm from CD/EoR.

Experiment	Operating freq. range (MHz)	Sampling frequency (Ms/s)	ADC bit precision (Bits)	Spectral resolution (kHz)	Reference
SARAS 3	50–100	500	10	61	This paper
SARAS 2	110–200	500	10	61	(Singh *et al.*, 2018a)
SARAS 1	87.5–175	175	12	85.4	(Patra *et al.*, 2013)
EDGES (Low-band)	50–100	400	14	6.1	(Bowman *et al.*, 2018)
EDGES (High-band)	90–190	400	14	6.1	(Monsalve *et al.*, 2017a)
LEDA	30–88	196.6	8	24	(Price *et al.*, 2019)
PRI^{z}M	0–250	500	8	61	(Philip *et al.*, 2019)
BIGHORNS	∼500	960	8	117	(Sokolowski *et al.*, 2015)
SCH-HI	30–250	500	12	7.6	(Voytek *et al.*, 2014)

spectrometer is a high-speed signal processing platform, precision SPECtrometer (pSPEC), consisting of two 10-bit ADCs from e2V technologies followed by a Virtex-6 FPGA. The ADCs, operating at 500 mega samples per second (Ms/s), digitize the two analog signals. In the FPGA, blocks of ADC samples from each receiver chain are weighted with a window function and separately Fourier transformed. The averaged power spectra corresponding to each of the two arms, as well as the complex cross power spectrum corresponding to the product, are computed and streamed out to an acquisition computer through a Gigabit Ethernet interface.

The SARAS radiometer consists of an antenna, antenna-base electronics that is located in an enclosure immediately beneath the antenna, an analog signal conditioning unit and a digital receiver. The analog signal conditioning unit and digital receiver are located about 100 m away from the antenna. The antenna base electronics is designed to cycle through a number of switching states to present successively the antenna and cold and hot terminations to the receiver for calibration. The digital receiver enclosure includes the digital spectrometer and a laptop computer and electronics for generating control signals for the antenna base electronics; the digital receiver controls the radiometer operations, generating signals for switching the antenna base electronics, synchronously controlling the digital signal processing in the spectrometer and also the acquisition into the laptop computer. Signal transport of digital control signals to the antenna and of analog signals from the antenna base to the analog signal conditioning unit is via optical-fiber.

In the following sections, we present the system description, including the rational behind choice of components, integration of various sub-sections of the digital correlation spectrometer, packaging, thermal management and, finally, laboratory tests carried out to evaluate the SARAS spectrometer.

2. System Description

Design of any digital correlation spectrometer for detecting EoR, which is an extremely weak signal embedded in orders of magnitude brighter foreground, is challenging. The theory of the formation of First Stars and the subsequent heating and reionization of the gas by First Light that emerges from the earliest ultra faint galaxies is highly uncertain; therefore, the predicted 21 cm signal is largely unknown but nevertheless expected to be in the range of a few 10's to a few 100's of mK brightness temperature. Since the sky foreground brightness in the frequency band of interest is in the range of several 100's to 1000's of K, the dynamic range of spectral receivers aiming to detect the global 21 cm signal needs to be about a million to one. Additionally, since the receiver band includes FM and TV channels, which can be several orders stronger than the foregrounds, it is required to operate in the presence of substantial terrestrial RFI. Every sub-system in the signal path, from the sensor of the EM field to the back-end digital spectrometer, needs careful design/engineering to adequately suppress the deleterious effects of RFI.

Figure 1 shows the system architecture of the SARAS spectrometer. At the core of the spectrometer is the pSPEC board, built around two, four-core time-interleaved Analog-to-Digital Converters (ADCs) and a Virtex-6 FPGA. For wideband applications in radio astronomy, FPGAs are preferred due to the large number of high bandwidth input/output (I/O) pins that may be used to stream wideband data sampled at high rates to implement computationally-intensive signal processing algorithms. FPGAs, with their inbuilt specialized hardware blocks, are well-suited to demultiplex high-speed serial data into multiple parallel data streams, enabling a parallelized channelization structure to transform the samples of a wideband time-domain signal into multiple narrow sub-bands for further processing.

The digital spectrometer has a laptop computer for data acquisition and control. The laptop connects to a docking station that provides power to the laptop and has a port replicator with USB and Gigabit Ethernet ports. Through these ports, the laptop connects to the pSPEC board and also to peripherals like a control and monitor card, a synthesizer and an Arduino card, which is used to generate the state-switching signals to the RF front-end receiver of SARAS. A 10 MHz signal derived from a rubidium oscillator provides a stable reference to the synthesizer used to generate the sampling clock to the ADCs. The entire digital receiver is assembled inside an RF-shielded enclosure to suppress broad band and narrow band interfering signals, which are inevitably generated in the digital hardware, from propagating to the antenna and thereby limiting the sensitivity of the radiometer via self-generated RFI.

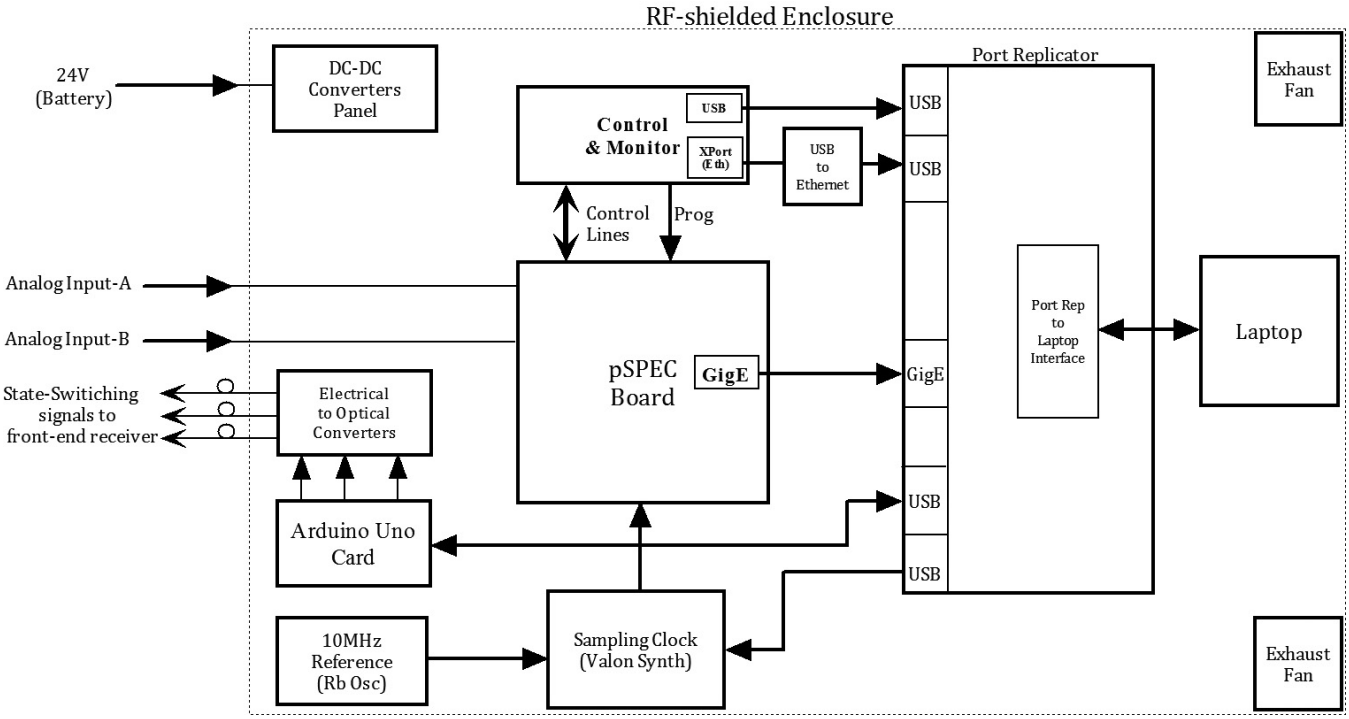

Fig. 1. System level architecture of the SARAS spectrometer.

It may be noted here that pSPEC was envisaged as a common DSP platform catering to the requirements of CD/EoR and also for detection of cosmological recombination lines (APSERa; Sathyanarayana Rao *et al.* (2015)), where a wide-band 2 GHz bandwidth correlation spectrometer is required. In this paper, as part of SARAS 3 experiment, we report the adaptation of pSPEC in the development of a high-precision, high dynamic range digital correlation spectrometer to detect the global CD/EoR signal. Table 2 provides a summary of the specifications of the FX correlation spectrometer for SARAS 3.

Table 2. Specifications of the SARAS 3 correlation spectrometer.

Spectrometer parameter	Value
Number of analog inputs	2
Sampled bandwidth	250 MHz
Sampling speed	500 Ms/s
ADC	EV10AQ190CTPY
ADC bit resolution	10 (ENOB = 7.8)
Nominal power at input to the ADC	−28 dBm
ADC headroom for RFI	26 dB
Virtex 6 FPGA	XC6VLX240T (1156 pins)
Length of FFT	16384 point
Precision in the FFT twiddle factors	16,16 bits
Length of window function	16384 point
Bit precision of coefficients of the window function	18 bits
Maximum sidelobe levels in the spectral PSF	81 dB
Spectral resolution following windowed FFT	61.75 kHz
Number of on-chip spectral averages and integration time	2048, 67.108 ms
Data rate	16 MBps

2.1. *The pSPEC board*

The pSPEC board is a Xilinx FPGA-based signal processing platform and is the primary building block of the digital correlation spectrometer. Figure 2 shows the major components within the pSPEC board. pSPEC features two 10-bit quad time-interleaved ADCs (ADC-1 and ADC-2; both are EV10AQ190CTPY from e2V technologies), a Virtex-6 LX240T FPGA from Xilinx, two high-speed electrical interfaces, a Gigabit Ethernet interface and optical interfaces consisting of eight 4.5 Gbps Small Form-factor Pluggable (SFP) ports and a 40 Gbps Quad Small Form-factor Pluggable (QSFP) port. Additionally, there are dedicated connectors to accept "SYNC" signals to control the synchronous sampling at the two quad ADCs and a Global Positioning System (GPS) signal to time-stamp data streaming out of the pSPEC. Figure 3 shows a photograph of the pSPEC board that has been implemented as a mixed-signal printed circuit

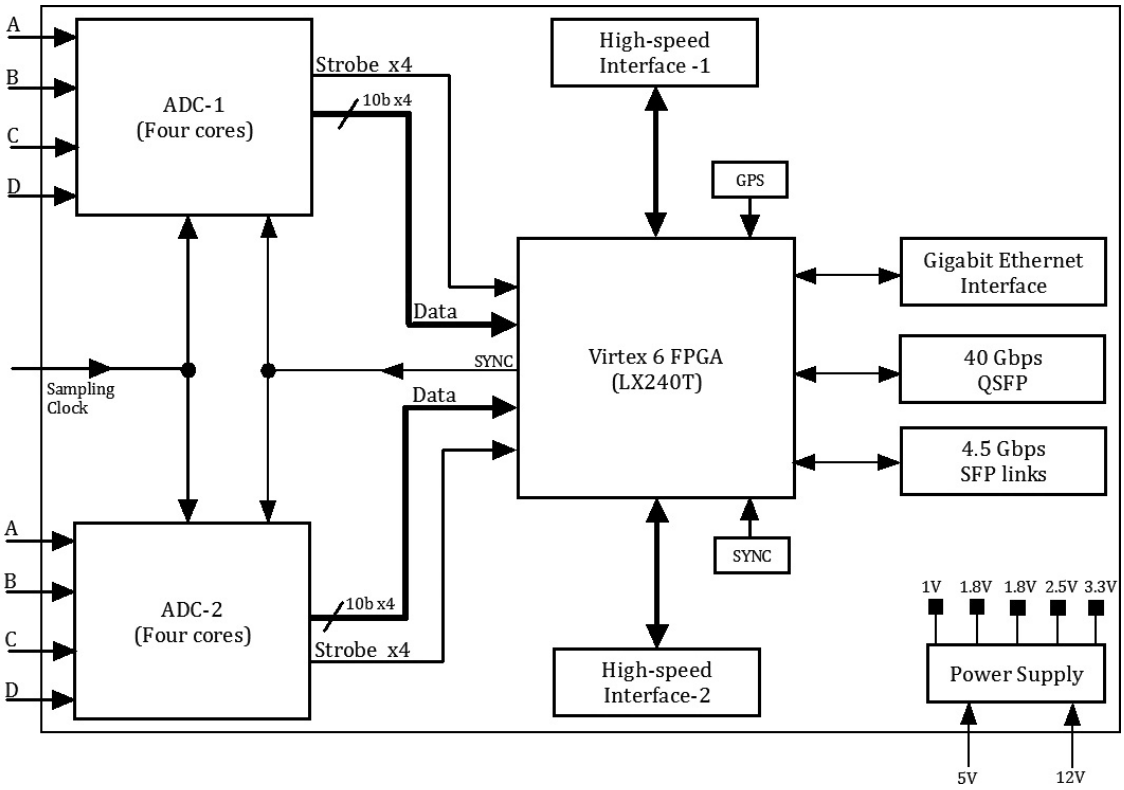

Fig. 2. Block diagram of the pSPEC architecture.

Fig. 3. Photograph of the pSPEC board.

board with a height of 233 mm (6U standard) and a depth of 257 mm.

2.1.1. *The analog-to-digital converter in pSPEC*

The choice of the ADC for the pSPEC board was driven by the requirement of developing a common signal processing platform capable of digitizing analog signals having bandwidths ranging from a few 100 MHz to about 2 GHz. A market survey of candidate broadband data converters possessing 2 or more channels with at least 10 bits of resolution resulted in the choice of EV10AQ190. It is a 10-bit quad core device, with each core having a maximum

Table 3. Data sheet specifications of the EV10AQ190 ADC used in pSPEC.

Quad core ADC, each with 10-bit resolution
On-chip programmable registers of ADC are accessed via SPI bus
Analog input bandwidth of 3.2 GHz
Full-scale input range of 500 mVp-p (~ -2 dBm)
SNR of 52 dB for Fin = 100 MHz and Fclk = 1.25 GSps (independent channel mode)
ENOB of 8.3 for Fin = 100 MHz and Fclk = 1.25 GSps (independent channel mode)
Power dissipation of 1.4 W per channel
380-pin EBGA package
Isolation between channels: 60 dB

sampling rate of 1.25 giga samples per second (Gs/s). A summary of the features and data sheet specifications of the ADC used in pSPEC is in Table 3.

The device has an on-chip programmable register that allows configuring the ADC in a mode in which it samples four independent analog channels, or samples two channels using a pair of ADC cores per channel in time-interleaved mode, or samples a single channel by time interleaving all four cores; the three modes provide maximum sampling rates of 1.25 Gs/s, 2.5 Gs/s and 5 Gs/s, respectively. Thus, the two ADCs on pSPEC enable digitization of eight independent analog signals (each up to 625 MHz bandwidth) or a pair of wideband analog signals (each up to 2.5 GHz bandwidth) in time-interleaved mode. The 10-bit wide data from the individual ADC cores are output on an low-voltage differential signaling (LVDS) bus using double data rate (DDR) interface, permitting the latching of data on rising and falling edges of the ADC data strobe signal, at maximum rate of 625 MHz. When pSPEC is configured to operate as spectrometer for SARAS, the ADCs are configured in independent channel mode (nontime-interleaving) of operation and only two out of four ADC cores are used. ADC cores, clocked at 500 MHz rate, are used to digitize a pair of baseband analog signals each of which have a band that at most extends up to 250 MHz.

When a multi-channel ADC is used to digitize multiple analog signals for a correlation spectrometer, crosstalk between channels is a major concern, especially in precision and high dynamic range applications. In the pSPEC board, we have provided adequate spacing between routes and utilized multiple routing layers within the 18-layer PCB of pSPEC; as a consequence, within each ADC, 58 dB isolation between cores has been achieved. This compares favorably with expectations based on the device data sheet, which specify about 60 dB isolation.

The signal-to-noise ratio (SNR) of an ADC is related to the effective number of bits (ENOB) b see (Kester, 2009; IEEE, 2000)

$$\mathrm{SNR} = (6.02b + 1.76)\,\mathrm{dB}. \tag{1}$$

From Eq. (1), the SNR of an ideal 10-bit ADC is $\sim$62 dB, assuming that the ENOB is 10 bits. The specifications of the ADC suggest an ENOB of 8.3, which implies that the ADC device used in pSPEC may be expected to provide sampling with a SNR of 51.7 dB.

One of the important factors that determines the performance of a high-speed, high-resolution ADC is the quality of its sampling clock. The degradation in the SNR of the ADC due to any jitter in the sampling clock is given by (IEEE, 2000)

$$\mathrm{SNR} = -20\log(2\pi f_o \tau), \tag{2}$$

where f_o is the highest frequency component in the analog signal that is input to the ADC and τ is the jitter in the sampling clock. From Eq. (2), for f_o of 250 MHz and assuming an ideal SNR of 62 dB, allowable jitter in the sampling clock should be less than 0.5 ps so as not to degrade performance beyond ideal device limitations.

The sampling clock for pSPEC is generated using a programmable frequency synthesizer Valon 5008 from Valon Technologies. It has the provision to take in an external stable reference signal so as to provide better stability and spectral purity for the generated sampling clock. In SARAS, the primary frequency standard for deriving the sampling clock is an ultra-low phase noise rubidium oscillator, PRS10, from Stanford Research Systems. The 10 MHz signal from PRS10 is used as reference for the Valon synthesizer to derive the 500 MHz sampling clock for the ADCs on the pSPEC board; use of such an ultra-stable reference provides a clock with jitter limited to $\sim$2 fs, which is substantially below the 0.5 ps requirement.

Preceding the digitizer, the voltage gains in the analog receiver chain of SARAS are adjusted such that the total power at the analog input of the ADC is about -28 dBm. This is the input power level at which the total harmonic distortion of the ADC is minimum. Corresponding to the quantization step of 0.488 mV, the quantization noise power referred to the ADC input is about -65 dBm, for an ideal 10-bit ADC. Assuming that the ENOB of the pSPEC

ADC is 8.3, the quantization noise power referred to the ADC input is given by:

$$-65 + (6.02 * (10 - 8.3)) = -54.7 \text{ dBm}, \quad (3)$$

where the term 6.02 converts decibels ($\log 10$ representation) to bits ($\log 2$ representation). Thus, the quantization noise increases the system temperature by less than 0.5%.

2.1.2. *The FPGA used in pSPEC*

The FPGA on pSPEC was envisaged to grab data from all eight ADCs, deserialize them into parallel data streams that can be clocked within the realm of Virtex 6 FPGA technology, and transform data that is in time sequence to spectral domain. The channel data is then processed in the FPGA to correlate between data streams of the different ADCs, and transport the averaged correlation computed in channelized data to a computer for further processing and recording on to hard disk.

There were a number of considerations leading to the choice of an FPGA for pSPEC. A requirement was that the FPGA have adequate I/O pin-count along with inbuilt deserializer to handle the data bits that would stream at 625 Mbps (double data rate) from all eight ADCs of pSPEC. Additionally, the FPGA was required to have logic and specialized resources like block RAM (BRAM), DSPE1 slices that would be required for implementation of a real-time FX correlation spectrometer, and embedded blocks like Tri-mode Ethernet Media Access Controllers (TEMAC) for control and data transfer. The cost of the FPGA device was also a consideration. These led to XC6VLX240T-FF1156 as the FPGA for the SARAS spectrometer. The selected Virtex-6 FPGA device is a 1156-pin flip-chip fine-pitch ball grid array (BGA) package built using 40 nm technology and belongs to the sub-family LXT that is meant for high-performance logic with advanced serial connectivity.

XC6SX315T, which is an FPGA that has a footprint compatibility with XC6VLX240T, has also been chosen for pSPEC as an alternate configuration. This FPGA is specifically meant for pSPEC cards for APSERa in which all the eight ADC cores may be used in time-interleaved mode and clocked at 1 GHz. This Virtex-6 SXT sub-family FPGA comes with enhanced DSP48E1 slices, BRAM and logic resources.

Both FPGAs have 600 user I/O pins sufficient to interface all eight ADCs and still have provision for general-purpose I/O lines and high-speed electrical interface between pSPEC boards. Specifications of the two FPGAs selected for pSPEC are summarised in Table 4.

Table 4. Specifications of the Virtex 6 FPGAs on pSPEC.

Parameter	LX240T FPGA	SX315T FPGA
Speed grade	−2	−2
Logic cells	241152	314880
Slices	37680	49220
Distributed RAM (kb)	3650	5090
Number of 36 kb BRAM	416	704
Multi-mode clock manager	12	12
Maximum single-ended I/O	600	600
Maximum differential I/O pairs	300	300
DSP48E1 slices	768	1344
Ethernet MACs (TEMACs)	4	4
GTX transceivers (up to 6.6 Gbps)	24	24
PCI Express interface blocks (SR 2.0)	2	2

2.1.3. *Layout of pSPEC board*

The 1156-pin BGA package of both LX240T and SX315T FPGAs are organized in a matrix of 34 rows by 34 columns. The 380-pin package of the ADC is organized in a matrix of 24 rows by 24 columns. At least six signal routing layers (Intel, 2017) are required to achieve full breakout of all the 600 I/O pins available on the FPGA package. Based on the component density, the pin-counts of the selected FPGA and ADC, and the need to provide for high-speed optical and electrical interfaces, pSPEC is laid out on an 18-layer printed circuit board (PCB) consisting of eight signal routing layers and 10 power and ground planes. To maintain signal integrity of high frequency analog signals and high speed digital routes, the two outer layers of the 18-layer pSPEC PCB are fabricated using low loss tangent, low coefficient of thermal expansion (CTE) and high glass transition temperature laminate EM-827 from Elite Material Corporation.

2.2. *Digital signal processing in pSPEC*

Inside the Virtex-6 FPGA of pSPEC, the correlation spectrometer is realized as four distinct stages: grabbing of ADC data samples, weighting of data samples, Fourier transformation using a 16384-point FFT engine (F-engine) and lastly a multiply-and-accumulate stage (X-engine). The F-engine

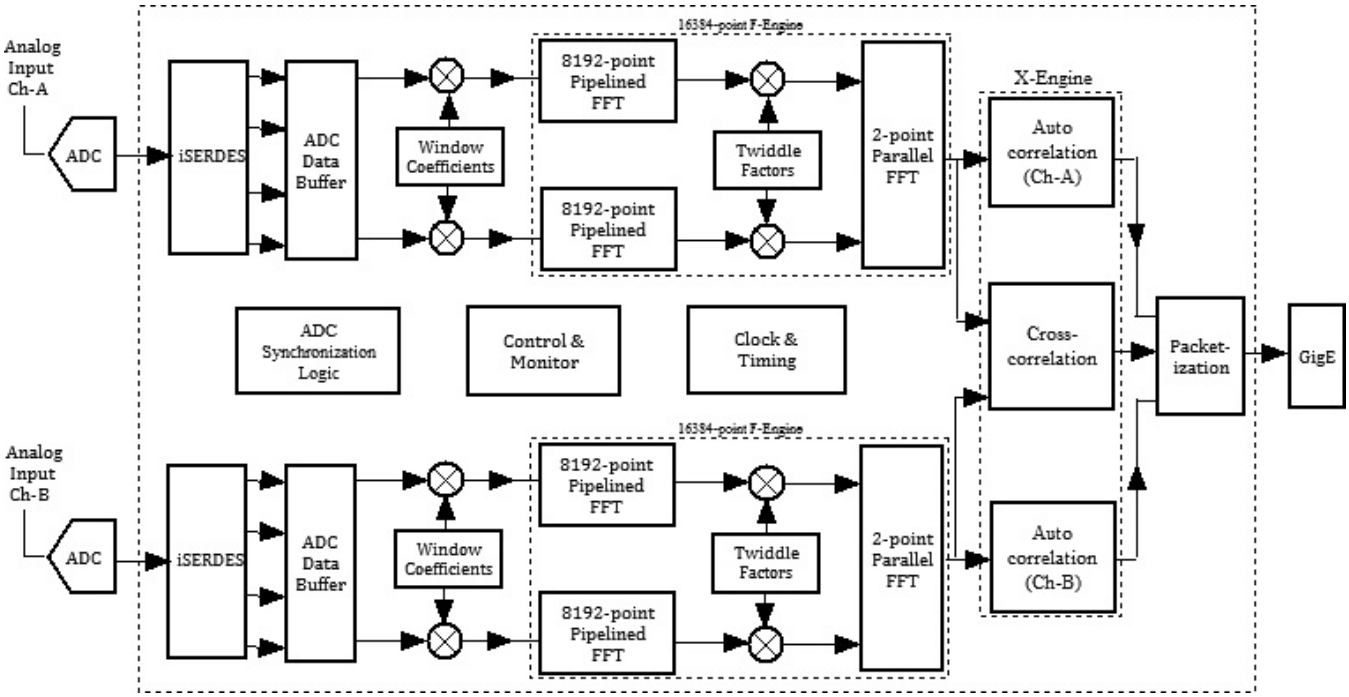

Fig. 4. FPGA firmware architecture of SARAS spectrometer.

is implemented as a split-FFT (MxN point) architecture.

Figure 4 shows the block diagram of the firmware architecture for the SARAS spectrometer. Analog signals from the pair of analog signal processing chains are fed to two ADC cores for digitization. The ADCs on pSPEC are supplied with a low-jitter sampling clock of 500 MHz from a Valon 5008 synthesizer. A 10 MHz signal derived from the rubidium oscillator, PRS10, forms the primary frequency standard and is provided as an external reference to this synthesizer. At the FPGA interface, individual bits of each ADC are grabbed and deserialized by a factor of four using input serializer–deserializer (ISERDES) primitives. The ADC data stream is required to be demultiplexed only by a factor of two to bring the clock frequency of the two parallel paths within the realm of the Virtex 6 FPGA. However, for DDR interface, the minimum deserialization factor of four in the ISERDES primitives constrains the design to demultiplex the data stream by the same factor. Subsequently, to keep the FPGA resource consumption to a minimum while implementing the correlation spectrometer firmware, we have used a data buffer to reduce the number of demultiplexed paths from four to two.

Considering the high sensitivity required for observing the CD/EoR signal, windowing helps to limit the spillover from any strong narrow-band interfering signal to adjacent spectral channels. Prior to Fourier transformation, time samples from each ADC are weighted with 16384 window coefficients, $w(n)$, generated using the minimum 4-term window function (Nuttal, 1981)

$$w(n) = 0.3635819 - 0.4891775\cos\left(\frac{2\pi n}{N-1}\right) + 0.1365995\cos\left(\frac{4\pi n}{N-1}\right) - 0.0106411\cos\left(\frac{6\pi n}{N-1}\right) \quad (4)$$

with index n ranging from 0 to 16383 and $N = 16384$.

The F-engine of the FX spectrometer consists of two 8192-point ($N = 8192$) pipelined FFT cores operating in parallel, followed by two complex multipliers for phase rotation and a 2-point ($M = 2$) parallel FFT to combine the outputs from the two parallel paths. While the 8192-point pipelined FFT cores are sourced from Xilinx IP-core generator, the 2-point parallel FFT is custom designed to compute a 2-point FFT in a single clock cycle. Using this scheme, a 16384-point streaming channelizer has been implemented, providing 8192 complex channels covering the band (0 to 250) MHz at the output. The 8192-point spectrum from the F-engine has

spectral values spaced 30.518 kHz apart; however, the spectral resolution is 61.035 kHz owing to the windowing. The time required to compute each 16384-point FFT is 32.768 μs. Two such F-engines that are instantiated inside the Virtex-6 FPGA to channelize the sampled signals from the two ADCs, produce complex FFT output streams $X(k)$ and $Y(k)$, with index k ranging from 1 to 8192.

$$S_{xx}(k) = X(k)X^*(k), \tag{5}$$

$$S_{yy}(k) = Y(k)Y^*(k). \tag{6}$$

As shown in Eqs. (5) and (6), in the multiplier unit of the X-engine, power spectrum corresponding to signals in each of the two paths are computed from complex FFT streams $X(k)$ and $Y(k)$. In the accumulator unit of the X-engine, blocks of 2048 FFT spectra are averaged to generate the auto-correlation power spectra corresponding to the signals in each of the paths. $X^*(k)$ and $Y^*(k)$ are the complex conjugates of the two FFT output streams.

$$S_{xy}(k) = X(k)Y^*(k). \tag{7}$$

As shown in Eq. (7), the cross-power spectrum, $S_{xy}(k)$, is obtained by channel-wise complex multiplication of $X(k)$ and $Y^*(k)$. The averaged cross-power spectrum is computed, simultaneously, in the second X-engine instantiated inside the FPGA, by averaging blocks of 2048 spectra. The choice of averaging time — over 2048 FFTs — avoids overflow in the multiply-and-accumulate resources of the FPGA and the processing of the block of 2048 spectra is realized in an on-chip integration time of 67 ms.

The on-chip integration time of 67 ms represents a trade-off between the need for detection and mitigation of short timescale and transient RFI, and sustaining the data acquisition in real-time without loss of data packets. UDP is used owing to its reduced bandwidth overhead and low-latency connection between applications. A dedicated hardware Tri-mode Ethernet Media Access Controller (TEMAC) block available inside the Virtex 6 FPGA, along with an external Small Form-factor Pluggable (SFP) module that provides a copper interface to the external world, is used for transferring data from pSPEC to the acquisition computer. 16 frames of integrated spectra, corresponding to a total integration time of about 1.072 s (67 ms $\times$ 16), are streamed out of pSPEC in a single data acquisition cycle. This allows the receiver to be switched between different system states, between Dicke switch positions, between calibration noise source in on and off conditions, etc. every 1.072 s and the 16 frames of data read out for each such state. The firmware for the operation of the FPGA was developed in VHDL using Xilinx ISE software for design flow and Mentor Graphics' ModelSim for HDL simulation. The optimized firmware operates at a clock frequency of 250 MHz, with less than 50% FPGA resource utilization. A summary of the FPGA resources utilized in implementing the FX correlation spectrometer is provided in Table 5.

Table 5. Summary of Virtex 6 LX24OT resource utilization.

FPGA resource utilization	Usage	Percentage
Number of occupied slices	9478 out of 37680	25
Number of RAM36E1	236 out of 416	56
Number of MMCM	6 out of 12	50
I/O	191 out of 600	31
Number of DSP48E1s	114 out of 768	14
Number of TEMACs	1 out of 4	25

2.3. *Control and data acquisition*

While the pSPEC unit forms the heart of the digital spectrometer, a laptop computer that is part of the digital receiver is designated to be the master controller. It is used to configure and control the ADCs and FPGA on pSPEC through a Lantronix XPort and USB-based controller card (XPort card), control the real-time digital signal processing activities inside the FPGA, perform acquisition of integrated spectra streaming out of pSPEC via the Gigabit Ethernet interface, and synchronously control the switching of states of the analog electronics in the antenna-base receiver and the signal conditioning unit. The Valon synthesizer module and the Arduino Uno microcontroller card are interfaced with the laptop. The laptop computer selected to be the master controller is a Toshiba Portege R930 laptop, which is a portable laptop weighing 1.4 kg and with a 512 GB solid-state drive (SSD) for storage. In addition to being compact, durable and light-weight and relatively invulnerable to vibrations, SSDs, as compared to hard-drives, provide advantages like better system responsiveness and operating power efficiency as there are no moving parts.

The laptop has a docking connector to interface with a compatible Toshiba high-speed port replicator/docking station. The port replicator has a 10/100/1000 Mbps LAN interface, six USB interfaces and laptop eject lever with lock. When the laptop is

docked, power to charge the laptop is provided through the DC-In port of the port replicator. With these features, the port replicator eliminates the inconvenience of connecting and disconnecting multiple cables whenever the laptop is required to be connected/disconnected from the spectrometer.

The digital spectrometer is wired in such a way that only when the laptop is docked in the port replicator and powered on, the Arduino Uno card receives its power and control-signals through a USB interface to the port replicator. A solid-state relay controlled by the Arduino Uno switches-in the +24 V to power all other units of the spectrometer.

2.3.1. *The switching states of analog receiver*

The switch states of the analog receiver chain housed beneath the antenna and in the signal conditioning unit are controlled using three control signals generated from the combination of a program running on the laptop and the microcontroller on the Arduino Uno card. The control signals (i) switch the calibration noise source on/off, (ii) Dicke switch between antenna and an internal reference termination, and (iii) switch the output of the front-end receiver alternately between the two paths to implement phase switching in the correlation spectrometer. Switching the calibration noise source provides calibration data for correcting for the bandpass response of the receiver chain. Dicke switching rejects unwanted additives in the front-end receiver electronics. Phase switching the analog signal path is designed to reject common-mode unwanted additives that enter the signal path in the analog signal conditioning unit and samplers.

Four Broadcom optical transmitters, based on HFBR 1412Z low-cost 820 nm miniature link fiber-optic components, mounted inside the digital spectrometer unit are used to convert the control signals (electrical) from the Arduino Uno card to optical. Four optical-fiber cables connected to ST (housed) optical interfaces on the RF-shielded enclosure carry the control signals to the front-end receiver unit kept at a distance of about 100 m from the digital spectrometer unit. One of the four control signals is dedicated to remotely switch on the front-end receiver at the start of observations and automatically shutdown both the analog front-end receiver and the digital receiver at the end of observing sessions, to save battery power. Optical-fibers are preferred to metallic coaxial cables as they minimally affect the antenna behavior. Synchronizing the switching of the states in the analog receiver via the control signals, and the operations of the pSPEC card and acquisition of averaged spectra corresponding to each of the states is carried out by a C program running on the laptop computer.

A setup script, written in C, routes the configuration bitstream of the FPGA through a USB interface between the port replicator and the XPort card. A high-speed cable connects the XPort card to the FPGA though one of the two high-speed interfaces. The programmable registers inside the ADCs are accessed through SPI interface between the FPGA and the ADCs. These registers are used to configure the ADC in one of the three operating modes, or write/read the Offset, Gain and Phase (OGP) control registers of each of the four cores in the ADC. The contents of the ADC registers are written to and read from a dedicated set of registers inside the FPGA. These registers in turn communicate with the laptop through the 10/100 Lantronix Ethernet interface on the XPort card.

2.3.2. *Data acquisition from pSPEC*

A socket program is used to grab the UDP data packets streamed out of pSPEC. The three integrated spectra along with data markers and identifiers are packetized and streamed out of the FPGA via the Gigabit Ethernet interface at about 16 MB/s, using User Datagram Protocol (UDP). The UDP packet header used in SARAS digital correlation spectrometer is 74 bytes long, of which 42 bytes are used to represent standard fields such as the destination media access controller (MAC) address, source MAC address, header checksum, Internet Protocol (IP) address of destination and source, etc. The remaining 32 bytes are customized for SARAS in which information related to packet counter, to keep track of packet loss (if any), time-stamp, standard patterns for data alignment, identifying the version of the SARAS experiment, etc., is embedded. Spectrometer data corresponding to each of the switched states of the front-end receiver are extracted by stripping out data markers and identifiers from the acquired data and routed to designated buffers for further processing.

The digital spectrometer built around the pSPEC platform and associated sub-systems, including the laptop and port replicator, were assembled in a custom designed three-tiered metallic frame. The trolley is placed in a shielded enclosure. A picture of spectrometer with the door of the

Fig. 5. Trolley showing various modules of SARAS 3 digital receiver.

shielded enclosure open to show the frame with subsystems is shown in Fig. 5.

2.4. *Shielded enclosure for the digital spectrometer*

The global cosmological redshifted 21 cm signal is expected to be rather faint, with peak amplitude about 20 mK to 200 mK; therefore, terrestrial RFI may potentially confuse a detection. External RFI from communications and broadcast transmitters may be avoided by deploying the radiometer in remote sites where RFI power is adequately small. However, self-generated RFI from the receiver system needs to be prevented from coupling into the signal path so that it does not produce artifacts in the data and hence limit the sensitivity of the radiometer. As with any radio telescope, in SARAS too, the primary effort has been on preventing the clock frequency tones, their harmonics and wideband emissions from the high-speed digital electronics and data acquisition computer from reaching the antenna and feeding back into the system. Radio frequency shielding of these contaminating sources of emission by housing them in an RF-shielded enclosure helps in isolating them from the antenna and analog receiver chain.

The entire digital receiver of SARAS is housed inside a commercial RF-shielded enclosure which attenuates electromagnetic signals generated within the enclosure by about 75 dB in the CD/EoR band. To measure the isolation achievable from the enclosure, a radiating antenna connected to a sinewave generator was placed inside the enclosure to simulate a source of RF emission. A receiving antenna connected to a spectrum analyzer and kept at a distance of 5 m from the enclosure was used to measure the strength of signal leaking out of the enclosure. Strengths of the tone were recorded for the two cases in which the door of the enclosure was kept open and subsequently closed. This differential measurement provided a measure of the isolation achievable from the enclosure. Additionally, measurements of strength of the radiated tone at increasing distances away from the enclosure showed that attenuation would increase by nearly 6 dB (Trainotti, 1990) due to propagation loss each time the distance of the receiving antenna from the enclosure was doubled. As the SARAS antenna is kept at least 100 m away from the enclosed digital receiver, the strength of any self-generated RFI from the digital receiver is suppressed by about 100 dB. The strength of emissions from the digital receiver were also measured without the shielding, and it was determined that the attenuation of the enclosure plus space loss was adequate to suppress the RFI received by the antenna to below 1 mK.

The shielded enclosure has two exhaust fans for forced cooling of the entire SARAS digital receiver system, which dissipates about 150 W. To test the cooling efficiency of the enclosure, the digital receiver was operated in its observing configuration while two temperature probes connected to a logger recorded the ambient temperature outside the enclosure (maintained constant) and the temperature inside the enclosure. The temperature recorded by the probe inside the enclosure gradually increased from the ambient value and in about 2 h, it saturated at a value about 5°C higher than the ambient value.

The pSPEC FPGA for SARAS application dissipates about 12 W. The sum of the thermal resistance of the LX240T FPGA (0.1°C/W) and that of the fan sink (1.7°C/W) mounted on the device is 1.8°C/W. In order to maintain the FPGA junction temperature below about 75°C, 10° below the maximum allowed value of 85°C, the maximum temperature inside the RF-shielded enclosure should not exceed 41°C. CD/EoR observations using the SARAS radiometer is carried out only at night to avoid solar emissions and also increased terrestrial RFI in the daytime; and the ambient temperature at the observing site at night is then required to be less than 36°C.

2.5. *Power supply*

As stated earlier, the precision SARAS spectral radiometer operates at long wavelengths in bands

covering FM and TV channels, and is susceptible to deleterious effects of strong RFI signals from terrestrial FM, TV stations. Therefore, all sub-systems of SARAS radiometers are designed to be compact, portable and easily deployable in remote areas where the strength of terrestrial RFI is expected to be relatively small. In remote areas with no access to mains power supply, the entire radiometer depends on battery power for its operation. The SARAS digital receiver system operates off a 24 V power supply. A set of four, 12 V 100 A h batteries, arranged in a series–parallel combination, provides 24 V supply with adequate current capacity. The battery pack has the necessary ampere-hour capacity for at least 8 h of continuous operation without exceeding 50% in the depth of discharge. The batteries are housed in a shielded enclosure with provision to recharge the batteries *in situ*, after each observing session. Two RG-400 coaxial cables are used to connect the power from the shielded enclosure containing the battery bank to the shielded enclosure housing the digital electronics; the center conductor of one coaxial cable carries the positive 24 V supply and that of the second coaxial cable connects the negative terminal of the battery pack. Type-*N* connectors are used at panels and the outer conductors of both the coaxial cables are connected to the battery enclosure chassis to shield the cores carrying the positive and negative lines of the DC power supply and prevent digital noise from being radiated via the power supply cables. The power supply lines are also filtered to block RF noise.

Charging of the battery pack is done using a petrol generator or, alternately, using a set of six solar panels and a Renogy Rover MPPT Solar Charge Controller. Charging is disabled and disconnected during observing.

Using a set of DC–DC converters from Vicor Corporation, power to various sub-sections of the spectrometer are derived from the 24 V supply. A panel containing four converter modules are used to derive 19.5 V for the laptop docking station that includes a port replicator and also supplies the laptop power, a 12 V for the pSPEC card, a 5 V also for the pSPEC card and a separate 5 V for the Valon synthesizer and a Lantronix+USB based XPort card. The rubidium-disciplined crystal oscillator PRS10 is powered directly from 24 V.

A picture of RF-shielded enclosure containing the SARAS digital receiver is in Fig. 6.

Fig. 6. The Digital Receiver is in the white colored shielded enclosure and the black painted shielded enclosure beneath the digital receiver houses the batteries. The analog signal conditioner is the unit to the right and the red unit to the left is the battery charger.

3. Performance of the Spectrometer

The SARAS spectrometer is a common digital receiver for all SARAS antennas and analog receiver configurations, that may individually target up to octave bandwidth spectral segments in the 40 MHz to 200 MHz band. In this section, results from characterization of high-speed ADC on pSPEC, evaluation of basic performance of spectrometer as a common digital receiver for SARAS and evaluation of spectrometer's capability to provide output spectra with spurious features which are well below the expected limits of CD/EoR signals are described.

3.1. *ADC characterization*

The signal-to-noise-and-distortion ratio (SINAD), an important dynamic performance indicator of an ADC, is defined as the ratio of the root-mean-square (RMS) signal amplitude to the mean value of the root-sum-square of noise and all other spectral components, excluding DC. In the pSPEC board, for a sampling clock of 500 MHz and for an input tone at 150 MHz with power at 1 dB below full scale (−3 dBm), SINAD is measured to be 48.71 dB. If we substitute this measured SINAD for SNR in Eq. (1), we infer that the ENOB of the ADC in the pSPEC board is 7.8 bits, which is somewhat lower than the device data sheet specification of 8.3 bits. Another important specification of a high-speed ADC is the spurious-free dynamic range (SFDR) indicating the

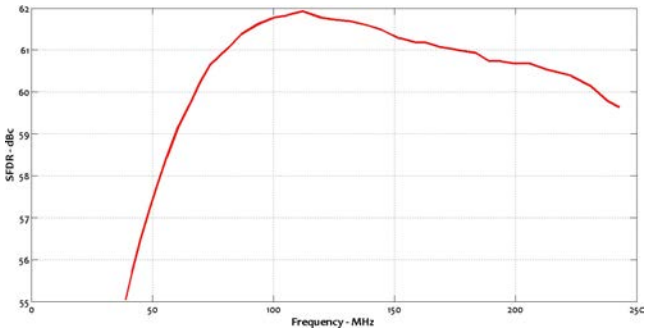

Fig. 7. SFDR performance of ADC on pSPEC as function of frequency (40 to 240 MHz).

nonlinearity in the analog-to-digital conversion process. It is defined as the ratio of the RMS value of the signal to the RMS value of the worst spurious signal regardless of where it falls in the frequency spectrum (Kester, 2009). For the ADC on pSPEC, SFDR as function of frequency covering the basic SARAS spectrometer frequency range of 40 MHz to 240 MHz has been measured. A plot of SFDR (dB below carrier) versus frequency of the input tone to ADC is shown in Fig. 7. The tone power was maintained at 1 dB below the full-scale input of the ADC, which is −2 dBm. The measured SFDR is consistent with the data sheet specifications to within ±1 dB.

The tolerance on ADC nonlinearity is demanding because of the high dynamic range required of the spectrometer, particularly when operated in sites where significant RFI is present. A measure of ADC nonlinearity is two-tone, third-order inter-modulation distortion (IMD3). For an input consisting of two closely spaced tones around 200 MHz (close to the upper edge of SARAS band of interest), IMD3 performance was evaluated for tone powers ranging from −45 dBm to −6 dBm. Best IMD3 performance of ADC of −53 dBc was measured for tone powers in the range −16 dBm to −28 dBm. In SARAS experiments, we have aimed to maintain total power at ADCs analog input port at −28 dBm. The total power of −28 dBm in any Gaussian random signal presented at the analog input of the ADC is 26.7 dB greater than the quantization noise of the ADC, and also 26 dB below the full-scale range of the ADC (−2 dBm) beyond which pSPEC ADC clips a sinusoidal signal. This ensures a headroom corresponding to about 4 bits is available to accommodate any strong RFI that may be substantially greater than the total band power from the sky and receiver noise.

These performance measurements suggest that the SARAS spectrometer may be expected to have spurious responses at about 50 dB below the RFI. Therefore, if spurious spectral structure is to be significantly less than the expected CD/EoR signals, which is 20 mK to 200 mK, then SARAS radiometer cannot be used in places where there are a large number of interfering lines within the band whose strength exceed 2000 K.

3.2. *General performance of the spectrometer*

Windowing of ADC time sequence helps in limiting the spill over to adjacent spectral channels due to a strong narrow-band interfering signal. This minimum 4-term Nuttal window function provides, ideally, a sidelobe suppression of about 98 dB; in practice, due to the 10-bit digitization of the analog signals and the finite-precision representation of signals inside the FPGA, a sidelobe suppression of 80 dB is measured. The down weighting by the window function reduces the effective integration time by a factor of two and increases the noise-equivalent bandwidth of the channels by a factor of two; however, the severe windowing has the advantage that even with an RFI as strong as 10^6 K, due to high suppression achieved, contamination of neighboring and other spectral channels is limited to below 10 mK.

3.3. *CD/EoR testing*

The performance of the spectrometer has been demonstrated in the laboratory with long duration integrations. The digital spectrometer was connected to the SARAS 3 analog receiver (Nambissan *et al.*, 2020). It was inappropriate to conduct laboratory tests of the digital spectrometer with any CD/EoR antenna connected to the receiver. First, the laboratory environment has substantial locally generated RFI that would saturate the sensitive receiver. Second, it is critical that the scattering matrix element S11 of the antenna be the same as in open field conditions where CD/EoR observations are done: this is because the magnitude and structure of internal systematics does depend on the S11 characteristics. The near-field environment within the laboratory would have parasitic elements that alter the antenna scattering matrix element S11. It may also be pointed out here that anechoic

chambers, with wall absorptivity of the quality needed to allow for laboratory testing for internal systematics, are not available at the long wavelengths at which CD/EoR radiometers operate. For all these reasons, in place of the antenna, a resistance-inductance-capacitance (RLC) series network was connected to the receiver. This approach is the same as that adopted by Singh *et al.* (2018a). The SARAS 3 CD/EoR antennas are shaped monopoles (Raghunathan *et al.*, 2020), electrically short in that their tuned frequencies are above their operating bands. To make the RLC network a useful simulator of the antenna, the network values are chosen so that the circuit provides to the receiver an S11 characteristic similar to what the CD/EoR antenna would provide. For this, the resonant frequency of the network is kept above the operating band and at the tuned frequency of the antenna. And the values are selected so that the magnitude of the reflection coefficient across the observing band is same as that for the antenna. Thus, the internal receiver systematics would be expected to be the same as when the system observes in open field.

The RLC network was selected to simulate the CD antenna designed for operation in the 50 MHz to 100 MHz octave band (Raghunathan *et al.*, 2020). The digital spectrometer system was operated for 17 h to examine for internal systematics. Data acquired were band pass calibrated with switched noise injection; absolute calibration was provided by separate laboratory calibration of the magnitude of the injected wideband noise (Singh *et al.*, 2018a). The calibrated spectrum was averaged for the 17 h. The receiver Dicke switches between the RLC network and an ambient temperature termination, to make a differential measurement; therefore, the calibrated spectrum is corrected for this differencing by adding the ambient temperature of the reference, to yield the antenna temperature. The measured spectrum of the antenna temperature over this octave band is shown in Fig. 8: in this laboratory test, the spectrum represents the noise temperature of the RLC network. The resistance R in the RLC network is chosen to be 50 Ω. At the resonant frequency of the LC series elements, the impedance of the network is matched to the receiver and the measured noise temperature (antenna temperature in Fig. 8) is the ambient temperature of the resistance, which is about 300 K. But this occurs above and outside the 50 MHz to 100 MHz observing band. Within the band, the impedance of the RLC

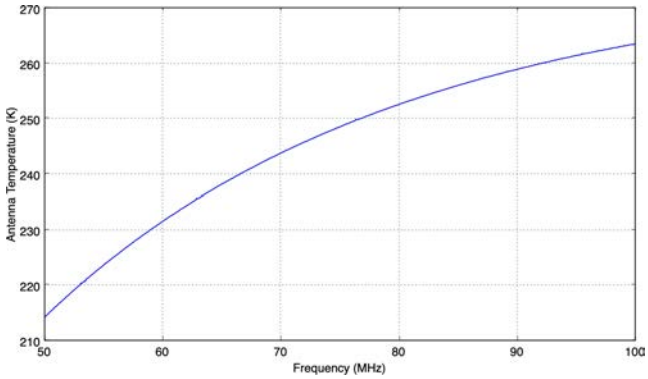

Fig. 8. Calibrated spectrum of a resistance-inductance-capacitance network as measured with the SARAS spectrometer over an octave band (50 to 100) MHz.

network progressively deviates from this matched condition as we move to lower frequencies, and the noise temperature provided by the network to the receiver progressively diminishes below 300 K. As seen in Fig. 8, the measured antenna temperature or network noise temperature drops over the band from about 264 K at 100 MHz down to about 215 K at 50 MHz, and this fall off appears to be smooth with no obvious higher order structure.

We have examined the data in Fig. 8 for spurious spectral structure arising from internal systematics including the digital spectrometer, which might confuse any detection of CD/EoR 21 cm signals. A maximally smooth polynomial (Sathyanarayana Rao *et al.*, 2017) was fit to the data to examine for embedded low-amplitude systematics. It may be noted here that the maximally smooth fitting polynomial is purpose designed to not have zero-crossings in higher order derivatives, and hence will not fit out any embedded structures indicative of spurious features from the spectrometer. The residual to a maximally smooth fit is shown in Fig. 9. As seen from Fig. 9, there are no obvious spectral structures in the residual. The individual calibrated spectra have RMS noise of 1.75 K, consistent with the system temperature, integration time, and propagation through the calibration process. The residual spectrum shown in the bottom trace in Fig. 9 has an RMS noise of 22.8 mK, at a native spectral resolution of 61 kHz. This is consistent with the expectation from integration over 17 h that average over 7283 spectra. We have then smoothed the residual to examine for lower amplitude spurious structure. Smoothing and degrading the spectral resolution from the native 61 kHz all the way to 3.9 MHz reduces the RMS noise to 2.7 mK.

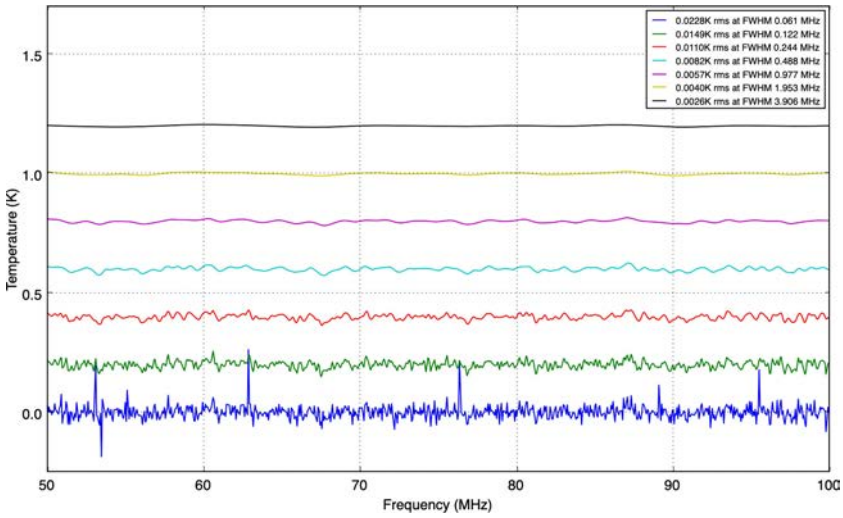

Fig. 9. Residuals on fitting out a maximally smooth polynomial from the measured spectrum. The maximum-resolution residual spectrum is shown as the lowest trace, with traces above that obtained by smoothing to progressively lower spectral resolutions. The full-width at half maximum (FWHM) of the smoothing kernel and the RMS of the amplitudes of the smoothed spectra are given in the legend.

We show the reduction in the variance of the residual with smoothing scale in Fig. 10. The logarithm of the variance decreases in inverse proportion to the increase in smoothing window FWHM, demonstrating that there are no unwanted spurious structures contributed by the digital spectrometer to this sensitivity level of a few mK.

This laboratory test of the SARAS correlator performance validates its capability for detecting CD/EoR spectral features that may have amplitudes 20 mK to 200 mK.

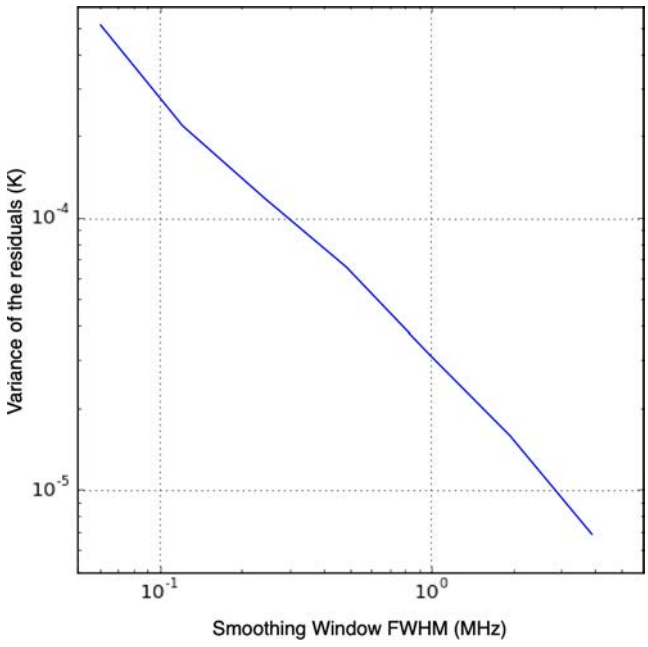

Fig. 10. Run of variance in the residual versus FWHM of the smoothing window.

4. Summary and Future Work

As part of the SARAS experiment that aims to detect the weak 21 cm global signal from CD/EoR, we have developed a digital correlation spectrometer system capable of processing a baseband analog signal pair with up to 250 MHz bandwidth. The RF signals from SARAS antennas are processed in analog signal chains and provided to the digital receiver as a pair of baseband analog signals; in the digital receiver, the signals are digitized, then channelized using windowed FFTs to yield spectra with resolution of 61 kHz, thus producing self- and cross-power spectra of the two analog inputs. A high side lobe suppression of 80 dB is provided by the window function; thus even if RFI as strong as 10^6 K is present, the spillover across the band into other channels is limited to be below 10 mK. The 10-bit ADC has a two-tone, third-order intermodulation performance of 53 dBc that suggests that, if unwanted spectral structure due to intermodulation distortion of closely spaced multiple RFI signals is to be less than the CD/EoR signal strength of 20 mK to 200 mK, strength of multiple RFI signals — if present — needs to be well below 2000 K. In the operating band, the RF-shielded enclosure that houses the integrated spectrometer, along with the external battery units and interconnections, provides about 75 dB attenuation of electromagnetic

signals generated inside the enclosure. Since the SARAS antenna is deployed at least 100 m away from the enclosure, the combination of RF isolation provided by the enclosure and space loss ensures that at the antenna terminals RFI from the digital receiver has strength less than 1 mK. We have evaluated the system performance with long duration acquisition of data with the antenna replaced by an RLC network that mimics the reflection coefficient amplitude of the SARAS antenna; analysis of the data demonstrates that the digital correlation spectrometer is capable of providing spectra with spurious spectral structure well below the expected amplitudes of CD/EoR 21 cm signals.

The SARAS digital correlation spectrometer performance is currently limited primarily by the analog-to-digital converter — the sampler — owing to the limited number of quantization levels; therefore, future upgrades are to change the analog-to-digital converter to an improved device with 14 bits of precision and hence improved dynamic range and linearity performance. Comparison of specifications of commercially available 14-bit, 500 Ms/s ADCs to replace the existing 10-bit ADCs is underway. The SARAS 3 radiometer has been integrated and extensively tested end-to-end in laboratory conditions and members of the team are traveling to remote regions in search of a suitable location (manageable RFI level) to deploy the SARAS 3 radiometer and carry out the much needed observations.

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