Offset, Gain and Phase Calibration of Quad ADC EV10AQ190

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Abstract

Due to technological limitations, commercial ADCs having multi-gigahertz sampling bandwidth and high bit precision (≥ 6 bits) are not easily available. For wide bandwidth applications, one option to enhance the sampled bandwidth is to time-interleave multiple ADC cores within a package. In an ideal scenario, parameters like DC offset, gain, phase and bandwidth of individual ADC cores within a package are identical. However, due to variations in the ADC manufacturing processes, the above parameters may not be identical in all ADC cores. Modern time-interleaved ADCs provide programmable features to calibrate these parameters so as to obtain optimal spurious-free dynamic-range performance.

Introduction

Array of **P**recision **S**pectrometers for the **E**poch of **R**ecombin**a**tion - **APSERa** is a project to detect recombination lines from the Epoch of Cosmological Recombination. **APSERa** is likely to consist of an array of 128+ purpose-built small telescopes, operating in the frequency range of 2 - 6 GHz. A digital signal processing platform consisting of high-speed analog-to-digital converter (ADC) and FPGA with capability to digitize and process data samples in real-time is being designed and developed. From our ADC survey, we found that there were not many options for a commercial ADC capable of sampling an analog signal having a bandwidth of about two to three gigahertz. Requirements of wide band digitizer had to be met by time-interleaving multiple, high-speed ADC cores within a single package or multiple ADC chips. EV10AQ190, a quad 10-bit, 1.25 GSps ADC from e2V technologies, was found to be a suitable choice for our signal processing platform. It has provision to time-interleave all four

cores or in two sets of two cores. The ADC, internally, distributes sampling clock to four cores at appropriate phases, so that, when all four cores are time-interleaved, a maximum sampling rate of 5 GSps is obtained.

As the requirement of **APSERa** is to sample two, quadrature (I-Q) analog signals, each having a bandwidth of about 2 GHz, ADCs are configured to time-interleave in groups of two, thereby, effectively sampling at 2 GSps. Fig-1 shows a picture of two EV10AQ190 ADCs configured in sets of two for **APSERa** requirement. The ADCs are interfaced to an FPGA for real-time processing of samples streaming out of individual ADC cores.
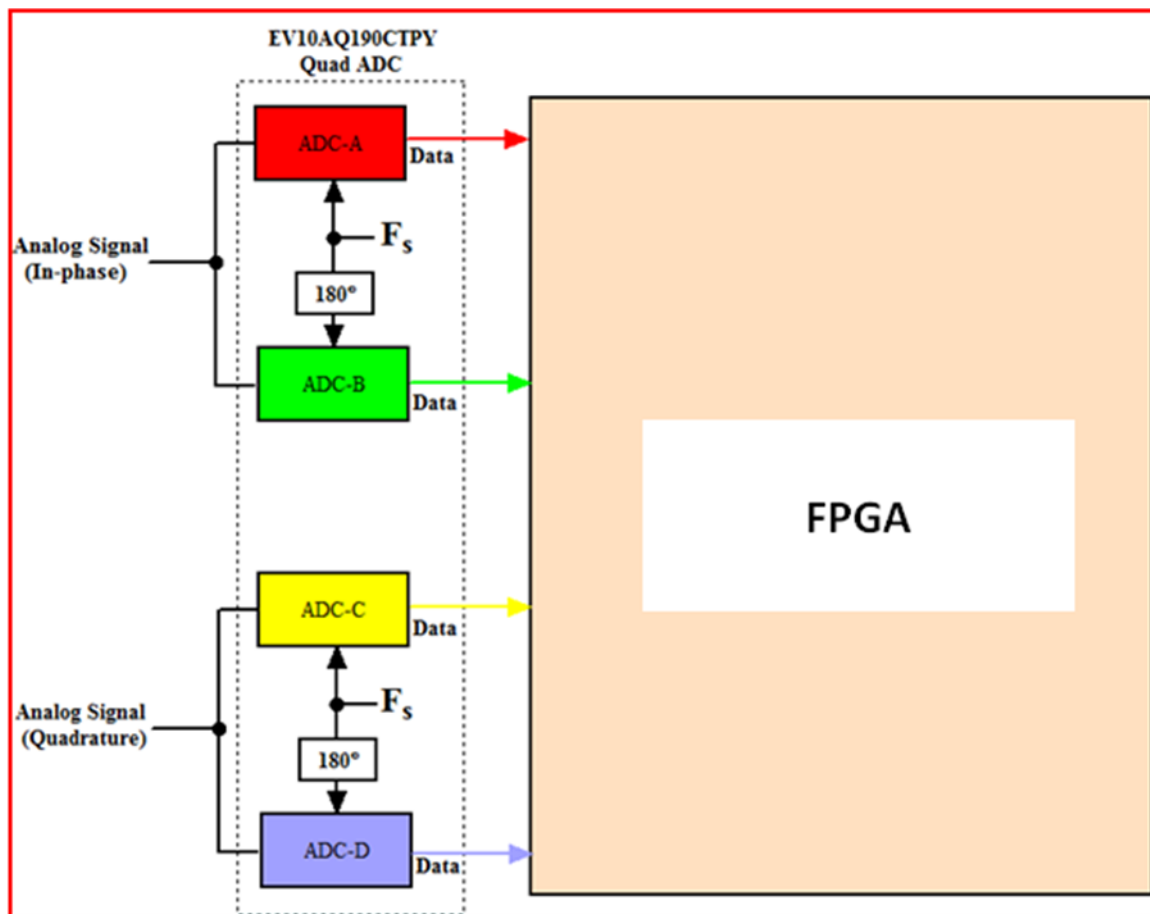

Fig-1: Configuration of time-interleaved ADCs for APSERa

The individual cores of the quad ADC (Core A, B, C and D), each having an analog input bandwidth of about 3 GHz, is capable of sampling analog signals up to 1.25 GSps. While time-interleaving facilitates sampling of broadband signals, distortion products (spurs) as a result of gain-, phase-, bandwidth- and offset-mismatch between time-interleaved ADC channels present a significant challenge in optimal performance of ADC.
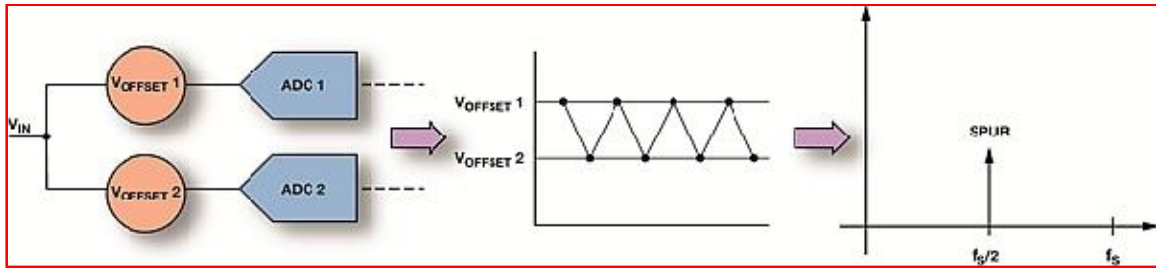
Fig-2: Effect of offset mismatch between time-interleaved ADCs

Fig-2 depicts the effects of DC offsets in individual ADC cores. If F_S is the effective sampling rate of the time-interleaved ADCs, the output switches between these offset values at a rate of $F_S/2$. This will result in a spur in the output spectrum located at $F_S/2$. Since the mismatch itself does not have a frequency component and is only at DC, the frequency of the spur that appears in the output spectrum only depends on the sampling frequency and will always appear at a frequency of $F_S/2$. The magnitude of the spur is dependent upon the magnitude of the offset mismatch between the ADCs and is independent of analog input signal (F_{in}) and its amplitude.
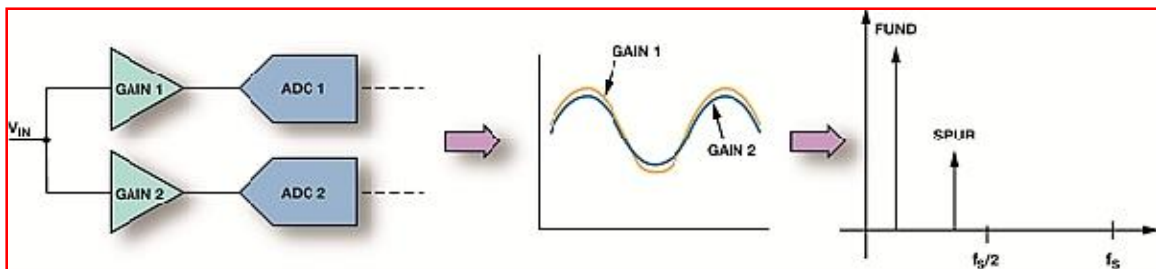

Fig-3: Effect of gain mismatch between time-interleaved ADCs

The gain mismatch will result in a spur in the output spectrum that is related to the input frequency as well as the sampling rate and will appear at $F_S/2 \pm F_{in}$. In order to minimize the level of the spur caused due to gain mismatch, the gain of one of the time-interleaved ADCs is chosen as reference and the gain of the other ADC is adjusted till it is compares very closely with the reference ADC. Fig-3 shows the effect of gain mismatch between two time-interleaved ADCs. When two ADCs with gain mismatch are time-interleaved, largest error occurs at peak amplitude.

Fig-4 shows the effect of phase mismatch between two time-interleaved ADCs. This is the timing mismatch between the two ADCs as shown in Fig

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5. The timing mismatch has two components, group delay in the analog section of the ADC and clock skew. The analog circuitry within the ADC has an associated group delay and the value can be different between the two ADCs. In addition, there is clock skew that has an aperture uncertainty component in each of the ADCs and has a component related to the accuracy of the clock phases that are input to each converter.

Similar to the gain mismatch spur, the timing mismatch spur is also a function of the input frequency and the sample rate and appears at $F_S/2 \pm F_{in}$. In order to minimize the resulting spur, the group delay through the analog section of each converter needs to be properly matched with good circuit design techniques. In addition, the clock path designs need to be closely matched to minimize aperture uncertainty differences. And lastly, the clock phase relationships need to be precisely controlled such that the two input clocks are as close to 180° apart as possible. As with the other mismatches, the goal is to attempt to minimize the mechanisms that cause the timing mismatch. When two ADCs with phase mismatch are time-interleaved, largest error occurs during highest slew rate (zero-crossings for a sinusoidal signal).
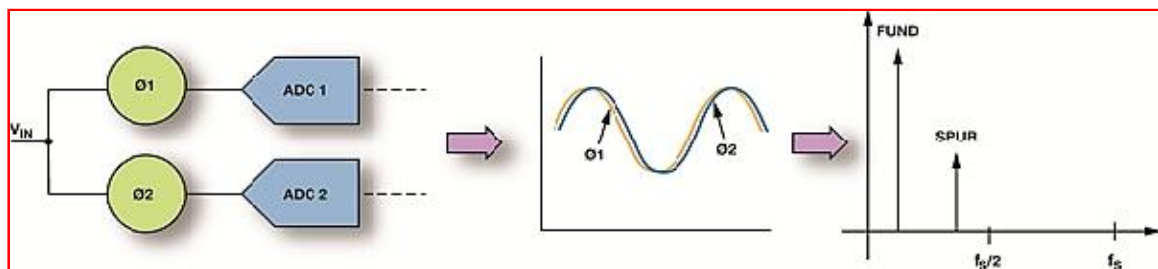

Fig-4: Effect of phase mismatch between time-interleaved ADCs

Fig-5 shows a power spectrum of output samples from two time-interleaved ADC cores of pSPEC sampling a tone at 156.25 MHz at 2 GSps. Offset mismatch between ADC cores produces a spurious component at one-half of the sampling rate (Fs/2), i.e. 1 GHz. Gain- and phase-mismatch between the cores produces another spurious component at {(Fs/2) - 156.25 MHz} = 843.75 MHz. These spurs reduce the spurious-free dynamic-range (SFDR) of the time-interleaved ADCs.
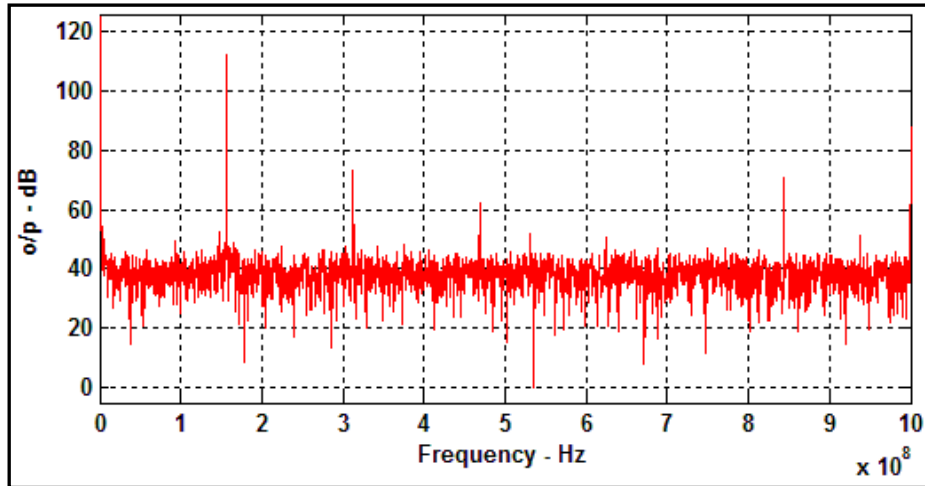
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Fig-5: Spurious components from two time-interleaved ADC of pSPEC

Challenges in time-interleaving ADCs

Modern ADCs have in-built features to correct the mismatches described. For example, the challenging tasks of providing analog input to multiple ADC cores and providing required phase offset in the sampling clock are made part of the IC design process. Only finer gain and phase adjustments are left to the user so that optimal ADC performance could be realized. In the case of 10-bit EV10AQ190 ADC, the best (theoretical) signal-to-noise ratio that can be obtained is ~62 dB. If two, 10-bit ADCs are time-interleaved to enhance the sampled bandwidth, to obtain a system performance of ~62 dBc, gain matching and phase matching (clock skew) between time-interleaved ADCs should be better than 0.1% and 0.04 degrees (~120 femtoseconds) respectively, for an input tone having a frequency of 1000 MHz.

Features for OGP Calibration in EV10AQ190

The EV10AQ190 ADC has on-chip features to compensate offset, gain and phase offsets across ADC cores. In this report, we describe the compensation methodology adopted and feature of the associated hardware and software that aid in implementing the compensation scheme. EVAOAQ190 has in-built 10-bit registers for offset, gain and phase (OGP) correction. A pre-computed 10-bit value can be written into these registers inside the ADC through a three-line serial programming interface (SPI). Details of the 10-bit offset correction register are as shown in Fig-6. Considering that the ADC full-scale voltage is ~500mV$_{p-p}$ and there are 1024 levels within this range, value of least significant bit (LSB) is about 0.4882 mV. The offset correction register can compensate for offset mismatch between ADC cores ranging ± 40 LSB, in steps of 0.08 LSB (40μV). Similarly, the gain correction register can compensate for ±10% gain mismatch between ADC cores, in steps of 0.02%. Phase correction register can compensate for clock skew mismatch of about ±15 ps, in steps

of ~30 femtoseconds. As evident from these features, gain matching to 0.1% and phase matching to ~120 femtoseconds is possible.

External Offset Control Register Description

Bit label	Value	Description	Default Setting
EXTERNAL OFFSET X<9:0>	0x000	Maximum positive offset applied	0x200 0 LSB Offset
	0x1FF	Minimum positive offset applied	
	0x200	Minimum negative offset applied	
	0x3FF	Maximum negative offset applied	

Notes   1: Offset variation range: ~+/- 40 LSB, 1024 steps.
2: Current offset of the selected channel is controlled by the External Offset Control Register but is updated only upon request placed through the SPI in the CAL control register of the selected channel.
3: The transfer function of the ADC is given by the following formula transfer function result = offset + (input*gain).

External Gain Control Register Mapping: address 0x22

Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Unused						EXTERNAL GAIN X <9:0> (See Notes)									

Table 44.   External Gain Control Register Description

Bit label	Value	Description	Default Setting
EXTERNAL GAIN X <9:0>	0x000	Gain shrunk to min accessible value	0x200 0 dB gain
	0x200	Gain at Default value (no correction, actual gain follow process scattering)	
	.....		
	0x3FF	Gain Increased to max accessible value	

Notes   1: Gain variation range: ~+/-10%, 1024 steps (1 step ~0.02%).
2: Current gain of the selected channel is controlled by the External Gain Control Register but is updated only upon request placed through the SPI in the CAL control register of the selected channel.
3: The transfer function of the ADC is given by the following formula transfer function result = offset + (input*gain).

External Phase Register Mapping: address 0x24

Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Unused						EXTERNAL PHASE X <9:0> (See Notes)									

Table 48.   External Phase Control Register Description

Bit label	Value	Description	Default Setting
EXTERNAL PHASE X <9:0>	0x000	~ -15ps correction on selected channel aperture Delay	0x200 0ps correction on ADC X aperture Delay
	.....		
	0x3FF	~ +15ps correction on selected channel aperture Delay	

Notes   1: Delay control range for edges of internal sampling clocks: ~+/-15 ps (1 step ~30 fs).
2: Actual Aperture Delay of the selected channel is controlled by the External Phase Control Register but is updated only upon request placed through the SPI in the CAL control register of the selected channel.

Fig-6: Offset, gain and phase (OGP) correction register inside ADC
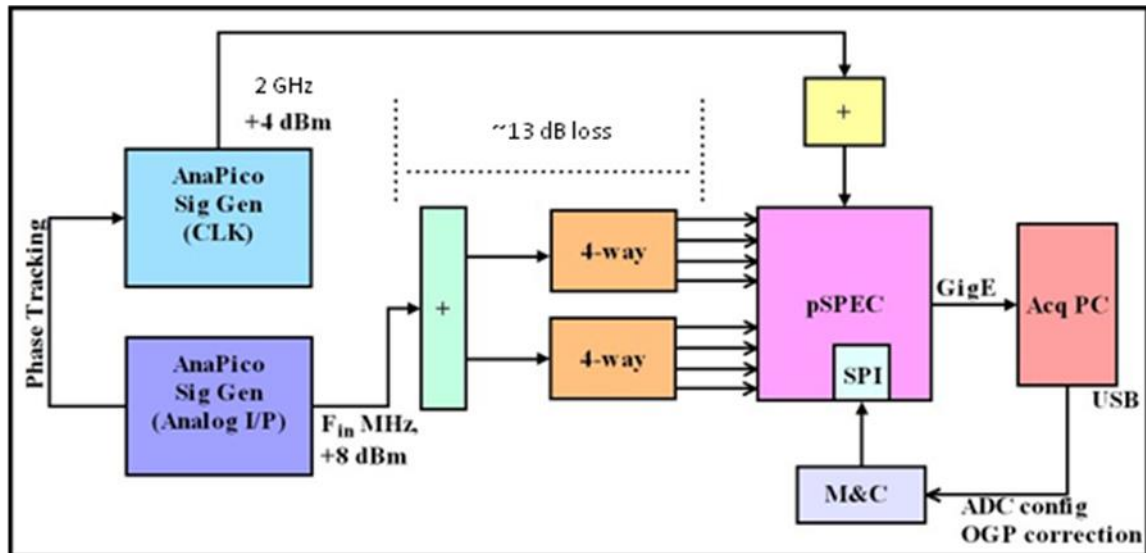
Fig-7: Hardware setup for ADC calibration

Fig-7 shows various blocks that are part of a setup to calibrate ADC mismatches. The sampling clock (F_s= 1 GHz) and analog input (F_{in}) to pSPEC are derived from two Ana Pico signal generators that are phase tracking. Raw voltage samples from individual ADC cores of two EV10AQ190 ADCs are captured using the FPGA, packetized and streamed out via a Gigabit Ethernet interface to an acquisition PC.

Computation of OGP correction values

In the acquisition PC, Matlab routines are used to process the raw voltage samples and extract information related to DC offsets in individual ADC cores, gain mismatch and phase mismatch between pairs of ADC. 4096 voltage samples corresponding to phase-coherent analog input F_{in} presented at the input of all eight ADC cores are sampled at F_s, packetized and acquired in burst-mode form of data acquisition. The mean value, peak value and standard deviation of F_{in} are computed for all eight series to obtain an estimate of DC offsets and gain in each ADC core. Additionally, a 4096-point FFT on each of the eight time series provides information related to phase and peak value (gain) of F_{in}. For each pair of ADCs, taking one of them as reference, gain and phase correction values of the other ADC are computed so as to match that of the reference. The DC offset correction values tend to reduce the DC offset of individual ADC cores to zero. All the correction values so computed are transferred to dedicated registers inside FPGA through a Monitor and Control (M&C) card. The M&C

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card communicates to the acquisition PC via a USB-1 interface. OGP correction values stored in the FPGA registers are sequentially loaded into designated mismatch correction registers. The summary of sequence involved in calibration of ADC is listed below:

1. Configure FPGA in ADC calibration mode
2. Configure ADC to 2-ch time-interleaving mode of operation
3. Set all mismatch correction register of ADC cores to default state
4. Acquire voltage samples from all eight ADC cores via Gigabit Ethernet interface
5. Compute OGP mismatch values of all ADC cores
6. Calculate OGP mismatch compensation/correction values
7. Acquire voltage samples from all eight ADC cores via Gigabit Ethernet interface
8. Compute OGP mismatch values of all ADC cores
9. Repeat steps 4 to 8 if OGP compensation still produces insufficient matching

Results of OGP calibration

Calibration set-up:

1. Time-interleaved ADC pairs for I1: ADC1-A & B; Q_1: ADC1-C & D,
2. Time-interleaved ADC pairs for I2: ADC2-A & B, Q_2: ADC2-C & D
3. Sampling clock (F_s) to individual ADC cores = 1 GHz, -2 dBm
4. Coherent analog input (F_{in}) to all ADC cores = 39.0625 MHz, -6 dBm
5. Number of voltage samples available from each ADC core = 4096
6. Number of voltage samples in one complete cycle of F_{in} = 25.6
7. Number of complete cycles of F_{in} in 4096 samples is equal to 160, which is also the FFT bin number of input tone (F_{in}) to ADC
8. Length of FFT, after time-interleaving of samples = 8192 points
9. Spectral resolution = 244.14 kHz

Fig-8 and Fig-9 show overlapped plots of voltage samples acquired from 2-ch time-interleaved ADC pairs. The mean value, peak value and standard deviation of all four time series for default setting of OGP correction registers are also shown. After DC offset calibration, mean value of all four ADCs was within an ADC count.
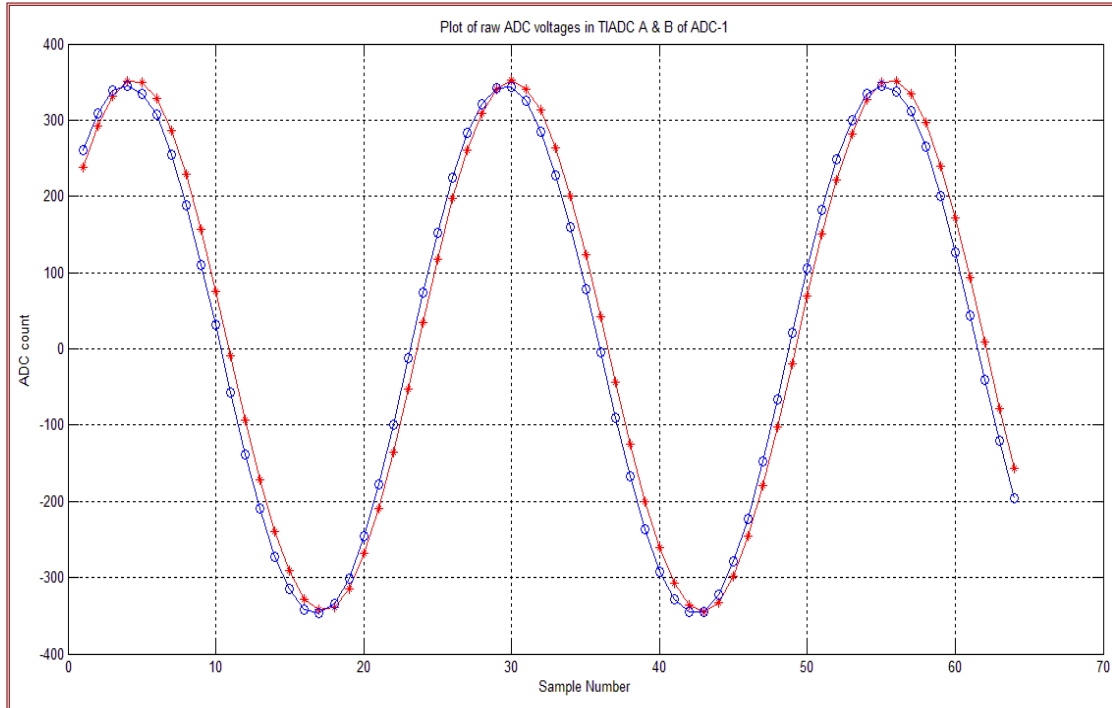
Fig-8: Overlapped plot of voltage samples from ADC1-A (Red) and ADC1-B (blue)

➢ Mean(ADC1-A):3.5 ADC counts;   Mean(ADC1-B):2.0 ADC counts
➢ Peak(ADC1-A): 349.09;   Peak(ADC1_B):348.00
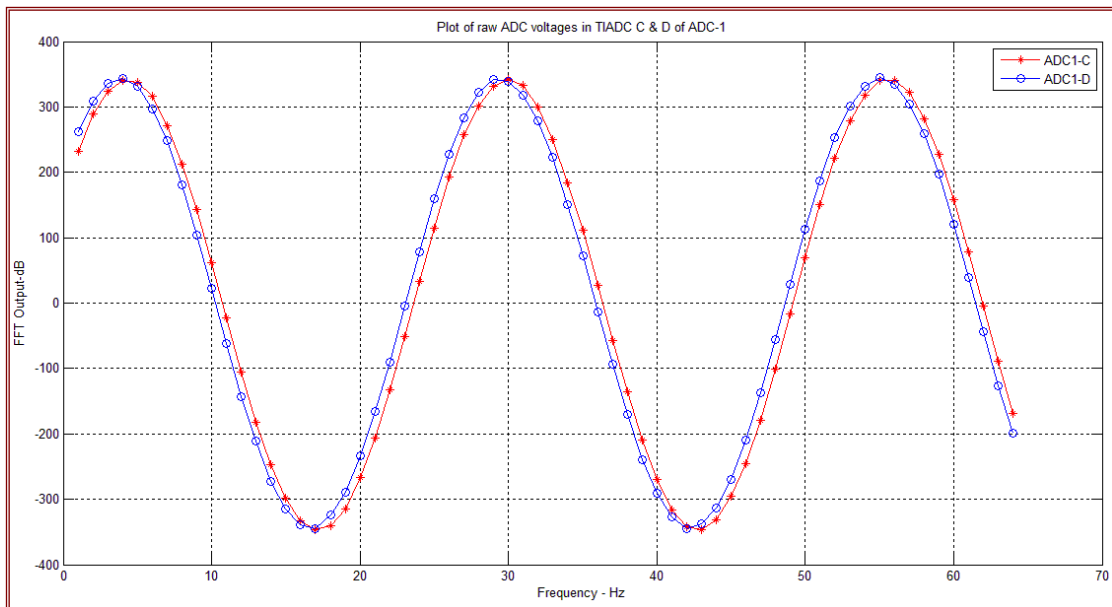➢ STD(ADC1-A):246.84;   STD(ADC1-B):246.07

Fig-9: Overlapped plot of samples from ADC1-C (Red) and ADC1-D (blue)

➢ Mean (ADC1-C): 2.0 ADC counts;   Mean(ADC1-D):0 ADC counts
➢ Peak (ADC1-C): 344.84;   Peak(ADC1_D):343.88
➢ STD (ADC1-C): 243.84;   STD (ADC1-D):243.16

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Fig-10 shows the power spectrum obtained by Fourier transforming data from time-interleaved ADC pair 1A and 1B, for default settings of OGP correction/compensation registers. Spurs at $F_s/2 = 1$ GHz and ($F_s/2 - F_{in} = 960.9375$ MHz) are clearly visible and their levels are 82 dB and 67 dB. Power of input tone Fin=39.0625 MHz, which appears at FFT bin number 161 in the power spectrum, is 123 dB. Level of spurious components is about 41 dB and 56 dB below the carrier. As shown in Fig-11, level of spurious components is about 43 dB and 57 dB below the carrier level of 122.87 dB.
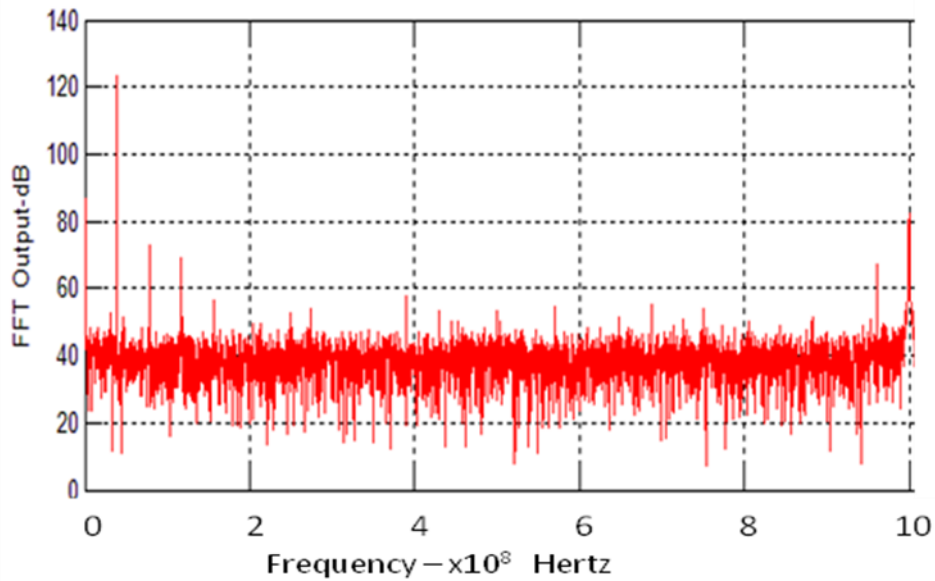

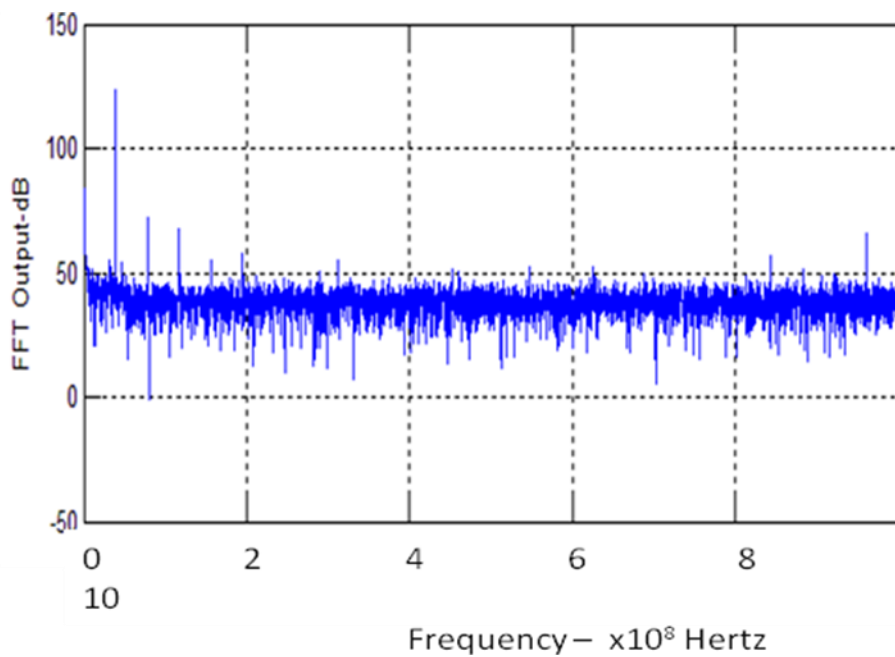Fig-10: Power spectrum of time-interleaved ADC pair 1A and 1B

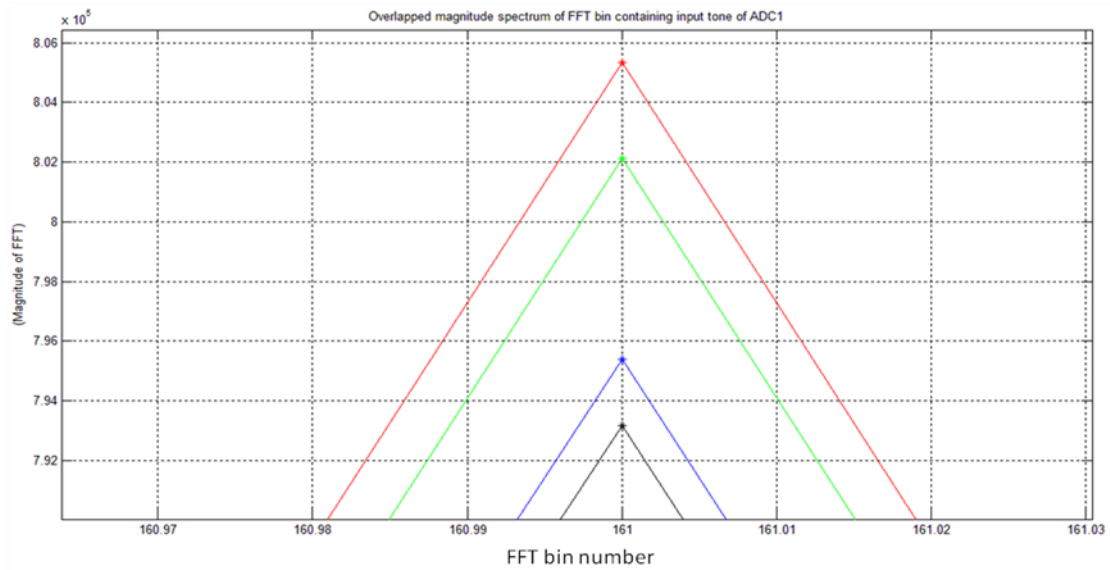Fig-11: Power spectrum of time-interleaved ADC pair 1C and 1D

Fig-12: Overlapped spectrum of all four cores of ADC1 for Fin=39.0625 MHz, default OGP
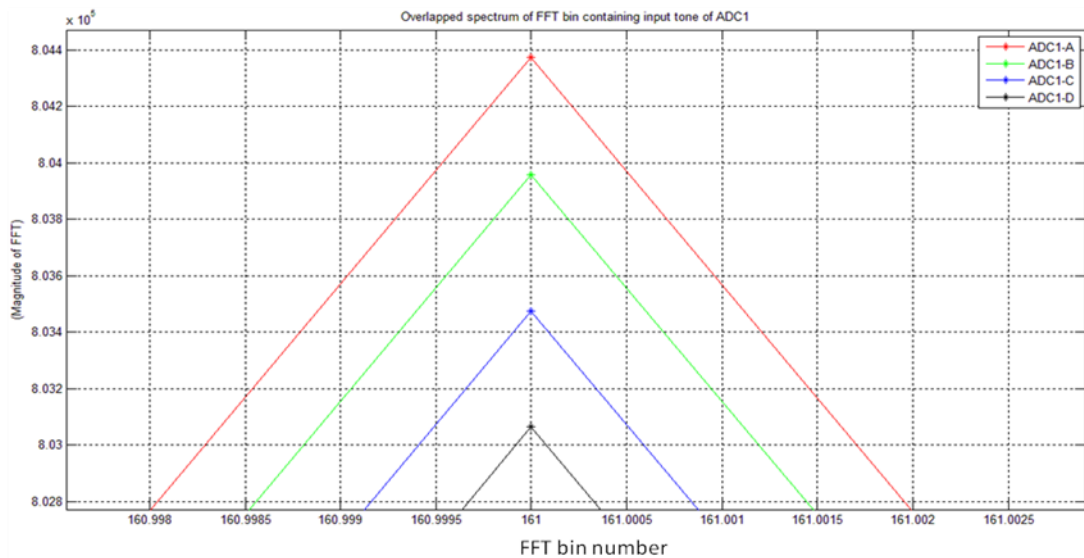

Fig-13: Overlapped spectrum of all four cores of ADC1 after DC offset and Gain correction

As shown in Fig-12, difference in peak power level of F_{in}= 39.0625 MHz between ADC pair 1A and 1B is (8.053e5 - 8.021e5) = 3200 in units of abs (FFT) and that of ADC pair 1C and 1D is (7.954e5-7.931e5) = 2300. After calibration, the above pairs of ADC1 for DC offset and gain, as shown in Fig-13, difference in peak power levels are (8.0435e5 - 8.0395e5) = 400 and (8.035e5 – 8.0305e5)= 450, respectively. In logarithmic scale, difference in peak power level for the two ADC pairs is 0.004 dB and 0.0048 dB, respectively. Peak power levels in both ADC pairs are within ~0.05%, better than the required gain matching of 0.1% for APSERa application.

Fig-14 shows overlapped power spectra of ADC pair 1A-1B and 1C-1D after DC offset and gain calibration, but phase set to default. As depicted in the top plot, for ADC pair 1A-1B, spurs at $F_s/2 = 1$ GHz and ($F_s/2$ - F_{in} = 960.9375 MHz) are at FFT noise floor level of ~35 dB and 55 dB respectively. Prior to DC offset and gain calibration, these levels were: 82 dB and 67 dB respectively. So, with respect to tone power of 123 dB, spurious components are 87 dB and 67 dB below carrier. As shown in the bottom plot of Fig-14, similar performance is obtained for ADC pair 1C-1D.
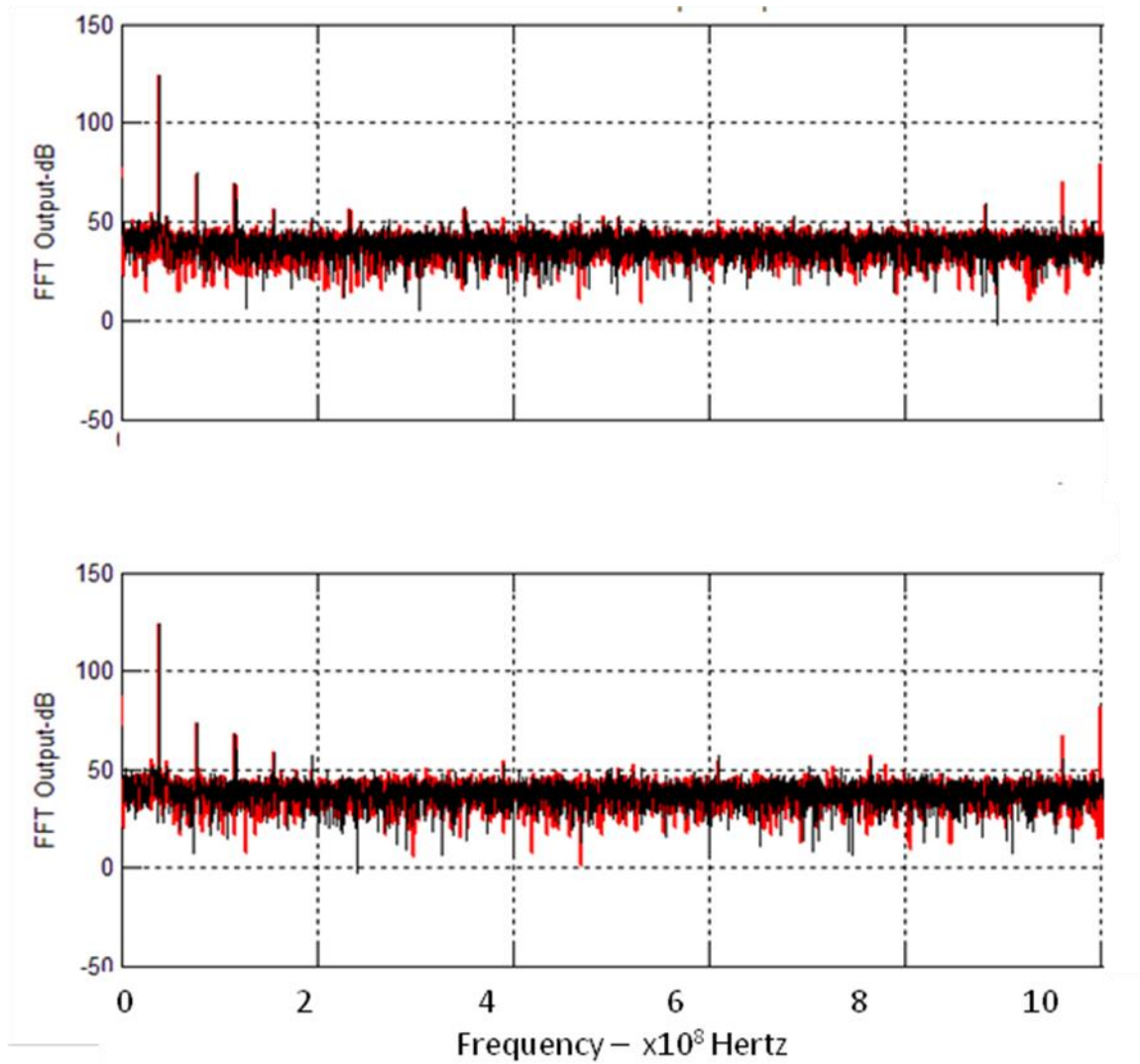

Fig-14: Overlapped power spectra of ADC pair 1A-1B and 1C-1D after calibration

The calibration procedure described above were repeated at analog input frequencies F_{in} set to 156.25 MHz and 312 MHz. Considering the higher input frequencies and the associated faster slew rates, expectedly, degraded calibration results were obtained. However, it must be noted that, in practice, the ADC in 2-ch time-interleaved mode of operation for quadrature sampling requirements of APSERa, would be sampling a noise band input having a bandwidth of ~2 GHz.

Conclusion

Time-interleaving of individual ADC cores of EV10AQ190 in 2-ch mode of operation has been demonstrated in pSPEC. By interleaving two ADC cores, quadrature sampling requirement of effective sampling rate of 2 GSps has been realized. Although level of spurious components generated - even after calibration of DC offset, gain and phase mismatch between time-interleaved ADC pairs - cannot be totally eliminated, it has been demonstrated that their levels can be significantly reduced. Using ADC's on-chip programmable mismatch correction features, the results obtained compare favourably with expected levels of suppression of spurious components. If calibration of time-interleaved ADC is carried out for input tones centered at the middle of the band and at either band edges, a mean value of OGP correction values can be used for the entire band. Instead of spurious components that appear at $F_s/2$ and ($F_s/2$ - F_{in}) for a tone input at frequency F_{in}, for input consisting of band-limited noise, output spectrum from 2-ch time-interleaved ADC is contaminated with an attenuated and flipped version of the input band.

References

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Revision History

v1.0 – April, 2017