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Miniaturised Portable Dual-Channel Receiver for Radio Astronomical Observations

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Abstract :

For carrying out sky observation at multiple / remote sites without having to spend significant amount of time in setting up the experiment, it is essential that the radio receiver be portable and compact in size. It features an improvement in the performance and reliability due to i) the use of miniaturized electrical components in the circuit which have good performance characteristics over a wide range of frequencies and ii) significant reduction in the number of connectors required for establishing electrical connectivity in the RF circuit. This report describes a compact portable dual channel receiver built to have these features and operate in the nominal frequency range of 100 – 1000 MHz. It has an instantaneous bandwidth of 14 MHz selectable anywhere in the whole range of above the frequency band. The analog receiver is superheterodyne in nature, converting the RF input signal to an IF centred around 140 MHz using an appropriate local oscillator. The receiver has a noise temperature of approximately 430 K over the entire receiver band and a gain of 65 dB. It has an input 1 dB compression point at an input level of -60 dBm and third-order intercept point at the input level of -55 dBm. The digital back-end receiver Nyquist samples the IF band, employing 8-bit digitization for the pair of channels and records directly the raw voltage time-sequences corresponding to 16 MHz bandwidth. The dual channel capability allows full polarisation measurement when the inputs are from a dual-polarisation antenna, as well as interferometric measurements with a pair of antennas, usually with same polarisation.

1. Introduction

Conventionally, receiver systems are built using discrete RF modules connected together with several co-axial cables. Such configurations will have limitations in terms of volume, size, cost, mobility, reliability and stability. To improve upon these aspects, it is necessary that the receiver system be made compact by using miniaturized components and less number of cable connectors. Based on these thoughts, a compact receiver receiver has been designed and built to operate in the frequency range of 100-1000 MHz. Our receiver is capable of handling dual polarization outputs of an antenna by having identical electronics for both the polarization channels. It is a superheterodyne receiver converting the input RF signal into an IF output centered at 140 MHz. The instantaneous bandwidth of the receiver is about 14 MHz. The motivation in developing the compact front end receiver is given in section II. Section III describes the analog front-end receiver in detail about the receiver configuration. Fabrication details are given in section IV and test/measurement results are in Section V. Section VI describes the digital back-end system, section VII describes the control and data analysis software and section VIII concludes with the summary of work carried out.

2. Motivation

The scientific motivation for building a compact and portable receiver system is to make possible sky observation in different sites with less effort setting up, and to have improved reliability in the performance of the entire receiver system. It is also thought that if the receiver is made generic with dual channel processing capability, it will be useful for a variety of radio astronomical observations and antenna configurations.

3. Description of the Portable Dual Analog front-end receiver:

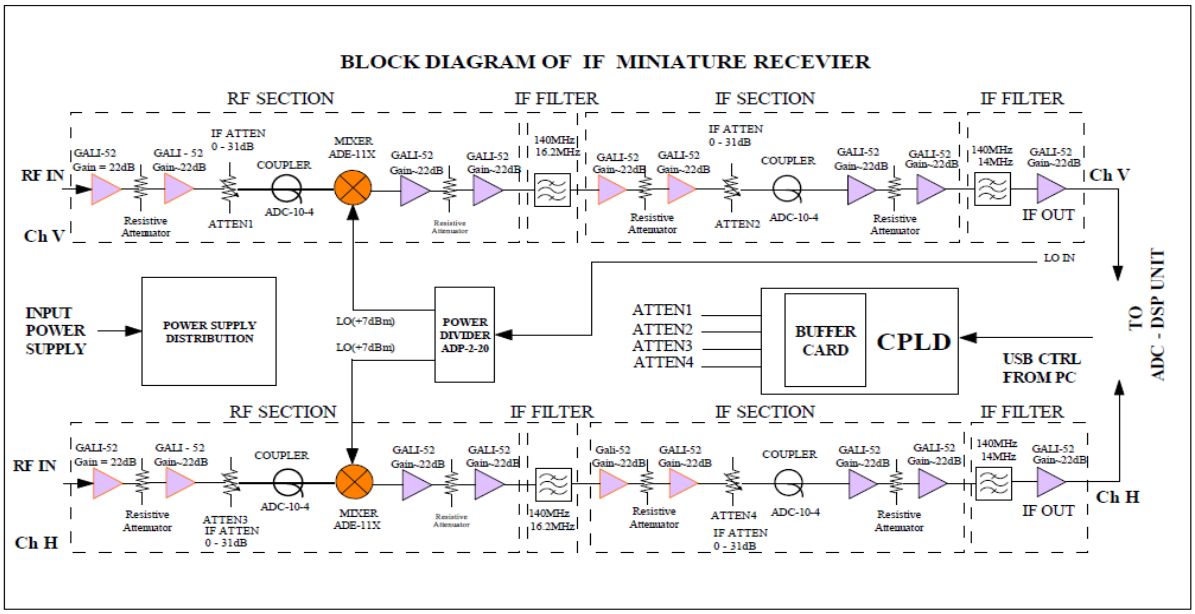

Figure 1. Block diagram of the Portable Dual Analog front-end Receiver

5in the frequency range 100-1000 MHz is as shown in the Figure 1. The input RF signal is amplified and down converted to 140 MHz using a mixer and a suitable local oscillator (LO) input. The frequency of LO is chosen appropriately while selecting the RF signal in the band mentioned above. Care should be taken to filter out contributions at potential image band (using what are called “anti-aliasing” filters). The down converted signal is band limited to the 14MHz using a SAW filter in the IF section. The IF outputs are brought out for ready connection to the inputs of the Digital back-end, where they are digitized using high speed samplers. A pair of digitally controllable attenuators are provided, separately in both in the RF and IF sections, to control the power level of the signals required. A computer control via a USB port sends the control words which are decoded through a CPLD interface to the attenuators, to choose the attenuations in the signal paths .

3.1 RF Section

The RF section consists of Gali-52 amplifiers, variable attenuators (DAT31R5-SP+), 10 dB coupler (ADC-10-4) and a mixer(ADE-11X). The input RF signal in the frequency range 100-1000 MHz is amplified and down converted to 140 MHz IF using the mixer. The mentioned frequency range for RF is only nominal, and the response of the receiver is mainly

limited by the spectral response of the components. In the present case, the components used allow operations well beyond the mentioned frequency range (30 MHz – 2GHz). The overall gain of the RF section could be varied from 24dB to 56dB using the variable attenuators provided. The power level of the RF signal is monitored using a 10dB directional coupler (which has significant attenuation beyond 1GHz). The schematic diagram, prototype and the gain characteristics of the RF section are shown in Figures. 2, 3 and 4. The RF section is observed to have an overall gain droop of about 7 dB in the above mentioned band.

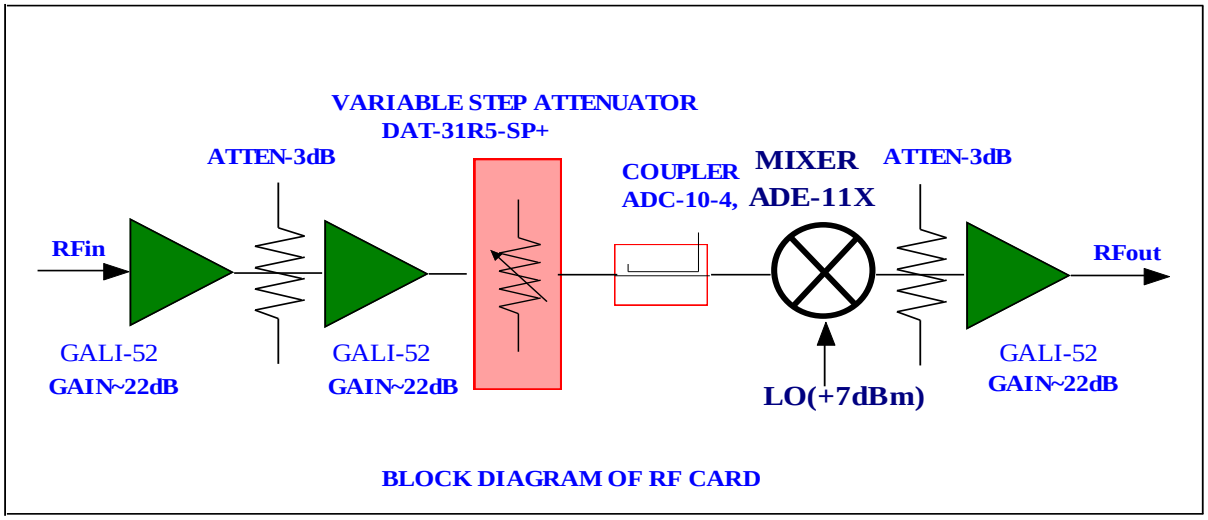

Figure 2 Schematic diagram of the RF section

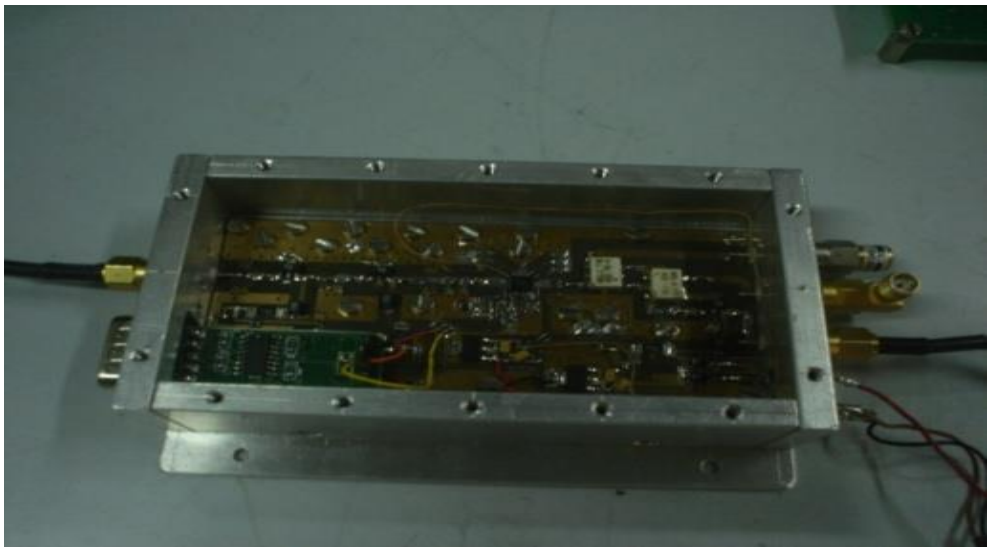

Figure 3 Prototype of the RF module

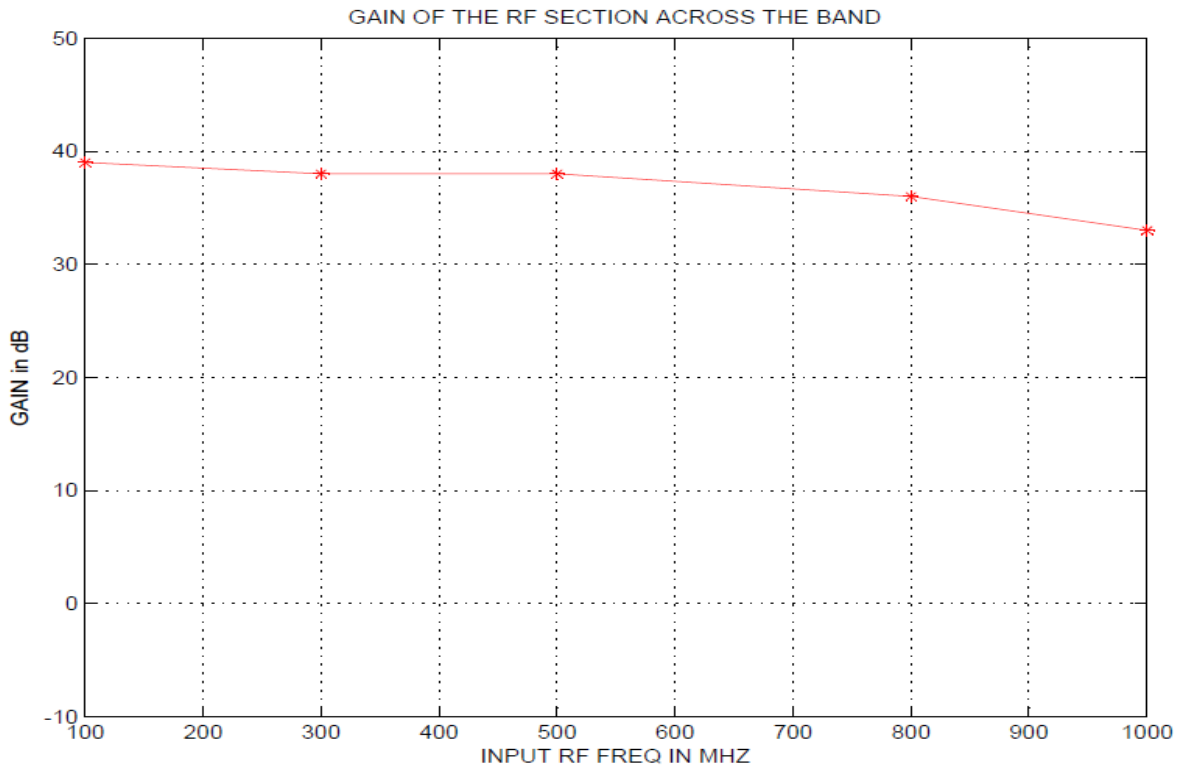

Figure 4 Gain characteristics of the RF section with attenuators set at 16 dB

3.2 IF Selection Filter :

The IF signal is bandlimited to 16 MHz around 140 MHz in this post mixer stage, to reject the other products at the output of the mixer. This band-limiting is achieved using a SAW filter, which has approximately 30 dB roll off at 10 dB below the passband (40dB form factor=1.18). This filter can be replaced by any other suitable filter having alternative desired specifications. The schematic diagram, prototype and the gain characteristics of this section are shown in Figures 5, 6 and 7.

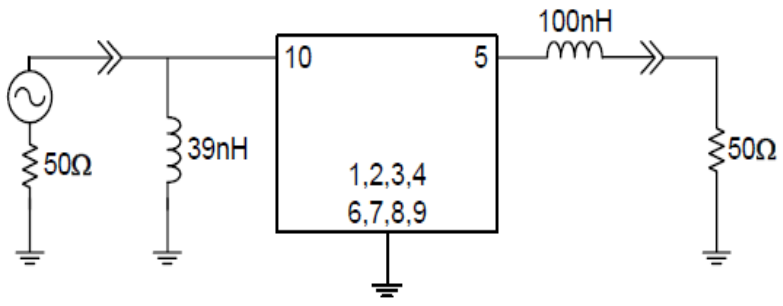

Figure 5 Schematic diagram of the IF SAW FILTER section

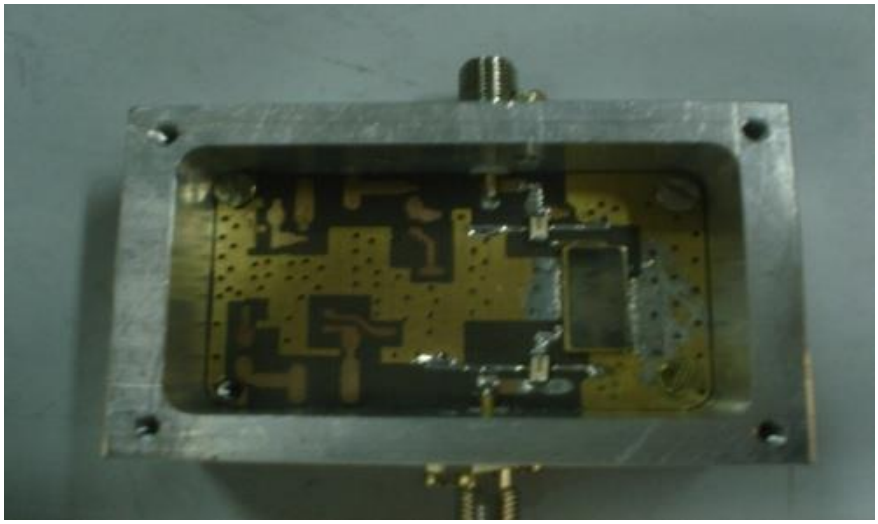

Figure 6 Prototype of the IF SAW Filter module

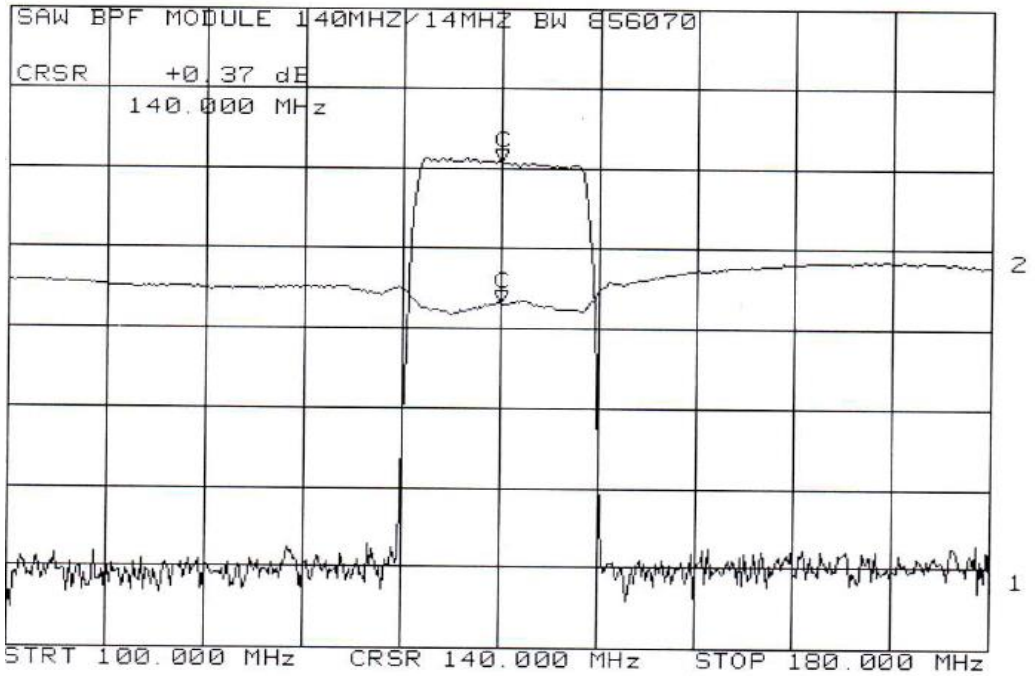

Figure 7 Characteristics of the IF SAW Filter section.

3.3 IF Section

In this section, IF signal is amplified before digitizing using the sampler. The total gain provided in this section using Gali-52 amplifiers is about 85 dB. However, it can be varied over the range 85dB to 55dB using variable attenuators (DAT31R5-SP+). A 10 dB coupler (ADC-10-4) is used in this section to monitor the IF power. The schematic diagram,

prototype and the gain characteristics of the IF section are shown in Figures 8, 9 and 10. The IF section has an overall gain droop of about 5 dB in the 500 MHz to 1 GHz range, a point to note when an alternative IF frequency were to be chosen in that range. The output of IF section is amplified using an IF amplifier and is further band-limited to 14 MHz around 140 MHz, to cut down any out-of-band noise introduced since the previous IF filter.

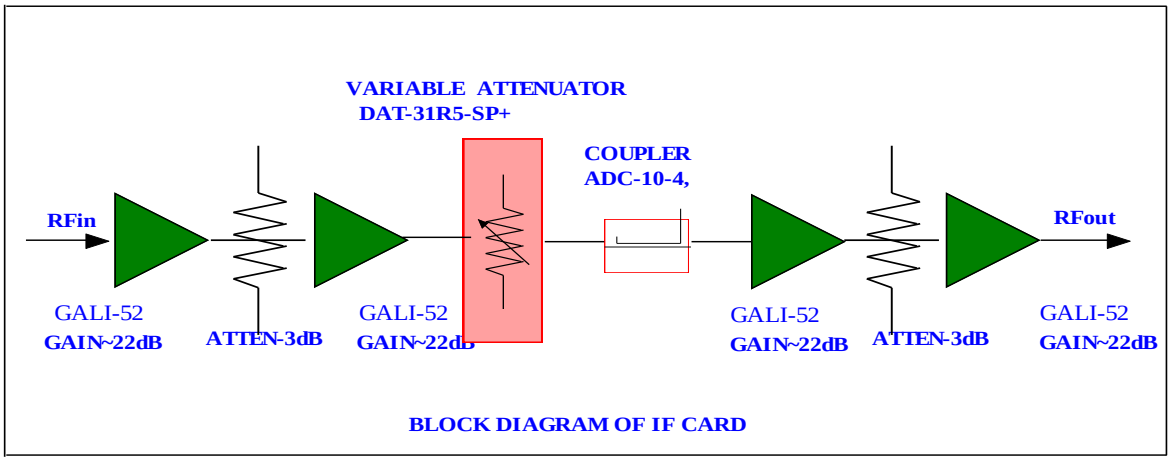

Figure 8 Schematic diagram of the IF section

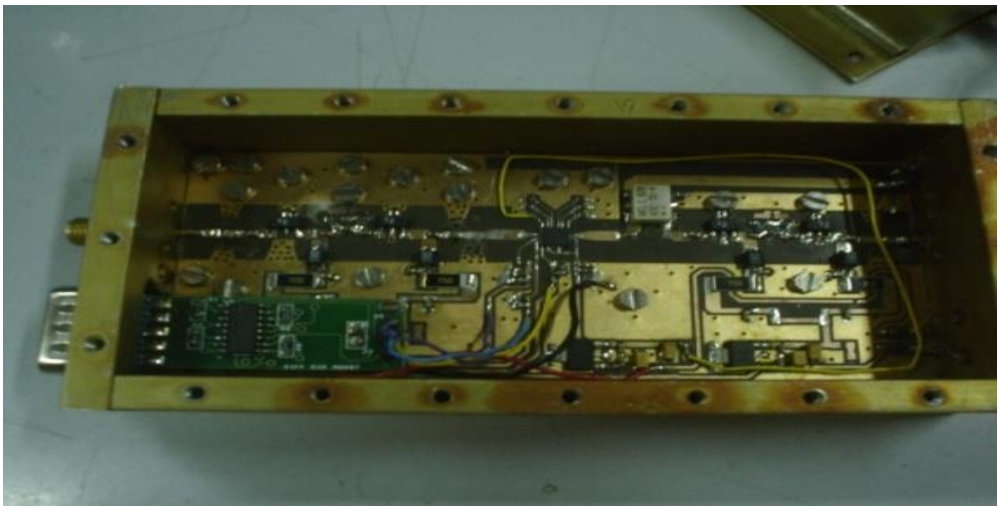

Figure 9 Prototype of the IF module

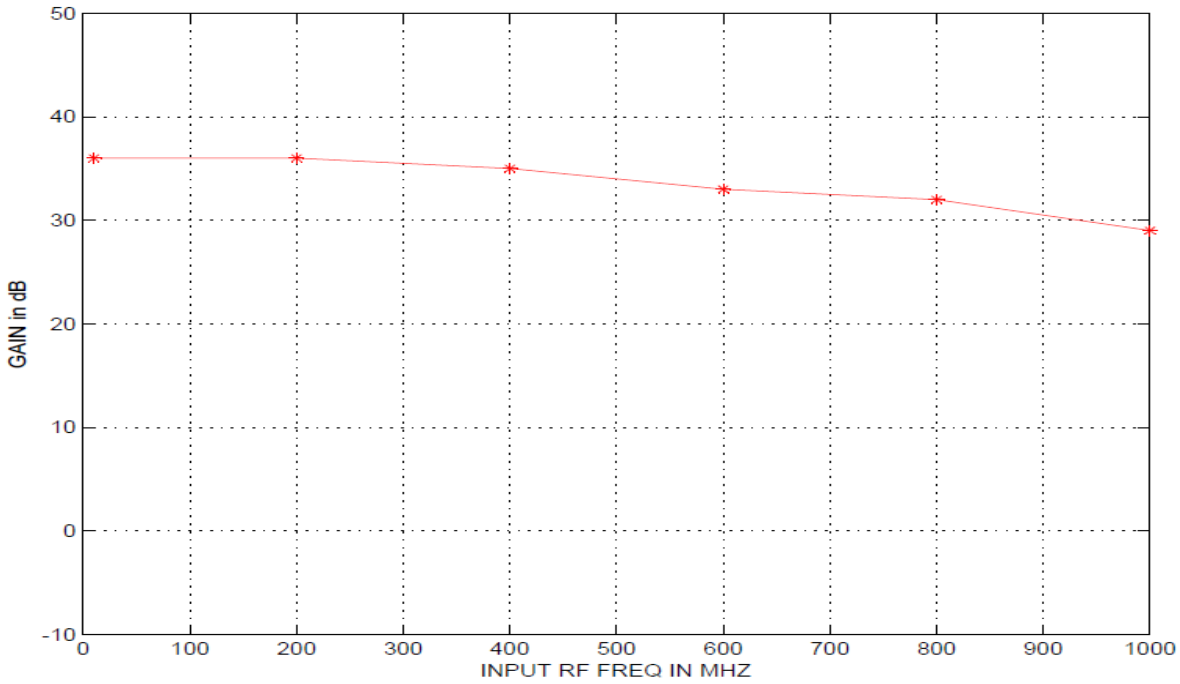

Figure 10 Gain characteristics of the IF section with attenuators set at 16 dB

3.4 Power Supply Section

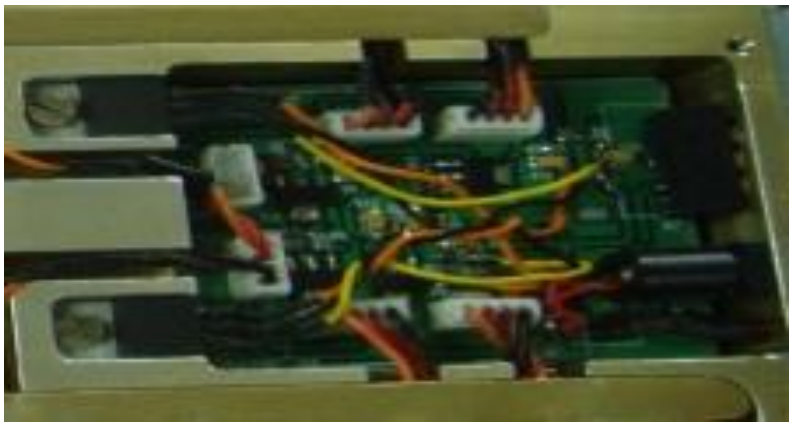

Figure 11 Power supply section

The power supply section distributes required voltage to all the sections in the receiver. The input voltage is 19v from a laptop charger, used as a voltage converter. Voltages +15v, +12v, +8v and +3.3v are derived through regulators from the input voltage. The total current drawn is ~850mA. LED indications are provided for monitoring purpose, on the same side of the chassis where the RF inputs are provided.

3.5 CPLD Section

The DAT-31R5-SP+ is a 50 ohm RF digital step attenuator that offers an attenuation range up to 31.5 dB in 0.5dB steps, operating on a single +3 volt supply. The digital control is a 6-bit serial interface used to select the desired attenuation state.

The digital serial control for setting the attenuation is done through the Computer Universal Serial Bus(USB) port. A standard USB 1.1 card is interfaced to CPLD XCR3128 through a FTDI USB first in, first out (FIFO) chip. The FT245R is a USB to parallel FIFO interface.

The Parallel data from the FTDI enters the CPLD and is decoded to generate three control signals required for the attenuator namely Data, Clock and Latch enable. The Data and the Clock inputs are serially transmitted as shown in figure 12 to the serial interface of the attenuator. The Latch enable is an active high signal.

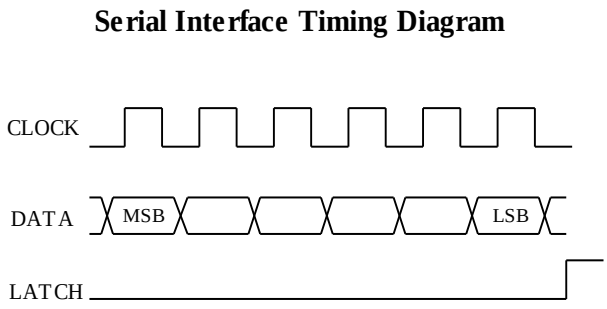

Figure 12. Timing diagram of the attenuator controls

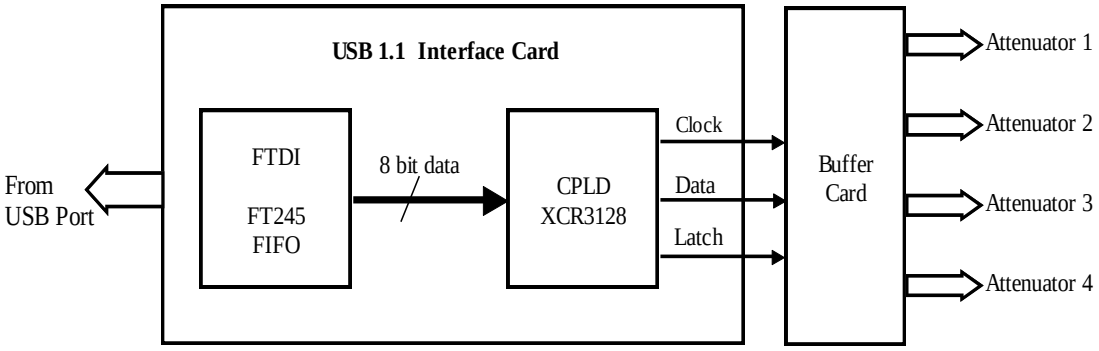

Figure 13 Block diagram of the attenuator controls through USB interface card

Figure 13 shows the block diagram of the attenuator control through USB interface card. The attenuator 1, 2, 3 and 4 corresponds to the two signal channels of the RF and IF signals to be attenuated.

4. Fabrication details

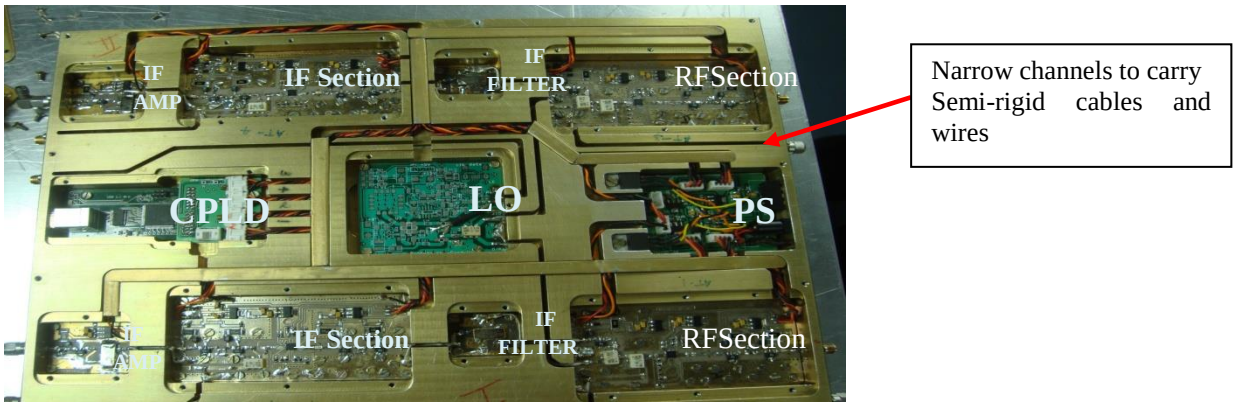

Figure 14. Integrated analog front-end receiver

The subsections of the front end receiver are assembled in single chassis to make it compact and portable. This has been carried out by making cavities corresonding to different sections of the RF chain in one single block of aluminium as shown in Figure 14. Narrow channels are made in the chassis to carry connectorless semi-rigid cables to interconnect suubsections and wires to carry DC supply and digital control words. SMD Feedthrus are used in each of the sections to minimize RF leakage in to the power supply lines. Cavities and channels are covered using aluminium plates and strips of appropriate dimension to minimize radiation leakage from the circuit and the wires. RF input and IF output connectors are provided on both the sides of the chassis. A USB connector is provided to control the signal power levels through the computer.

5. Measurement Results from characterisation of the Analog section (pre-digitisation)

5.1 System Gain: 66dB ± 2dB

The system gain is plotted by varying the RF and LO frequencies for a fixed IF frequency over the entire RF band.

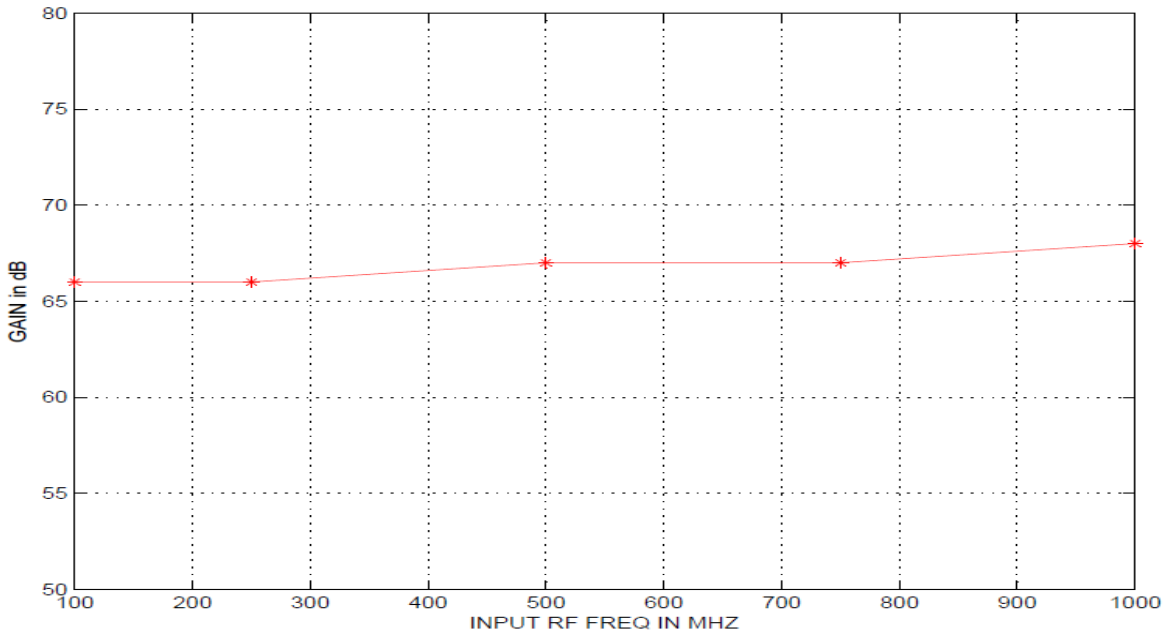

Figure 15 System gain across the band

5.2 Noise Temperature of the Receiver:

The noise in a system can also be expressed as an equivalent noise temperature T_e. The receiver input noise temperature is calculated using liquid nitrogen by Y factor method. The Y factor method involves measuring the system noise power output when input is terminated 1) with a hot termination of known temperature (290 K room temperature) of 2) with a cold termination of known temperature (77 K), as illustrated in figure 16.

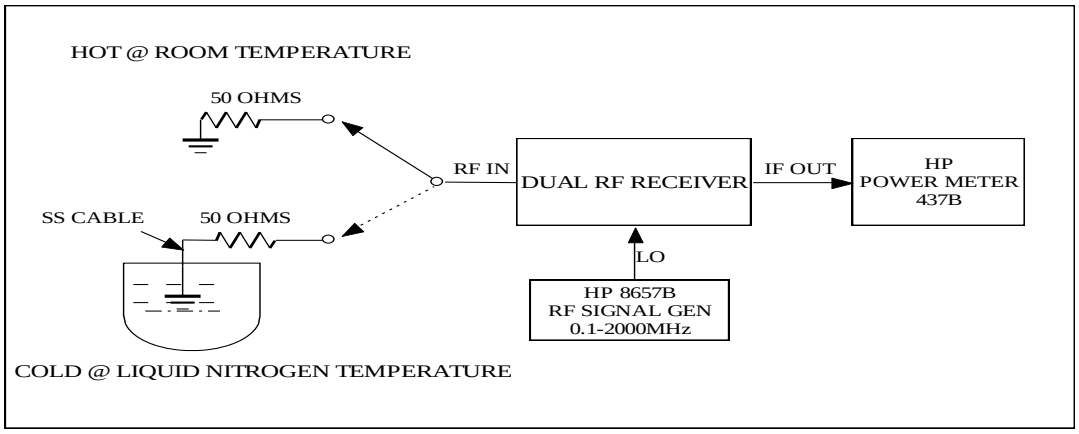

Figure 16. Setup used to measure the Noise temperature of the system

The formula used to calculate the Noise temperature of the receiver (TR) is

TR = ((TH-TC)/(Y-1))-290

Where Y = (VH/VC)-1

The measurements were done at the range of RF across the band, by suitably varying the LO. The red curve(***) and the blue curve (+++) shown in the figure 17 indicates the measured TR values for CH1 and CH2 respectively.

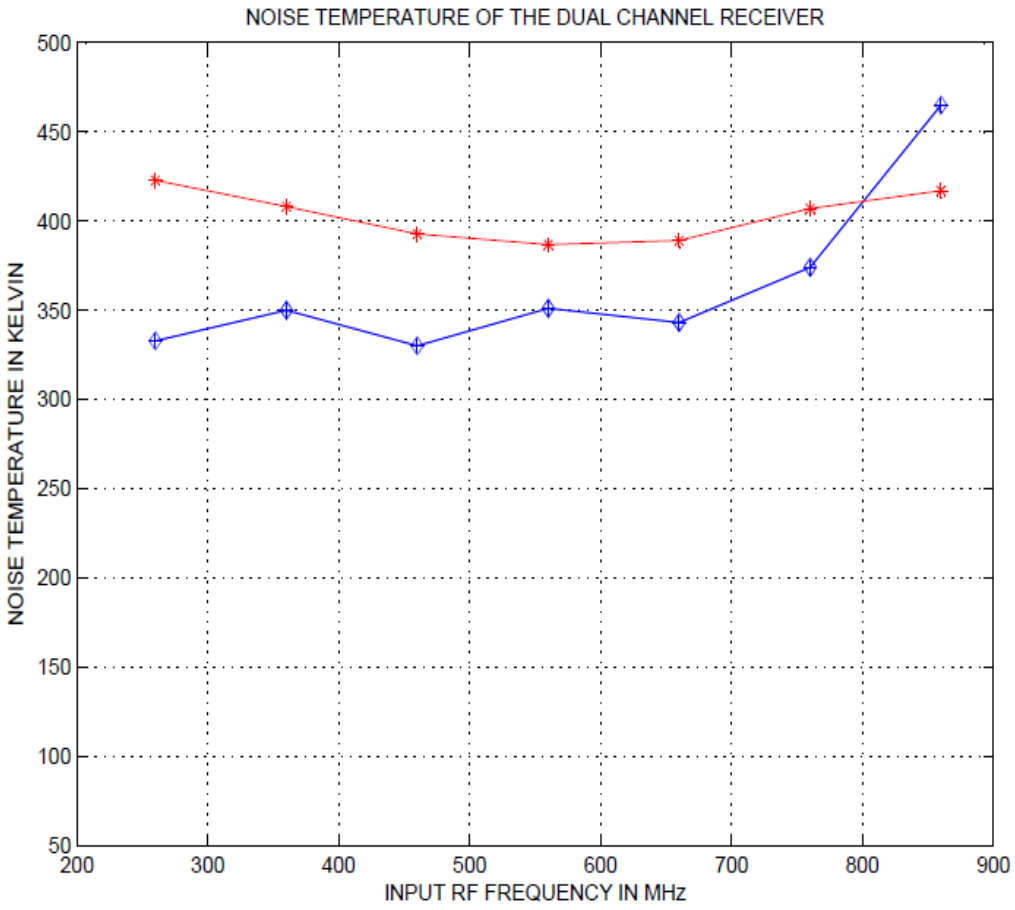

Figure 17. Noise temperature of the system

From these measurement, the Noise Temperature of this receiver over 250 - 850 MHz is in the range : 380K - 430K.

The effective receiver temperature will of course depend largely on the noise temperature of the first amplifier following the antenna elements. Often these amplifiers are particularly low noise amplifiers making the effective noise temperature of the signal chain much smaller than the values quoted above for this portable receiver.

5.3 LINEARITY AND DYNAMIC RANGE OF THE RECEIVER

While amplifying the weak astronomical signals to a usefully recordable level, the amount of gain required is often very high. It is important therefore to ensure that the receiver caters to the demanding requirements of high gain and high dynamic range, simultaneously. Although the variations in the sky signals are usually not very high, presence of man-made signals in the observing band can be high enough to drive the system to non-linear performance, if not to saturation. When an amplifier or other circuit becomes non-linear, it will begin to produce harmonics of the amplified inputs. The second, third, and higher harmonics are usually outside of the amplifier bandwidth, so they are usually easy to filter out if their strengths are beyond acceptable levels. However, non-linearity will also produce a mixing effect of two or more signals.

If the signals are close together in frequency, some of the sum and difference frequencies called intermodulation products produced can occur within the bandwidth of the amplifier. These cannot be filtered out, so they will ultimately become interfering signals to the main signals to be amplified. This may happen even due to interference signals that may be even outside the eventually selected band, but would have produced intermodulation products within the desired band, before filtering. That's why every effort must be made to control the biasing, signal levels, and other factors to ensure maximum possible linearity, greatly reducing the intermodulation distortion (IMD) products, at every stage. The linearity of the system can be examined by measuring input-output relation across a wide range of inputs, as described in the measurements below, in particular, the 1-dB gain compression point, as well as the point at which the third-order product becomes significant.

A. Input 1-dB compression point at the band center : -60dBm.

The 1-dB compression point gives the input power point where the compression begins and distortion will occur. This means the receiver should be always operated below the compression point, defining the maximum level of allowed input.

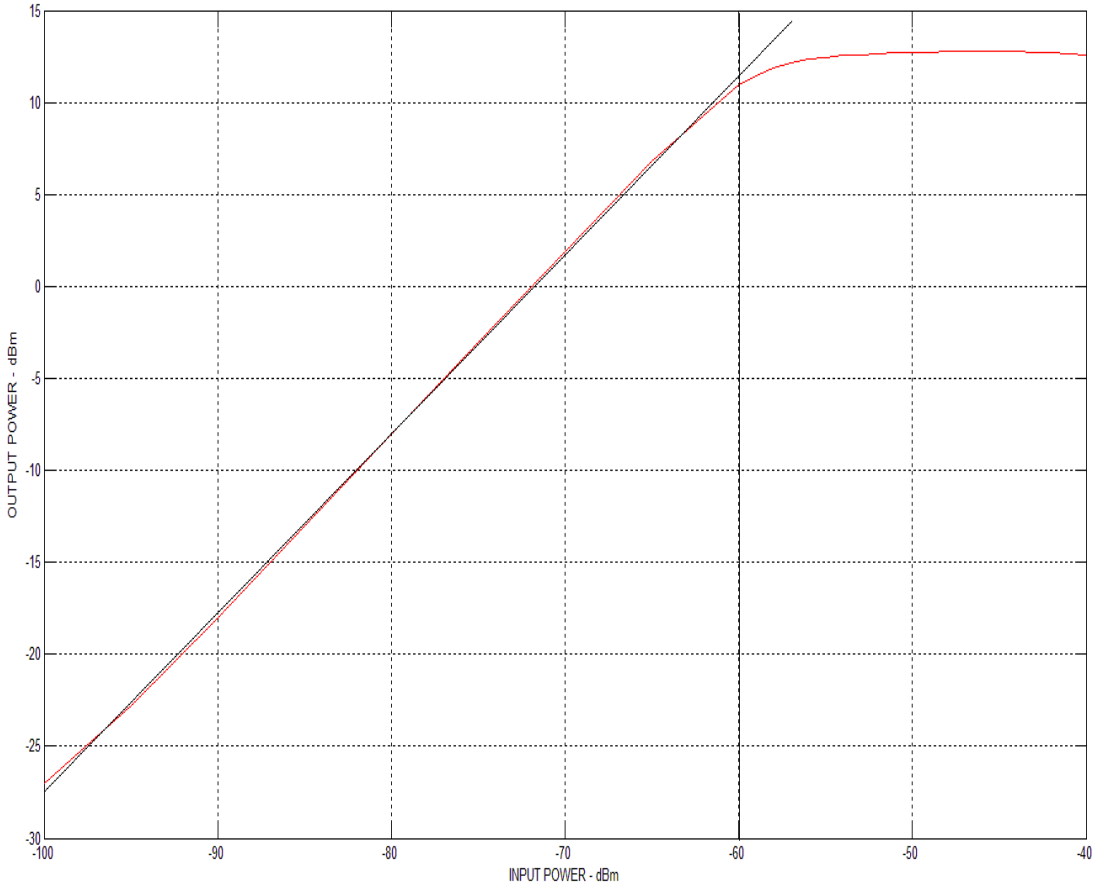

Figure 18. 1dB gain compression of the system is identified by the departure of the gain curve (red) from the linear trend (black).

B. IP3 MEASUREMNETS

The output IP3 measurement of the dual analog receiver system has been carried out by accessing the levels of the spurious 3rd order inter-modulation products generated by system, for given RF input signals separated by smallest resolution like 1MHz and found to be +10dBm to +12dBm in the frequency range from 100MHz-1GHz.

The RF input levels of the two frequencies 300MHz and 301MHz were set @-60dBm.The spurious IMD products at the IF output was found to be -16.54dBm and -15.74dBm at 138MHz and 141MHz respectively.

C. Other Measured results of the Receiver:

- The leakage of the LO component in the IF band has been measured by noting the difference between its amplitude from the pedestal outside the IF band. The LO leakage was not visible as a distinct feature above the pedestal. Based on this, we estimate the possible leakage to be well below ~35dB w.r.t. the IF band, when the RF attenuation was set to 16 dB.

- The dynamic range of the receiver is where the receiver can operate in the linear region, without reaching the gain compression. The dynamic range was measured to be 30dB, from the minimum detectable input signal (usually defined by the system noise).

- The Isolation between the channels was measured by injecting power only at channel 1 and measuring the output power at channel 2, with input terminated at channel 2. The isolation was found to be ~40 dB between the channels.

6. Description of the Portable Dual Digital Back-End Receiver:

6.1 Digitizer :

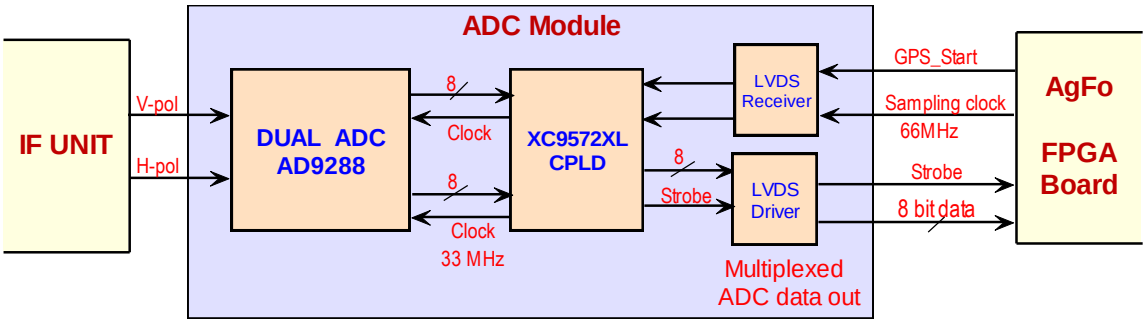

Figure 19. Block diagram of the digitizer

The IF signals for the two channels, each with 16 MHz bandwidth & centred at 140 MHz, are digitized directly using harmonic sampling with a clock of 33MHz . A low-power, 8-bit dual-channel ADC (AD9288) capable of operating at 100 mega samples per second, and with an analog bandwidth of 475 MHz is used for this purpose. The basic block diagram of the

digitizer is as shown in the figure 19. The ADC is controlled by a CPLD (Complex Programmable Logic Device; XC9572XL), configured using VHSIC hardware description language (VHDL), where an input clock at twice the desired sampling frequency is de-multiplexed and fed to the two channels of the ADC. At the start of each acquisition, the clocks are synchronized with respect to 1 PPS signal generated from GPS-disciplined rubidium standard. The dual channel 8-bit samples along with strobe are time multiplexed and passed to the FPGA board.

6.2 AgFo - virtex 5 FPGA board

The ADC data are collected in the PC using Ethernet interface, implemented using AgFo board containing Virtex 5 FPGA. The 8-bit parallel input stream at the rate of about 66 mega-samples per second, representing multiplexed raw voltage samples from the two channels (orthogonal polarizations or from two apertures) is received, and after appropriate packetization, the data are transmitted to the PC on a Gigabit Ethernet (GbE) channel. The FPGA firmware for this purpose has been developed in VHDL. The GbE interface logic is realized on the FPGA using the intellectual property (IP) core "Embedded Tri-Mode Ethernet MAC Wrapper v1.3" provided by Xilinx. The basic block diagram of the digital back-end receiver is shown in Figure 20. The on-board FPGA is programmed through a USB port from the PC via a USB1.1 controller board.

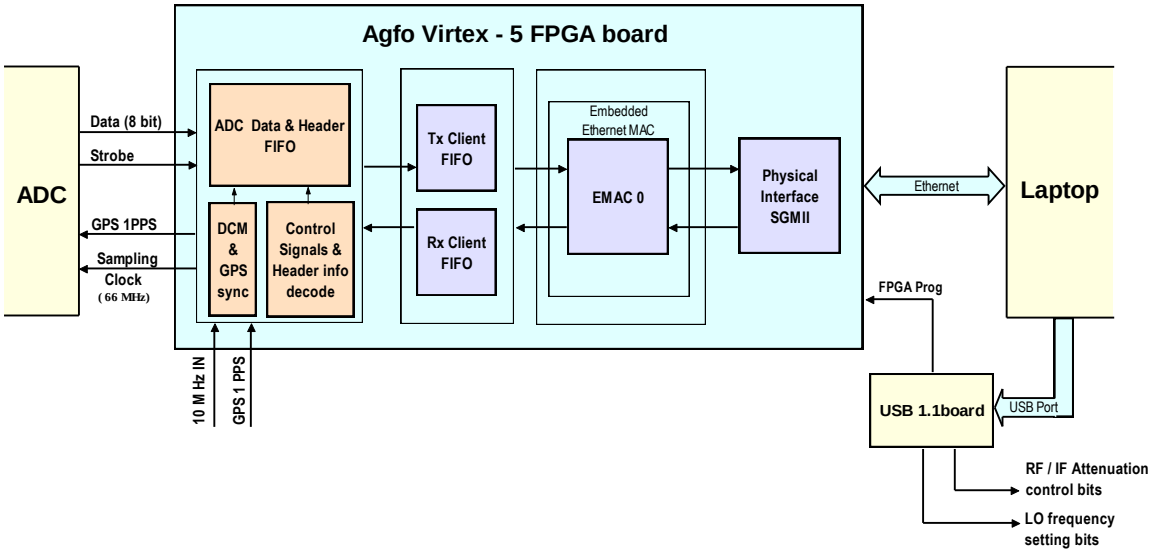

Figure 20. Block diagram of the Digital back-end, consisting of ADC, Virtex-5 FPGA board and computer-based control & DAS

The functionality in the FPGA includes generation of sampling clock (66 MHz, used for the ADC) and 100 MHz clock used for reading the ADC data buffered through FIFO (First In First Out). These programmable clocks are generated from an input reference clock at 10 MHz (from rubidium standard) using the digital clock manager (DCM) blocks in the FPGA. A GPS-disciplined rubidium-based 1PPS input to the FPGA is used for both, synchronization at the start of the acquisition as well as for its time-stamping. Several pieces of information relevant to receiver settings and acquisition details (sent from the control software on the PC) are decoded, using a separate firmware, before their inclusion in the packet header.

The FPGA logic is designed to transmit the data and header information in packet form, using the user datagram protocol (UDP). Each data packet consists of 42 bytes of protocol header (Ethernet, IP and UDP headers), 32 bytes of MBR header (which contains the identity of the receiver, status information like mode of operation, GPS counter, and packet counter), and 1024 bytes of digitized data (dual-polarization, interleaved), as shown in Figure 21. Any change made in the system settings is reflected instantaneously in the headers associated with the acquired data.

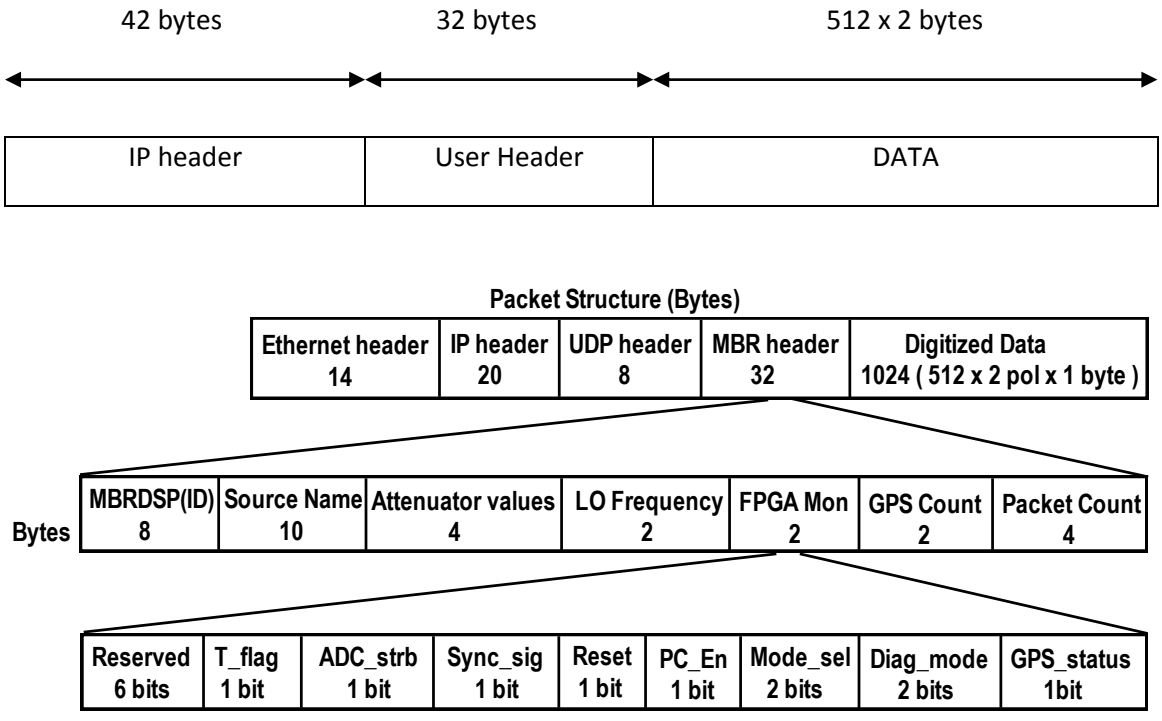

Figure 21. Ethernet Packet Structure

6.3 Clock Generation and Distribution Board

The AD9513 is a high speed and very low jitter clock generation and distribution board. Figure 22 shows a simplified block diagram of the board. This board uses AD9513 chip from Analog Devices that features three-output clock distribution IC in a design that emphasizes low jitter and phase noise. There are three independent clock outputs that can be set to either LVDS or CMOS levels. The AD9513 device is programmed by means of 11 pins labelled ‘S0’ to ‘S10’ using 4-level logic. The board uses ICS8543 chip from Integrated Circuit Systems, which is a low skew, high performance 1-to-4 Differential-to-LVDS Clock fanout buffer.

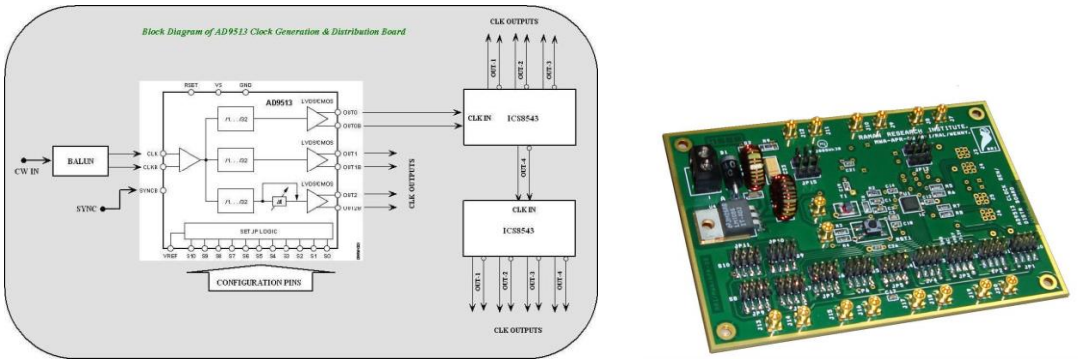

Figure 22. Clock generation and distribution board

The 10 MHz clock from a standard Rubidium source is received by this card which is converted to differential signal and forms the reference clock to be used in the FPGA.

7. Control and Data Analysis software

The monitoring and control as well as data acquisition software which were specially developed for the GBT-RRI MBR system were used in this receiver system also. The command-based control facilitates (a) setting of RF/IF attenuation and LO frequency relevant to the Analog section, and (b) GPS synchronization, specifying bit-length/sample, duration and mode of acquisition for the Digital back-end system. The data acquisition program records packeted data to the local/external hard disk at 66 MHz data rate. This recorded data is used for subsequent processing.

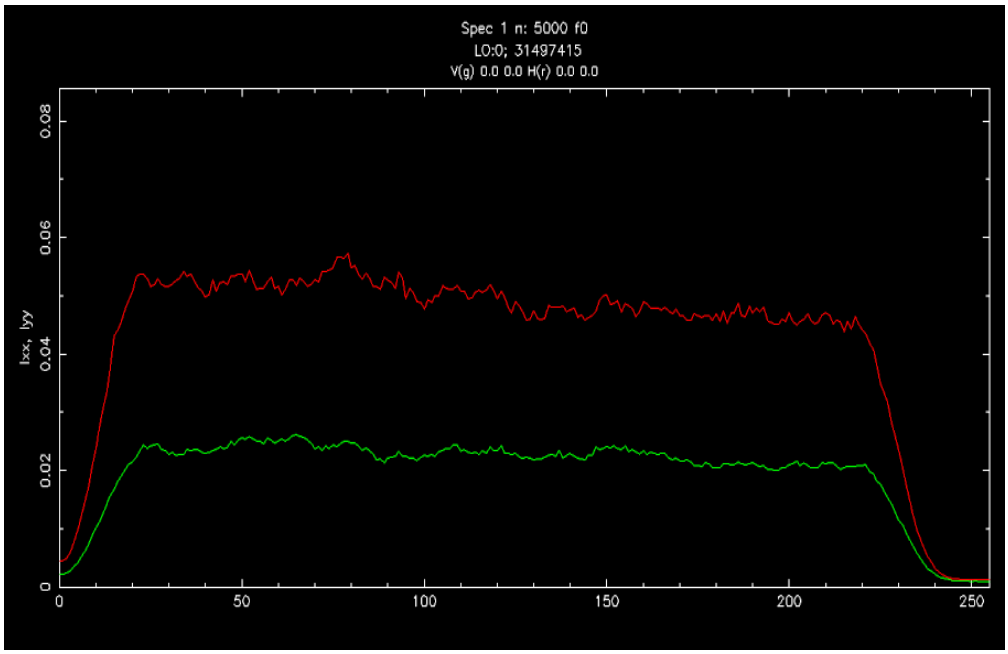

Figure 23. Spectra total power time-sequences of the two channels.

8. Conclusions

We have successfully built a dual channel miniaturised portable receiver which could meet the specifications of the multiband GBT receiver without compromising on the quality of the receiver. The receiver is highly stable and can be used for doing various astronomical observations in any of the observatory. We have achieved good responses in the frequency band of (100 – 1000) MHz. The dynamic range of the receiver is found to be 30dB, from the minimum detectable signal (-98dBm). The 1-dB compression point of both the channels was found to be 12dBmat the output. The Gain of the receiver was found to be approximately 65dB and the noise temperature of the receiver measured with liquid nitrogen test (y- factor method) at 500MHz RF, was found to be approximately 430 K for both channels.

Further tests have been carried out using an antenna such as ST Radar arrays at CUSAT & ARIES with this receiver to observe astronomical sources.

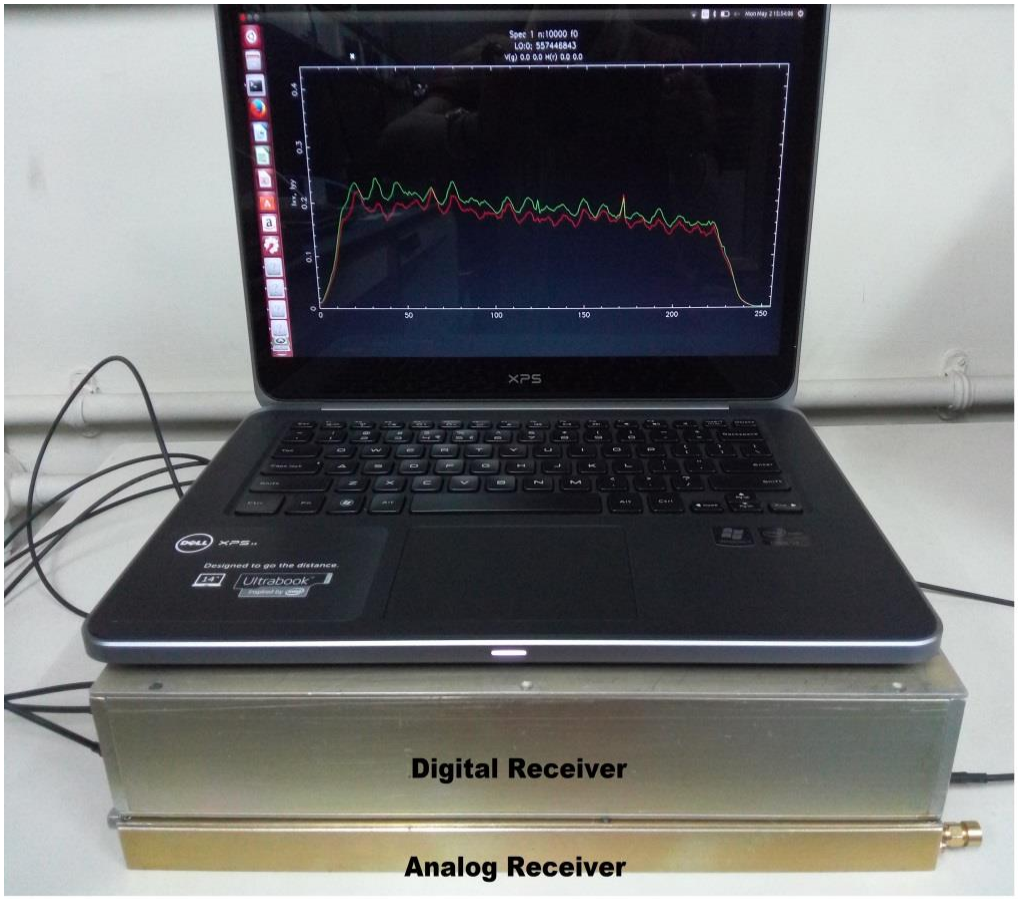

Figure 24 Miniaturised Portable Dual-Channel Receiver System

Acknowledgements

We thank all the members of the EEG and the Mechanical section for providing us all the support in building and testing the "MINIATURISED PORTABLE DUAL-CHANNEL RECEIVER".

References

1. RRI-GBT Multi-Band Receiver : Motivation, Design & Development
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2. Microwave Filters, Impedance-Matching Networks, and Coupling Structures (Artech Microwave Library) [G. Matthaei, E.M.T. Jones, L. Young]

Appendix

Cost Estimation of the Receiver

SL No	Description	Amount (Rs)
1	Analog Receiver	30,000
2	Digital Receiver	1,45,000
3	Mechanical box	20,000
4	Miscellaneous (cables, connectors, etc)	5,000
	Total cost	2,00,000