RRI Technical Report

RRI-EEG Internal

Technical Report No. : 01

Date : Jan. 2, 2018

Integrated Intermediate Frequency Processor Unit for Efficient Linear array Imager

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Abstract :

Efficient Linear array Imager (ELI) is a cross telescope capable of producing 64 beams simultaneously in the sky. It uses 16 receivers and each is likely to use 4 IF chains, making a total of 64 numbers. Clearly, such a large number of IF chains require optimisation of volume, power and cost. Following the model of commercial LNBCs, we have made a prototype integrated IF processor (IFP) board for use with ELI. This integrates 3 gain stages totalling a gain of 60 dB, a directional coupler, a SAW filter and a mixer, all in a board size of 14 cm x 5 cm. This integrated IF processor has avoided multiple SMA connectors and thereby improving reliability at the cost of inter-changeability. In this technical report, we describe the effort put in development of this prototype.

1.Introduction

Efficient Linear array Imager (ELI) is a cross telescope obtained by laying two fan-beam telescopes orthogonal to each other. It will form 64 simultaneous beams on the sky using 16 receivers. It is also envisaged that 4 spectral lines be simultaneously observed using this. This implies that one needs 64 IF chains. Such a large number of IF chains will occupy large volume, be heavy, consume more power and overall cost more, owing to boxes and connectors. Therefore, it is desirable that one makes an integrated IFP board that is compact, economical

and consumes less power. In this technical report, we describe our effort in developing an integrated IFP board which processes the first IF signal located anywhere in the frequency range 0-3500 MHz to generate 2nd IF output with sufficient power centred at 403MHz, over a bandwidth of 8MHz, so that it may be digitised. The motivation in building an integrated IFP is given in Section 2. IFP board is described in section 3. Fabrication details are given in section 4 and the measurement results are in section 5. Section 6 concludes with the summary of work carried out.

2.Motivation

As mentioned, ELI requires a large number of IF chains and it is necessary to reduce the overall weight, cost, power consumption while improving reliability. Thus, the motivation for building an integrated IFP unit is to i) minimize the number of connectors and cables ii) make the system compact, light weight, efficient and reliable for using it in the ELI receiver system.

3.Description of the Integrated IF Processor

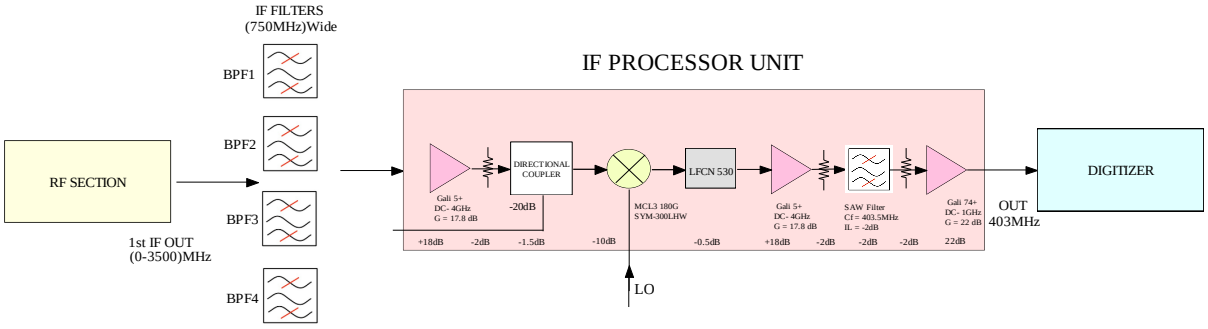


Figure 1. Block diagram of the IF Processor

The basic purpose of the IFP unit is to i) down-convert the 1st IF signals received from the Front End unit to 2nd IF, ii) band-limit it to 8 MHz and iii) amplify the signal to the level required for digitising iv) avoid aliasing and minimise additional noise and insertion losses.

The RF section produces (0-3500) MHz wide output. This is split into four sub-bands of 750 MHz and the first BPF selects one of the four sub-bands (eg.750-1500) and feeds this band-limited signal to the IFP unit. In the IFP unit, the signal is amplified using post amplifiers and down converted to 403 MHz using a broad band mixer by appropriately using a Local

Oscillator (LO) signal. The down converted signal is band limited to 8MHz using a SAW filter. Then the IF output is brought out to be connected to the digitizer for sampling. Provisions are made in the card to introduce attenuators to control the power level of the signals to the required level. To test the prototype IFP chain built, a band Pass Filter of 300 MHz wide designed in the lab was used in between RF and IF sections. The details of it along with the measurement results are described in the sub Section 3.2.

3.2 Band Pass Filter(BPF) Specification:

- Frequency – 1500MHz – 1800 MHz
- Band Width – 300 MHz
- Roll off - 1.3
- Insertion loss- 1dB
- Return Loss- <15dB
- Stop band attenuation – 60dB

Chose an Inter-digital topology because these filters are most useful in the low microwave frequency range of about 0.5 to 5 GHz. In this region, lumped element filters are difficult to build, and waveguide filters are mechanically large. The inter-digital filter easily fills this gap between low frequency LC filters, and microwave waveguide. Thus, interdigital filters are of interest for frequencies up to 5 GHz and down at least as low as 430 MHz and also these filters are commonly used because they provide reasonably a good pass band characteristics, moderate loss, and fairly high attenuation in the stop-bands. Furthermore, they are simple to build and tune.

This filter was simulated using the Genesys software on a ultram2000 board. We chose Ultralamm2000 board because of its stable electrical properties and it has low loss which extents frequencies upto K-band. To meet the filter specification inter-digital topology with 9^{th} order filter was chosen. This filter was assembled and tested, it required a small amount of tuning to achieve the specified bandwidth which is 300MHz. Fig 2 shows the simulated result of the band pass filter.

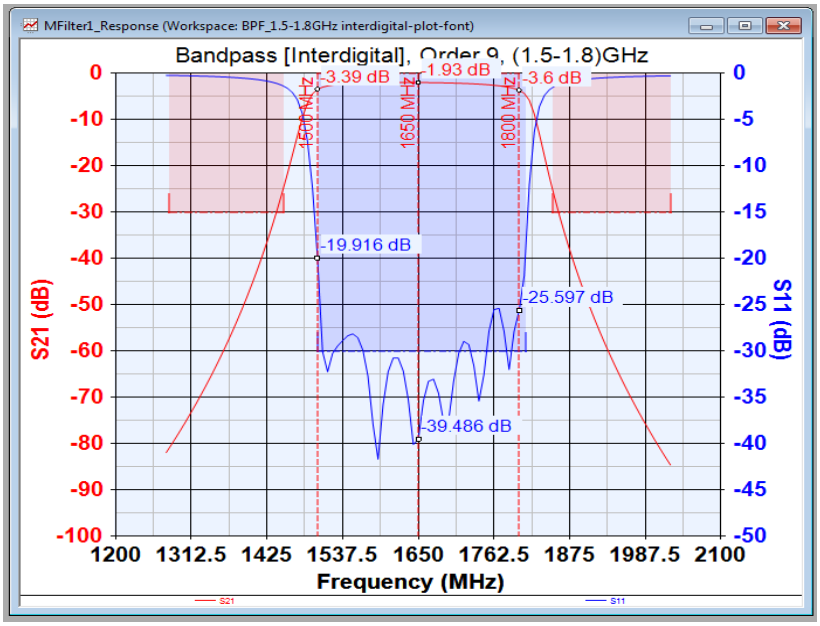


Fig 2 Simulated result of (1500-1800)MHz BPF using Genesys software

The simulated graph shows insertion loss of 1.93dB, return loss of <25 dB and 3 dB bandwidth is slightly less than 300MHz which is mentioned in the table below.

	Expected	Achieved
3dB BW	300 MHz	296MHz
Insertion Loss	<1.93dB	2dB
Return Loss	25dB	20dB
Roll off	1.3	1.33

4. Fabrication Details

4.1 Band Pass Filter Layouts

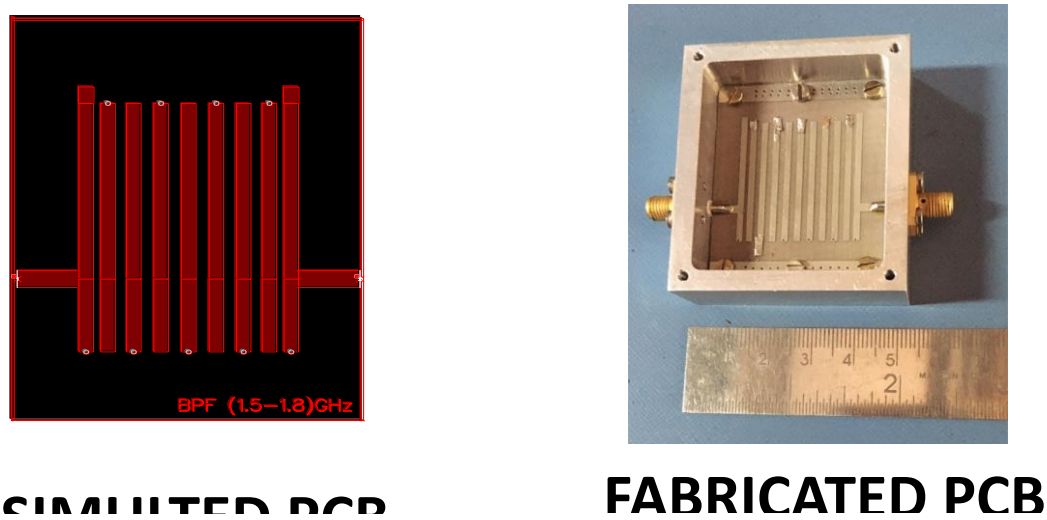


Fig 3 Simulated and the Fabricated Layout of the BPF

4.2 Integrated IF Processor

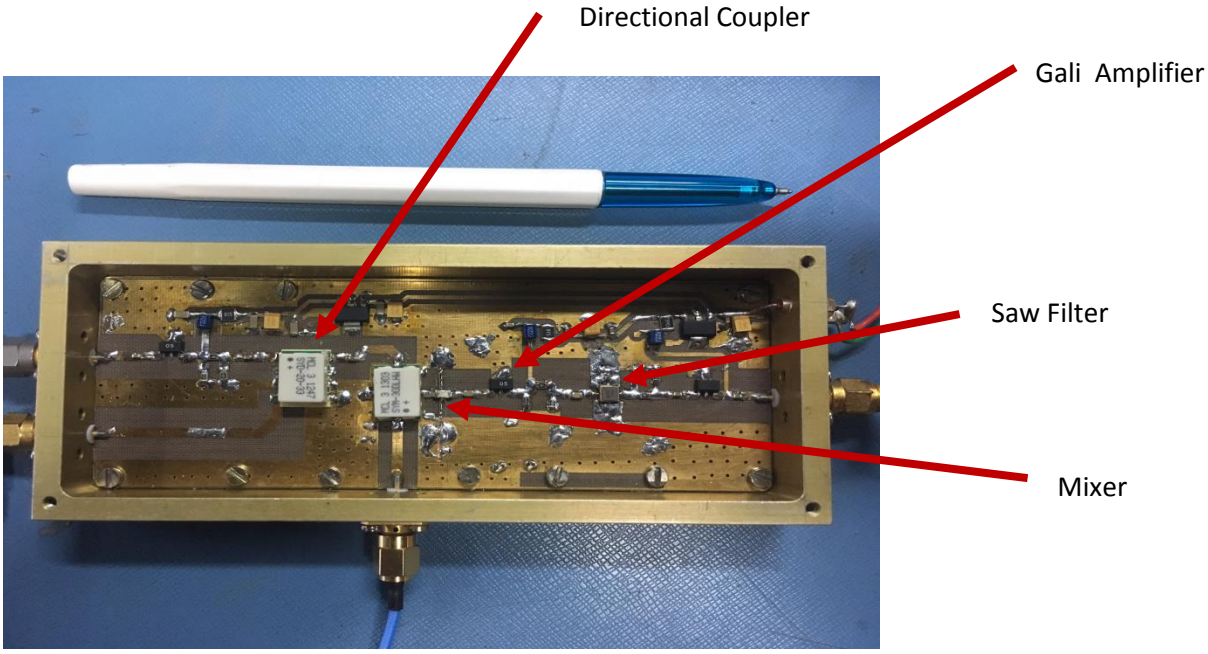


Figure 4. Assembled IFP Chain

Fig 4 shows an assembled printed circuit board of the IFP chain. Top layer carries RF components and transmission line with a ground on the bottom side. Sufficient number of vias are provided on the pcb to ensure good grounding. This also helps minimize parasitic ground inductance. Care is taken to provide good isolation between the RF and DC by providing RF choke in the dc path. This compact intermediate frequency chain is assembled in a milled box. SMA connectors are provided for the RF input and IF output, LO input and coupled port. Coupled port is used for monitoring the power level of the input RF signal. A feed thru filter is used at the output for providing the DC bias for the amplifier and to minimize RF leakage into the power supply line.

5.Measurement Results

5.1 Measurement result of the Band Pass Filter

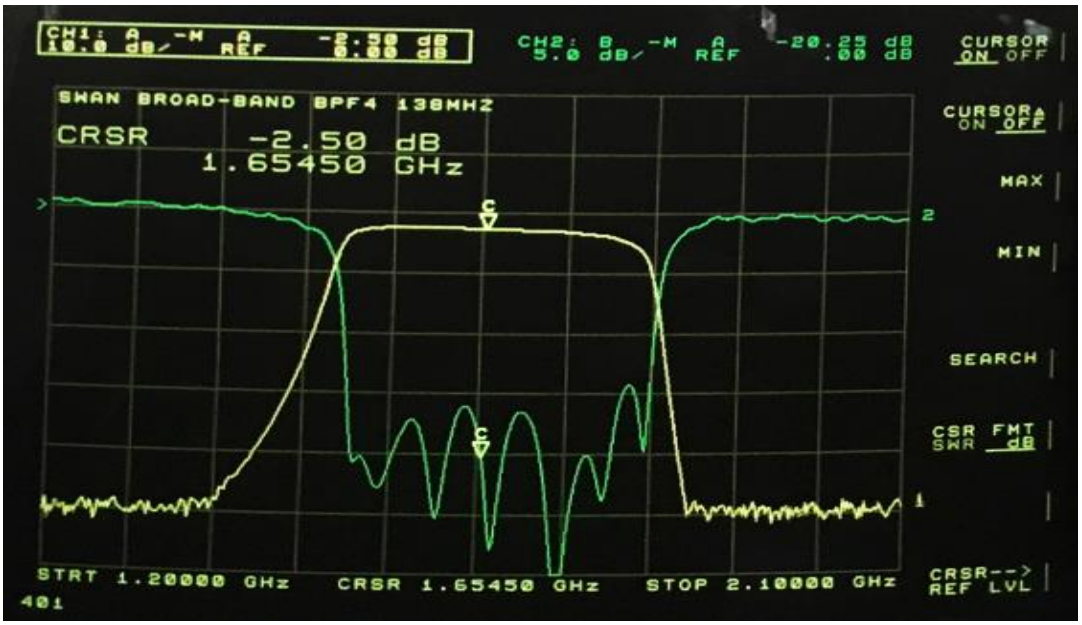


Fig 5 : Measured result of the Band Pass Filter (1500-1800)MHz

5.2 Measurement Results of IFP Chain

To characterize the total gain of the IFP chain, we used a home made Noise Generator NC513 operating in the frequency range 200kHz to 2 GHz. It had an ENR of 48dB giving a power output of -28dBm over 2 GHz. Used a Signal Generator to feed the LO signal and the output

of the IFP unit was measured using the VNA in the Spectrum Analyser mode. Experimental setup used for the measurement is shown in the Fig 6.

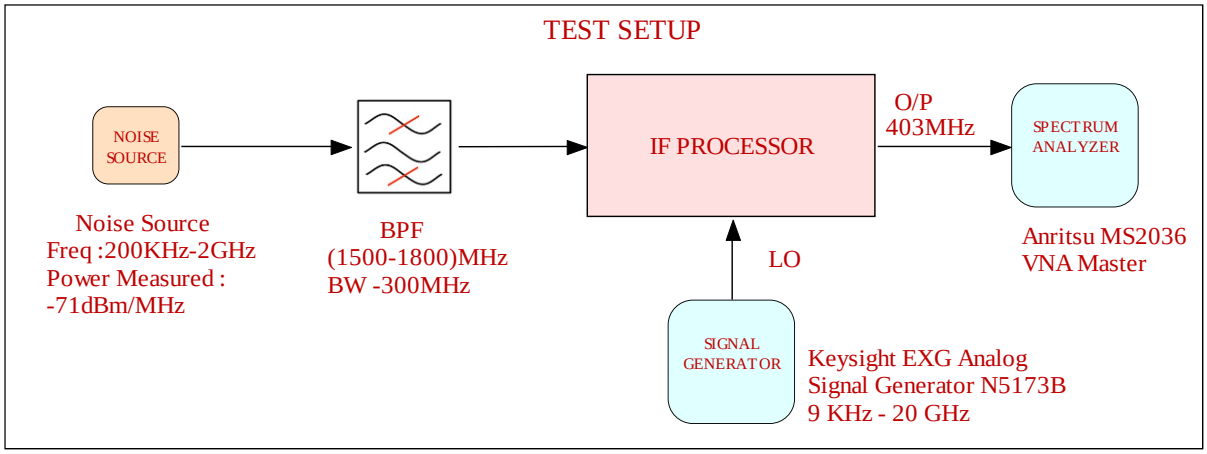


Figure 6. Test Setup of the Intermediate Frequency Processor Chain

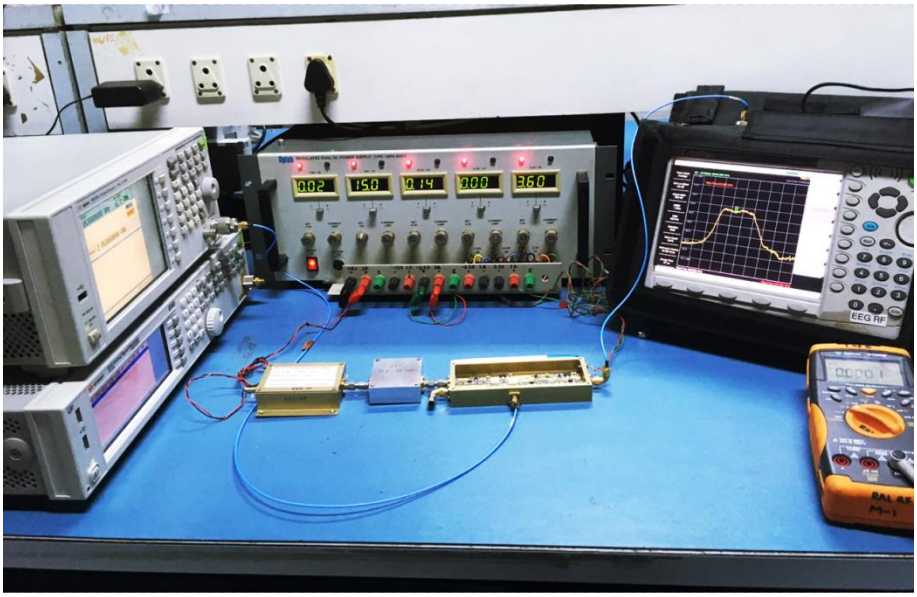
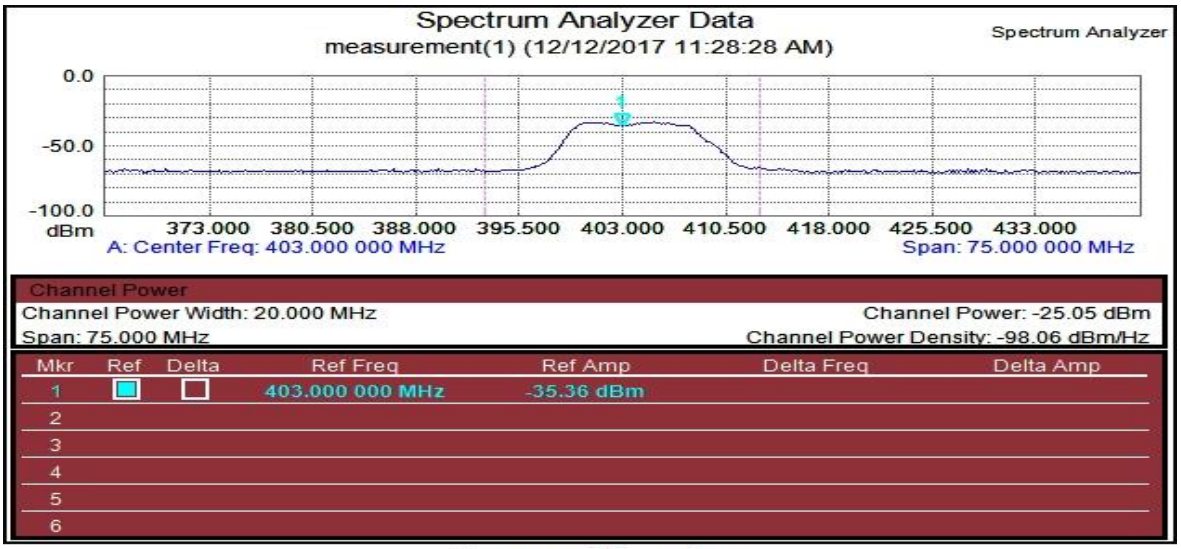


Figure 7. Test Setup of the Intermediate Frequency Processor in the Lab

Channel Power Measurement



Measurement Parameters

Trace A data:Trace Average	10	Start Frequency	365.500 000 MHz
Trace Mode	Average	Stop Frequency	440.500 000 MHz
Preamp	OFF	Frequency Span	75.000 000 MHz
Min Sweep Time	0.001 S	Reference Level	0.000 dBm
Reference Level Offset	0 dB	Scale	10.0 dB/div
Input Attenuation	20.0 dB	Serial Number	726040
RBW	1.0 MHz	Base Ver.	V2.01
VBW	300.0 kHz	App Ver.	V3.17
Detection	RMS	Date	12/12/2017 11:28:28 AM
Center Frequency	403.000 000 MHz	Device Name	RRI

Figure 8. Channel Power measurement of the IF Processor Chain

Gain of the IFP is measured as

I/P Power/8MHz = - 62dBm

O/P Power/8MHz = -23dBm

Therefore Total Gain = 39dB

6. Conclusions

We have successfully built the Integrated Intermediate Frequency Processor unit which could meet the expected results. The performance is found repeatable over many measurement cycles. The total gain of the IFP is ~39dB. Further tests need to be carried out with the RF chain and with the digitizer for sampling.

Acknowledgement

We thank Nagaraj H N for helping us with PCB fabrication process and Mohamed Ibrahim for providing us with milled boxes for the IFP chain and Band Pass Filter.

References

1.Reinhold Ludwig and Pavel Bretchko, "RF Circuit Design".

2. G. Matthaei, E.M.T. Jones, L. Young, "Microwave Filters, Impedance-Matching networks, and Coupling Structures (Artech Microwave Library)".